MCP6C02

Zero-Drift, 65V High-Side Current Sense Amplifier

Features

- Single Amplifier: MCP6C02
- Bidirectional or Unidirectional
- Input (Common-mode) Voltages:
  - +3.0V to +65V, specified
  - +2.8V to +68V, operating
  - -0.3V to +70V, survival
- Power Supply:
  - 2.0V to 5.5V
  - Single or Dual (Split) Supplies
- High DC Precision:
  - V_{OS}: ±1.65 µV (typical)
  - CMRR: 154 dB (typical)
  - PSRR: 138 dB (typical)
  - Gain Error: ±0.1% (typical)
- Preset Gains: 20, 50 and 100 V/V
- POR Protection:
  - HV POR for $V_{IP} – V_{SS}$
  - LV POR for $V_{DD} – V_{SS}$
- Bandwidth: 500 kHz (typical)
- Supply Currents:
  - I_{DD}: 490 µA (typical)
  - I_{BP}: 170 µA (typical)
- Enhanced EMI Protection:
  - EMIRR: 118 dB at 2.4 GHz (typical)
- Specified Temperature Ranges:
  - -40°C to +125°C (E-Temp part)
  - -40°C to +150°C (H-Temp part)

Typical Applications

- Automotive (see Product Identification System)
  - AEC-Q100 Qualified, Grade 0 (VDFN package)
  - AEC-Q100 Qualified, Grade 1 (SOT-23 package)
- Motor Control
- Analog Level Shifter
- Industrial Computing
- Battery Monitor/Tester

Related Products

- MCP6C04-020
- MCP6C04-050
- MCP6C04-100

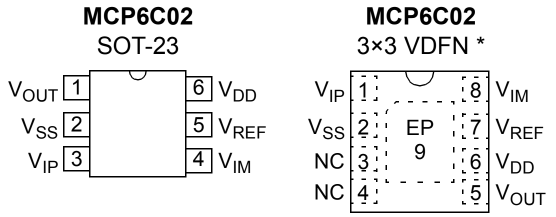
General Description

The Microchip Technology Inc. MCP6C02 high-side current sense amplifier is offered with preset gains of 20, 50 and 100 V/V. The Common-mode input range (V_{IP}) is +3V to +65V. The Differential-mode input range ($V_{DM} = V_{IP} – V_{IM}$) supports unidirectional and bidirectional applications.

The power supply can be set between 2.0V and 5.5V. Parts in the SOT-23 package are specified over -40°C to +125°C (E-Temp), while parts in the 3×3 VDFN package are specified over -40°C to +150°C (H-Temp).

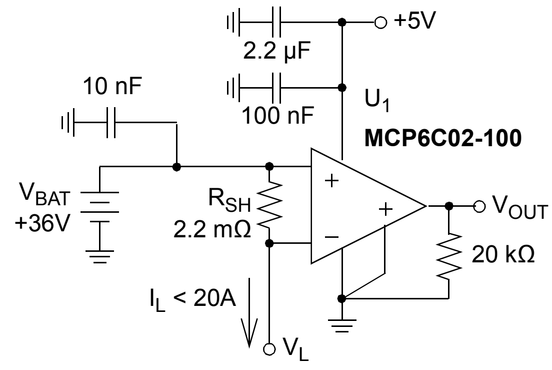
The Zero-Drift architecture supports very low input errors, which allow a design to use shunt resistors of lower value (and lower power dissipation).

Package Types (Top View)

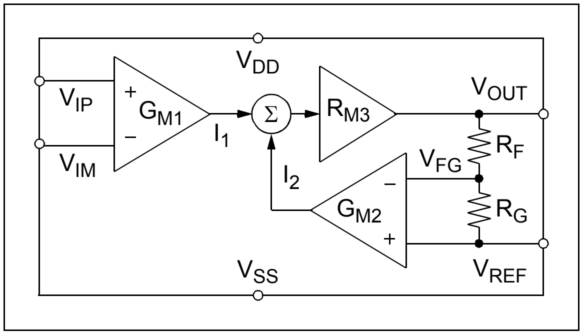


* Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Application Circuit



Functional Diagram



Gain Options

Table 1 shows key specifications that differentiate between the three different differential gain (G_{DM}) options. See **Section 1.0 "Electrical Characteristics"**, **Section 6.0 "Packaging Information"** and the **Product Identification System** for further information on the GDM options available.

TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS

Part No.	G_{DM} (V/V) Nom.	V_{OS} (± µV) Max.	TC_1 (± nV/°C) Max.	CMRR (dB) Min.	PSRR (dB) Min.	V_{DMH} (V) Min.	BW (kHz) Typ.	E_{ni} (μV_{p-p}) Typ.	e_{ni} (nV/√Hz) Typ.
MCP6C02-020	20	16	90	132	109	0.265	500	1.54	74
MCP6C02-050	50	14	70	138	115	0.106		0.95	46
MCP6C02-100	100	12	65		116	0.053	390	0.92	44

Note 1: V_{OS} and TC_1 limits are by design and characterization only.

2: TC_1 covers the Extended Temperature Range (-40°C to +125°C) and the High Temperature Range (-40°C to +150°C).

3: CMRR is at V_{DD} = 5.5V.

4: E_{ni} is at f = 0.1 Hz to 10 Hz. e_{ni} is at f < 500 Hz.

Figure 1, Figure 2 and Figure 3 show input offset voltage versus temperature for the three gain options (G_{DM} = 20, 50 and 100 V/V).

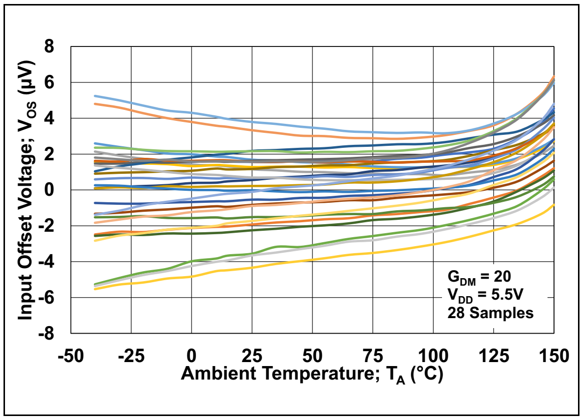


FIGURE 1: *Input Offset Voltage vs. Temperature, G_{DM} = 20 V/V.*

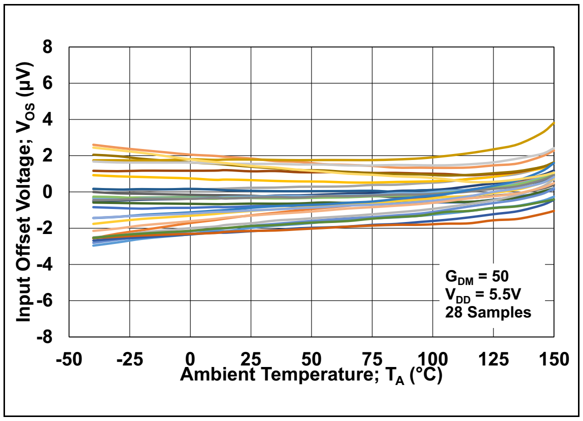


FIGURE 2: *Input Offset Voltage vs. Temperature, G_{DM} = 50 V/V.*

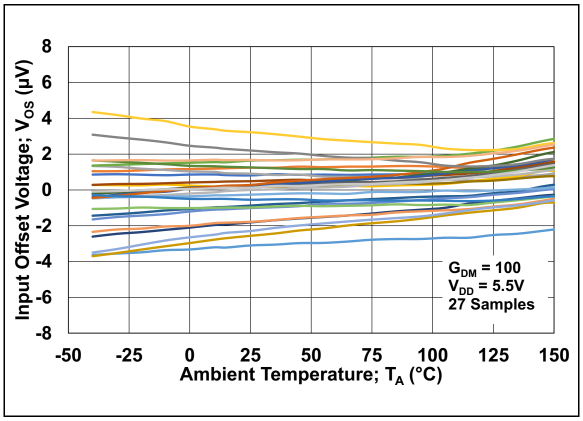


FIGURE 3: *Input Offset Voltage vs. Temperature, G_{DM} = 100 V/V.*

The MCP6C02's CMRR supports applications in noisy environments. Figure 4 shows how CMRR is high, even for frequencies near 100 kHz.

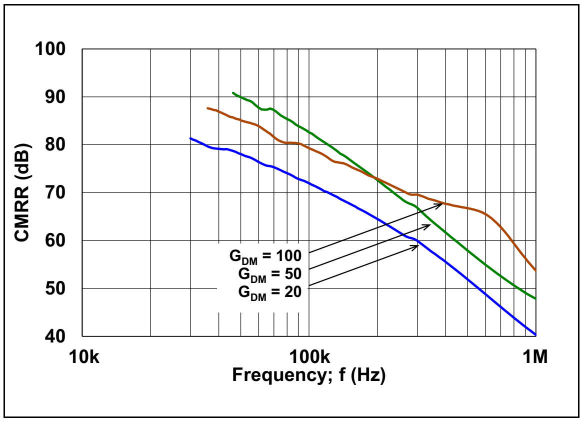


FIGURE 4: *CMRR vs. Frequency.*

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$	-0.3V to +5.5V
Current at Input Pins (Note 1)	±2 mA
Analog Inputs (V_{IP} and V_{IM}) (Note 1)	-0.3V to +70V
All Other Inputs and Outputs	V_{SS} – 0.3V to V_{DD} + 0.3V
Input Difference Voltage (V_{DM}) (Note 1)	±1.2V
Output Short-Circuit Current	Continuous
Current at Output and Supply Pins	±30 mA
Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (Note 2)	+155°C
ESD protection (HBM, CDM, MM)	≥ 2 kV, 2 kV, 300V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: These voltage and current ratings are physically independent; each required condition must be enforced by the user (see **Section 5.1.1 “Input Voltage Limits”** and **Section 5.1.2 “Input Current Limits”**).

2: The Absolute Maximum Junction Temperature is not intended for continuous use.

1.2 Voltage and Temperature Ranges

The various voltage and temperature ranges are listed in Table 1-1.

TABLE 1-1: VOLTAGE AND TEMPERATURE RANGES

Parameter	Units	G_{DM} (V/V)	Comment	Range				
				Type	Sym.	Spec.	Oper.	Abs. Min./Max.
V_{DD} (Note 2)	V	All	V_{DD} ↑ (LV POR on)	Min.	V_{DDL}	2.0	1.7	-0.3
			LV POR Hysteresis		V_{PLH}- V_{PLH}	0.1 Typ.	—	—
			—	Typ.	—	2.0 to 5.5	—	—
				Max.	V_{DDH}	5.5	5.5	5.5
V_{IP} (Note 2)	V	All	V_{IP} ↑ (HV POR on)	Min.	V_{IPL}	3.0	2.8	-0.3
			V_{IP} ↓ (HV POR on)		V_{IPLD}	2.8	2.6	
			HV POR Hysteresis		V_{IPLH}	0.2 Typ.	0.2 Typ.	—
			—	Typ.	—	34	—	—
				Max.	V_{IPH}	65	68	70

Note 1: All of this table’s limits are set by design and characterization.

2: The HV POR is triggered by V_{IP}, with hysteresis. The LV POR is triggered by V_{DD}, with hysteresis.

3: $V_{DM} = V_{IP} – V_{IM}$. V_{IM} is in its range when both V_{IP} and V_{DM} are in their ranges.

4: Allowing the ambient temperature (T_A) to exceed the Maximum Ambient Temperature limit (T_{AH}) may cause parameters to exceed their specified limits. See **Section 1.1 “Absolute Maximum Ratings †”** for the Absolute Maximum Junction Temperature and Storage Temperature limits.

5: V_{OL} and V_{OH} are at R_L = 1 kΩ.

TABLE 1-1: VOLTAGE AND TEMPERATURE RANGES (CONTINUED)

Parameter	Units	G_{DM} (V/V)	Comment	Range				
				Type	Sym.	Spec.	Oper.	Abs. Min./Max.
V_{REF}	V	All	—	Min.	V_{RL}	0	0	-0.3
				Typ.	—	$V_{DD}/4$	—	—
				Max.	V_{RH}	$V_{DD} - 1.25$	$V_{DD} - 1.15$	$V_{DD} + 0.3$
V_{OUT} (Note 5)	V	All	—	Min.	V_{OL}	0.06 Max	0	-0.3
				Typ.	—	$V_{DD}/2$	—	—
				Max.	V_{OH}	$V_{DD} - 0.13$ Min	V_{DD}	$V_{DD} + 0.3$
V_{DM}	V	20	—	Min.	V_{DML}	$-3/G_{DM}$	$-4.25/G_{DM}$	-1.2
		50, 100				$-4.05/G_{DM}$		
		All		Typ.	—	0	—	—
				Max.	V_{DMH}	$5.3/G_{DM}$	$5.5/G_{DM}$	+1.2
T_A	°C	All	E-Temp and H-Temp Parts	Min.	T_{AL}	-40	-40	-40
				Typ.	—	25	—	—
			E-Temp Parts	Max.	T_{AH}	+125	+150	+155
			H-Temp Parts			+150	+155	

Note 1: All of this table's limits are set by design and characterization.

2: The HV POR is triggered by V_{IP}, with hysteresis. The LV POR is triggered by V_{DD}, with hysteresis.

3: $V_{DM} = V_{IP} - V_{IM}$. V_{IM} is in its range when both V_{IP} and V_{DM} are in their ranges.

4: Allowing the ambient temperature (T_A) to exceed the Maximum Ambient Temperature limit (T_{AH}) may cause parameters to exceed their specified limits. See **Section 1.1 "Absolute Maximum Ratings †"** for the Absolute Maximum Junction Temperature and Storage Temperature limits.

5: V_{OL} and V_{OH} are at $R_L = 1\ k\Omega$.

1.3 Specifications

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L; see Figure 1-9 and Figure 1-10.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Input Offset (V_{IP} = V_{IM}) (Note 1)							
Input Offset Voltage	V_{OS}	-16	±1.9	+16	µV	20	Note 2
		-14	±1.65	+14		50	
		-12	±1.5	+12		100	
V_{OS} Drift, Linear Temp. Co.	TC_1	-90	±10	+90	nV/°C	20	T_A = -40°C to +125°C, for E-Temp parts (Note 2, Note 3)
		-70	±8	+70		50	
		-65	±7	+65		100	
V_{OS} Drift, Quadratic Temp. Co.	TC_2	—	±60	—	$pV/°C^2$	20	
			±95			50	
			±105			100	
V_{OS} Drift, Exponential Temp. Co.	TC_X	—	1.8	—	µV	20	
			0.31			50	
			0.10			100	
V_{OS} Aging	ΔV_{OS}	—	±0.18	—	µV	20	108 hr at +150°C (changes measured at +25°C)
			±0.11			50	
			±0.09			100	
TC_1 Aging	ΔTC_1	—	±1.9	—	nV/°C	20	
			±1.1			50	
			±1.0			100	
Power Supply Rejection Ratio	PSRR	109	134	—	dB	20	V_{DD} = 2.0V to 5.5V
		115	138			50	
		116	140			100	
Input Current and Impedance (V_{IP} and V_{IM})							
V_{IP}'s Input Bias Current	I_{BP}	120	170	215	µA	All	V_{DD} = 2.0V to 5.5V
V_{IM}'s Input Bias Current	I_{BM}	—	±0.2	—	nA		V_{DD} = 5.5V
	I_{BM2}		3				V_{DD} = 5.5V, V_{DM} = V_{DML}
	I_{BM3}		-2				V_{DD} = 5.5V, V_{DM} = V_{DMH}
Capacitance at V_{IP}	C_{VIP}	—	40	—	pF		
Capacitance at V_{IM}	C_{VIM}		11				
Capacitance across V_{DM}	C_{VDM}		12				

Note 1: The V_{IP} input is treated as the Common-mode input (e.g., for CMRR). V_{DM} = (V_{IP} – V_{IM}).

2: Set by design and characterization. V_{OS} is screened in production (see **Appendix B: "Offset Test Screens"**).

3: See the discussion in **Section 1.6.2, Input Offset Related Errors**.

4: See **Section 1.6, Explanation of DC Error Specifications**.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L; see Figure 1-9 and Figure 1-10.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Input Common-Mode Voltage (V_{IP})							
V_{IP}'s Voltage Range Low	V_{IPL}	—	2.4	3.0	V	All	V_{IP} ↑
	V_{IPLD}		2.15	2.8			V_{IP} ↓
	V_{IPLH}		0.2	—			$V_{IPLH} = V_{IPL} – V_{IPLD}$
V_{IP}'s Voltage Range High	V_{IPH}	65	—	—			
Common-Mode Rejection Ratio	CMRR	132	159	—	dB	20	V_{DD} = 2.0V to 5.5V, V_{IP} = 3V to 65V
		138	163			50	
			165			100	
Common-Mode Nonlinearity (Note 4)	INL_{CM}	—	±0.006	—	ppm	All	V_{DD} = 5.5V, V_{IP} = 3V to 65V
Reference Voltage (V_{REF})							
Reference Voltage Range (Note 2)	V_{RL}	—	—	0	V	All	See **Section 5.1.6, Setting the Voltage at VREF**
	V_{RH}	V_{DD} −1.25	—	—			
Gain Resistance	$R_F + R_G$	—	175	—	kΩ	20	
			185			50	
			240			100	
V_{REF} Input Capacitance	C_{REF}	—	11	—	pF	All	
Differential Input (V_{DM}) (Note 1)							
Differential Gain	G_{DM}		20		V/V	20	MCP6C02-020
			50			50	MCP6C02-050
			100			100	MCP6C02-100
Differential Input (V_{DM}) – Continued (Note 1)							
Differential Input Voltage Range	V_{DML}	-3/G_{DM}	—	—	V	20	V_{DD} = 5.5V, V_{REF} = 4.1V, V_L = 0V
		-4.05/G_{DM}				50, 100	
	V_{DMH}	—		5.3/G_{DM}		All	V_{DD} = 5.5V, V_{REF} = 0V, $V_L = V_{DD}$
Differential Gain Error	g_E	—	±0.1	—	%		V_{DD} = 2.0V, V_{REF} = 0.5V, $G_{DM}V_{DM}$ = -0.4V to 1.4V
		-1.6	±0.1	+1.6			V_{DD} = 5.5V, V_{REF} = 2.75V, $G_{DM}V_{DM}$ = -2.65V to 2.65V
		—	±0.1	—			V_{DD} = 5.5V, V_{REF} = 0V, $G_{DM}V_{DM}$ = 0.2V to 5.3V
			±0.1			20	V_{DD} = 5.5V, V_{REF} = 4.25V, $G_{DM}V_{DM}$ = -3V to 1.15V
			±0.1			50, 100	V_{DD} = 5.5V, V_{REF} = 4.25V, $G_{DM}V_{DM}$ = -4V to 1.15V

Note 1: The V_{IP} input is treated as the Common-mode input (e.g., for CMRR). $V_{DM} = (V_{IP} – V_{IM})$.

2: Set by design and characterization. V_{OS} is screened in production (see **Appendix B: "Offset Test Screens"**).

3: See the discussion in **Section 1.6.2, Input Offset Related Errors**.

4: See **Section 1.6, Explanation of DC Error Specifications**.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L; see Figure 1-9 and Figure 1-10.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Differential Gain Drift	$\Delta g_E/\Delta T_A$	—	±5	—	ppm/°C	All	V_{DD} = 2.0V, V_{REF} = 0.5V, $G_{DM}V_{DM}$ = -0.4V to 1.4V
		—	±5	—			V_{DD} = 5.5V, V_{REF} = 2.75V, $G_{DM}V_{DM}$ = -2.65V to 2.65V
g_E Aging	Δg_E	—	±0.15	—	%		408 hr at +150°C, V_{DD} = 5.5V, V_{REF} = 2.75V, $G_{DM}V_{DM}$ = -2.65V to 2.65V, (change measured at +25°C)
Differential Nonlinearity (Note 4)	INL_{DM}	—	±50	—	ppm		V_{DD} = 2.0V, V_{REF} = 0.5V, $G_{DM}V_{DM}$ = -0.4V to 1.4V
			±100				V_{DD} = 5.5V, V_{REF} = 2.75V, $G_{DM}V_{DM}$ = -2.65V to 2.65V
Output (V_{OUT})							
Minimum Output Voltage Swing	V_{OL}	—	3	—	mV	All	V_{DD} = 2.0V, V_{REF} = 0V V_{DM} = -0.5V/G_{DM}
			5				V_{DD} = 5.5V, V_{REF} = 0V V_{DM} = -0.5V/G_{DM}
			20	60			V_{DD} = 5.5V, V_{REF} = 0V V_{DM} = -0.5V/G_{DM}, R_L = 1 kΩ
			3	—			V_{DD} = 5.5V, V_{REF} = 0V V_{DM} = -0.5V/G_{DM}, V_L = 0V
Output (V_{OUT}) – Continued							
Maximum Output Voltage Swing	V_{DD} – V_{OH}	—	6	—	mV	All	V_{DD} = 2.0V, V_{REF} = 0.75V V_{DM} = 1.75V/G_{DM}
			10				V_{DD} = 5.5V, V_{REF} = 4.25V V_{DM} = 1.75V/G_{DM}
			40	130			V_{DD} = 5.5V, V_{REF} = 4.25V V_{DM} = 1.75V/G_{DM}, R_L = 1 kΩ
			5	—			V_{DD} = 5.5V, V_{REF} = 0V V_{DM} = 1.75V/G_{DM}, V_L = V_{DD}
Output Short Circuit Current	I_{SCP}	—	+12	—			V_{DD} = 2.0V, V_{REF} = 1V, $G_{DM}V_{DM}$ = 1.0V
			+20				V_{DD} = 5.5V, V_{REF} = 1V, $G_{DM}V_{DM}$ = 1.0V
	I_{SCM}	—	-12	—			V_{DD} = 2.0V, V_{REF} = 1V, $G_{DM}V_{DM}$ = -1.0V
			-20				V_{DD} = 5.5V, V_{REF} = 1V, $G_{DM}V_{DM}$ = -1.0V

Note 1: The V_{IP} input is treated as the Common-mode input (e.g., for CMRR). V_{DM} = (V_{IP} – V_{IM}).

2: Set by design and characterization. V_{OS} is screened in production (see **Appendix B: "Offset Test Screens"**).

3: See the discussion in **Section 1.6.2, Input Offset Related Errors**.

4: See **Section 1.6, Explanation of DC Error Specifications**.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L; see Figure 1-9 and Figure 1-10.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Power Supplies (V_{DD}, V_{SS} and V_{IP})							
Low Supply Voltage	V_{DD}	2.0	—	5.5	V	All	
High Supply Voltage	V_{IP}	(see V_{IP} spec)					
Quiescent Current at V_{SS}	I_{SS}	—	-660	—	µA		I_O = 0A
Quiescent Current at V_{DD}	I_{DD}	300	490	725			
Quiescent Current at V_{IP}	I_{BP}	(see I_{BP} spec)					
POR Trip Voltages, Low-Side (V_{DD})	V_{PLL}	1.05	1.35	—	V	All	LV POR turns off (V_{DD} ↓), V_L = 0V, V_{IP} = 3V, V_{REF} = 0V
	V_{PLH}	—	1.45	1.7			LV POR turns on (V_{DD} ↑), V_L = 0V, V_{IP} = 3V, V_{REF} = 0V
POR Trip Voltages, High-Side (V_{IP})	V_{PHL}	1.7	1.95	—			HV POR turns off (V_{IP} ↓), R_L = open, V_{DD} = 5.5V (change in I_{SS})
	V_{PHH}	—	2.05	2.6			HV POR turns on (V_{IP} ↑), R_L = open, V_{DD} = 5.5V (change in I_{SS})

Note 1: The V_{IP} input is treated as the Common-mode input (e.g., for CMRR). V_{DM} = (V_{IP} – V_{IM}).

2: Set by design and characterization. V_{OS} is screened in production (see **Appendix B: "Offset Test Screens"**).

3: See the discussion in **Section 1.6.2, Input Offset Related Errors**.

4: See **Section 1.6, Explanation of DC Error Specifications**.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-11.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
AC Response							
Bandwidth	BW	—	500	—	kHz	20, 50	$G_{DM}V_{DM}$ = 0.1V_{p-p}
			390			100	
Gain Peaking	GPK	—	0	—	dB	All	
Step Response							
V_{DM} Slew Rate	SR	(Note 1)			V/µs	All	$G_{DM}V_{DM}$ Step = V_{DD} – 0.5V
V_{DM} Step Overshoot	OS_{DM}	—	4	—	%		$G_{DM}V_{DM}$ Step = 0.1V, t_{r_in} = 0.2 µs
Overdrive Recovery, Input Differential Mode	t_{IRDL}	—	3	—	µs	20	V_{DD} = 5.5V, V_{REF} = 4V, $G_{DM}V_{DM}$ = -3.5V to -1.25V Step, 90% of V_{OUT} change
		(see t_{ORL} Spec)				50, 100	(Note 2)
	t_{IRDH}	—	3	—		All	V_{DD} = 5.5V, V_{REF} = 0.5V, $G_{DM}V_{DM}$ = +4.5V to +2.25V Step, 90% of V_{OUT} change

Note 1: SR is limited by GBWP; the large signal step response is dominated by the small signal bandwidth.

2: At these gains, we cannot distinguish between overdriving V_{DM} or V_{OUT}.

3: See Figure 2-58 for the noise density over a wider frequency range.

4: Not tested; for design guidance only.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-11.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Overdrive Recovery, Output	t_{ORL}	—	1.5	—	µs	All	V_{DD} = 2.0V, V_{REF} = 0V, $G_{DM}V_{DM}$ = -0.5V to +1V Step, 90% of V_{OUT} change
			1.5				V_{DD} = 5.5V, V_{REF} = 0V, $G_{DM}V_{DM}$ = -0.5V to +2.75V Step, 90% of V_{OUT} change
	t_{ORH}	—	1.5	—			V_{DD} = 2.0V, V_{REF} = 0.75V, $G_{DM}V_{DM}$ = +1.75V to +0.25V Step, 90% of V_{OUT} change
			1.5				V_{DD} = 5.5V, V_{REF} = 4.25V, $G_{DM}V_{DM}$ = +1.75V to -1.25V Step, 90% of V_{OUT} change
Noise							
Input Noise Voltage	E_{ni}	—	0.48	—	$\mu V_{p\text{-}p}$	20	f = 0.01 Hz to 1 Hz
			0.30			50	
			0.29			100	
		—	1.54	—		20	f = 0.1 Hz to 10 Hz
			0.95			50	
			0.92			100	
Input Noise Voltage Density (Note 3)	e_{ni}	—	74	—	nV/√Hz	20	f < 500 Hz
			46			50	
			44			100	f < 1 kHz
Input Current Noise Density – At V_{IP}	i_{nip}	—	10	—	pA/√Hz	All	f = 1 kHz
Input Current Noise Density – At V_{IM}	i_{nim}	—	8	—	fA/√Hz		f = 1 kHz, V_{DM} = 0V
			33				f = 1 kHz, V_{DM} = 0.15V
EMI Protection							
EMI Rejection Ratio	EMIRR	—	96	—	dB	All	V_{IN} = $0.1V_{PK}$, f = 400 MHz
			91				V_{IN} = $0.1V_{PK}$, f = 900 MHz
			114				V_{IN} = $0.1V_{PK}$, f = 1800 MHz
			118				V_{IN} = $0.1V_{PK}$, f = 2400 MHz
			121				V_{IN} = $0.1V_{PK}$, f = 6000 MHz
Power Up/Down							
Power On Time (V_{DD} ↑), V_{OUT} Settles	t_{PON}	—	65	—	µs	All	V_{DD} = 0V to 2.0V, V_L = 0V, 90% of V_{OUT} change
			140				V_{DD} = 0V to 5.5V, V_L = 0V, 90% of V_{OUT} change
Power Off Time (V_{DD} ↓), V_{OUT} Settles	t_{POFF}	—	8	—			V_{DD} = 2.0V to 0V, V_L = 0V, 90% of V_{OUT} change
			5.5				V_{DD} = 5.5V to 0V, V_L = 0V, 90% of V_{OUT} change
V_{IP} Edge Rate	$\Delta V_{IP}/\Delta t$	-25	—	+25	V/µs	All	ESD structure not triggered (Note 4)
V_{IP} Bypass Capacitor	C_{VIP}	—	10	—	nF	All	Connects to V_{IP} and GND

Note 1: SR is limited by GBWP; the large signal step response is dominated by the small signal bandwidth.
2: At these gains, we cannot distinguish between overdriving V_{DM} or V_{OUT}.
3: See Figure 2-58 for the noise density over a wider frequency range.
4: Not tested; for design guidance only.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND and V_{IP} = 34V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Specified Temperature Range	T_A	-40	—	+125	°C	E-Temp parts (Note 2)
				+150		H-Temp parts (Note 3)
Operating Temperature Range		-40	—	+150		Note 1
Storage Temperature Range		-60	—	+150		No power
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	191	—	°C/W	

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature specification (155°C), which is not intended for continuous use. See **Section 4.1.5, Temperature Performance** for design tips.

2: Automotive Grade 1 parts use the 6L-SOT-23 package. They can operate continuously at T_A = +125°C, as long as the junction temperature stays below 150°C.

3: Automotive Grade 0 parts use the 8L-3×3 VDFN package. They can operate at T_A = +150°C for a limited time, as long as the junction temperature stays below 155°C.

1.4 Simplified Diagrams

1.4.1 VOLTAGE RANGE DIAGRAMS

These ranges are constant across temperature.

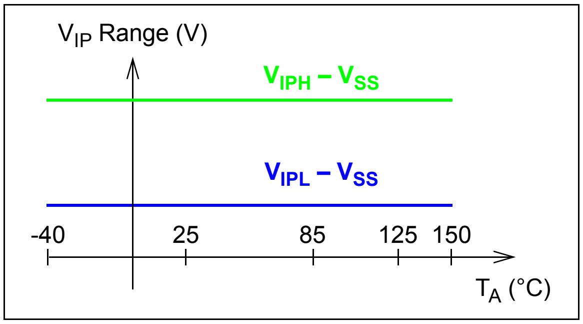


FIGURE 1-1: *Common-Mode Input Voltage Range vs. Temperature.*

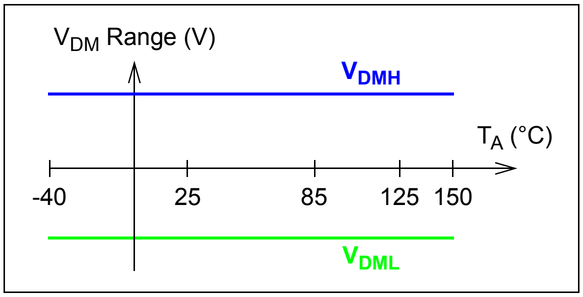


FIGURE 1-2: *Differential Input Voltage Range vs. Temperature.*

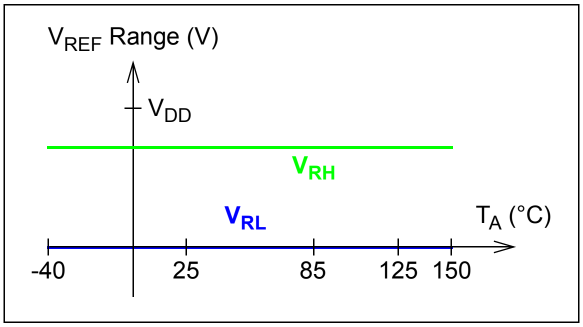


FIGURE 1-3: *Reference Voltage Range vs. Temperature.*

1.4.2 TIMING DIAGRAMS

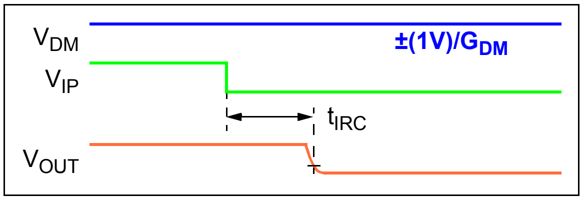


FIGURE 1-4: *Common-Mode Input Overdrive Recovery Timing Diagram.*

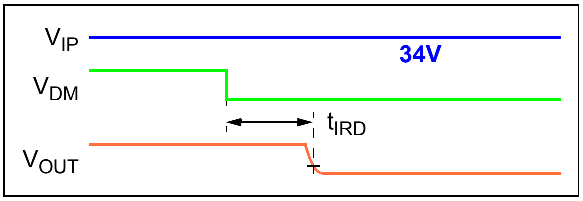


FIGURE 1-5: *Differential-Mode Input Overdrive Recovery Timing Diagram.*

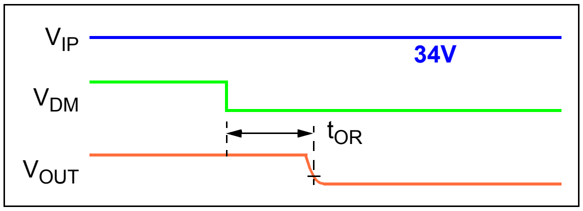


FIGURE 1-6: *Output Overdrive Recovery Timing Diagram.*

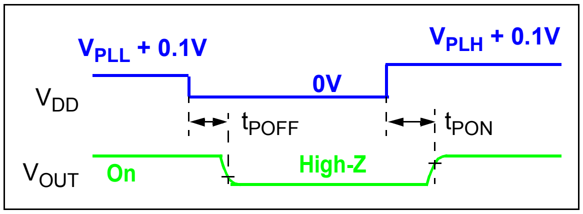


FIGURE 1-7: *V_{OUT} Power On/Off Timing Diagram, Low-Side.*

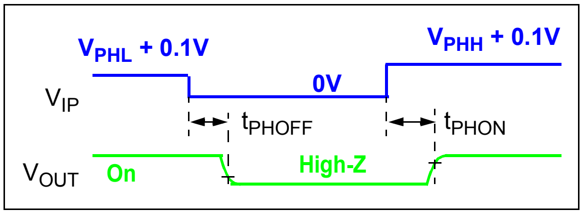


FIGURE 1-8: *V_{OUT} Power On/Off Timing Diagram, High-Side.*

1.5 Simplified Test Circuits

1.5.1 V_{OS} TEST CIRCUIT

Figure 1-9 tests the MCP6C02's input offset errors (V_{OS}, 1/CMRR, 1/CMRR2 and 1/PSRR, etc.). R_{WIP} is set very low, so I_{BP} does not affect the result. V_{OUT} is filtered and amplified, before measuring the result.

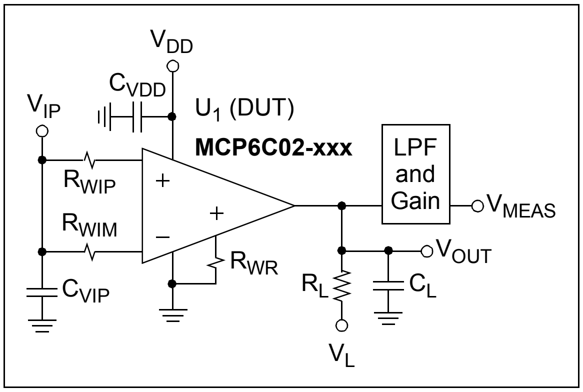


FIGURE 1-9: *Input Offset Test Circuit for the MCP6C02.*

When MCP6C02 is in its normal range of operation, the DC output voltages are (V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-1:

$$
\begin{aligned}
G_{DM} &= \textit{DM Gain} \\
V_{OUT} &= G_{DM}(1+g_E)V_E + V_{REF} \\
V_{MEAS} &= G_{PA}V_{OUT}
\end{aligned}
$$

The resistances at the Device Under Test (DUT) need to be small enough for accuracy (see Figure 1-10). These resistances include wires, traces, vias, etc.

EQUATION 1-2:

$$
\begin{aligned}
R_{WIP} &\le 4\ m\Omega \\
R_{WIM} &\le 0.1\Omega \\
R_{WR} &\le 1\Omega
\end{aligned}
$$

1.5.2 DC DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-10 is used for testing the differential gain error, nonlinearity and input voltage range (g_E, INL_{DM}, V_{DML} and V_{DMH}). We compare V_{MEAS} with the ideal V_{OUT}, then extract the above parameters.

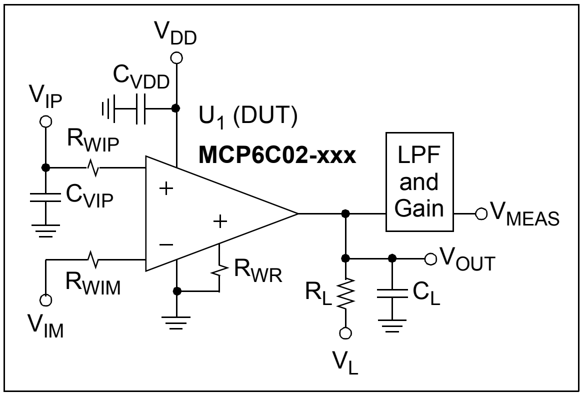


FIGURE 1-10: *Differential Gain Test Circuit.*

When measuring the differential input range, all of the voltages must be in range except V_{DM}.

When measuring differential errors (g_E, $\Delta g_E/\Delta T_A$ and INL_{DM}), all voltages are held constant, except V_{DM}.

For accuracy, the wiring resistances at the DUT need to be very small (see Equation 1-2).

1.5.3 AC GAINS TEST CIRCUIT

Figure 1-11 is used for testing the INA's different AC gains. The AC voltages are:

- v_{out} is the AC output
- v_{ip} is the AC Common-mode input, used for CMRR plots
- v_{dm} is the AC differential input, used for G_{DM} plots (also for CMRR and PSRR)
- v_{dd} and v_{ss} are the AC supply inputs, used for PSRR plots (including PSRR+ and PSRR-)

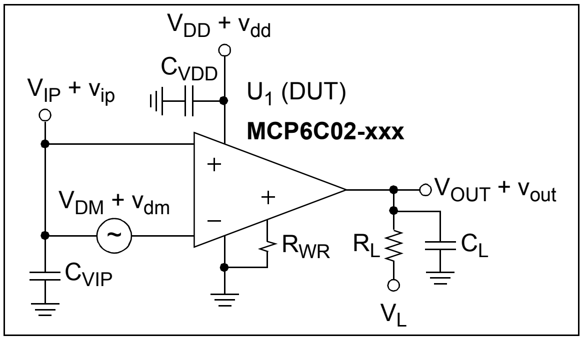


FIGURE 1-11: *AC Gain Test Circuit.*

The impedance at V_{REF} (shown here as R_{WR}) needs to have a magnitude less than 1Ω, for gain accuracy in the signal bandwidth. The magnitude needs to be < 50Ω, when f < 1 MHz, to maintain good stability.

1.6 Explanation of DC Error Specifications

1.6.1 LINEAR RESPONSE MODEL

When the inputs and the output are in their normal ranges, and the nonlinear errors are negligible, the output voltage (V_{OUT}) is:

EQUATION 1-3:

$$V_{OUT} = V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E)$$

V_{DM} is the input voltage. V_E is the sum of input offset errors (due to V_{OS}, PSRR, CMRR, CMRR2, TC_1, TC_2, etc.). g_E is the gain error (G_{DM} is the nominal gain).

1.6.2 INPUT OFFSET RELATED ERRORS

When V_{DM} = 0V, the linear response model for V_{OUT} becomes:

EQUATION 1-4:

$$V_{OUT} = V_{REF} + G_{DM}(1 + g_E)V_E$$

The input offset error (V_E) is extracted from input offset measurements (see **Section 1.5.1 "VOS Test Circuit"**):

EQUATION 1-5:

$$V_E = \frac{V_{OUT} - V_{REF}}{G_{DM}(1 + g_E)}$$

We usually assume $g_E = 0$, in Equation 1-5, when extracting V_E. The result is accurate enough, since g_E is so low.

V_E has several terms, which assume a linear response to changes in V_{DD}, V_{SS}, V_{IP} and V_{REF}.

V_{OS}'s dependence on temperature (T_A) is quadratic plus exponential (V_{OS}, TC_1, TC_2 and TC_X). The aging specs (ΔV_{OS} and ΔTC_1) are not included, for simplicity.

The exponential factor in Equation 1-6 decreases at colder temperatures (T_A). This table gives an indication of this relationship.

TABLE 1-5: EXPONENTIAL TERM

T_A (°C)	$2^{((T_A - 150°C)/(10°C))}$
≤ 65	≤ 0.003
+85	0.011
+105	0.044
+125	0.177
+150	1.000

EQUATION 1-6:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{IP}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} + \Delta T_A TC_1 + \Delta T_A^2 TC_2 + TC_X 2^{((T_A - 150°C)/(10°C))}$$

Where:

PSRR, CMRR and CMRR2 are in units of V/V
ΔT_A is in units of °C
$V_{DM} = 0$

1.6.3 INPUT OFFSET'S COMMON-MODE VOLTAGE NONLINEARITY

The input offset error (V_E) changes nonlinearly with V_{IP}. Figure 1-12 shows the MCP6C02's V_E vs. V_{IP}, as well as a linear fit line (V_{E_LIN}), that goes through the center point (V_C, V_2) and has the same slope as the end points.

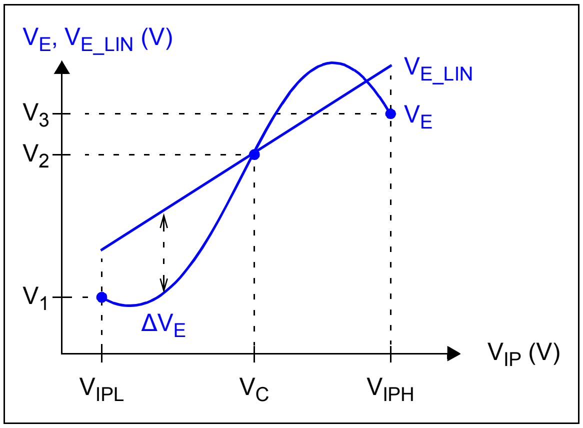


FIGURE 1-12: *Input Offset Error vs. Common-Mode Input Voltage.*

The part is in standard conditions ($\Delta V_{OUT} = 0$, $V_{DM} = 0$, etc.). V_{IP} sweeps from V_{IPL} to V_{IPH}. The test circuit is in **Section 1.5.1, VOS Test Circuit**. Calculate V_E at each point with Equation 1-5.

Based on the measured V_E data, we obtain the following linear fit:

EQUATION 1-7:

$$V_{E\_LIN} = V_2 + (V_{IP} - V_C)/CMRR$$

Where:

$$V_C = (V_{IPL} + V_{IPH})/2$$
$$1/CMRR = (V_3 - V_1)/(V_{IPH} - V_{IPL})$$

The remaining error (ΔV_E) is described by the Common-mode Nonlinearity spec:

EQUATION 1-8:

$$\begin{aligned} INL_{CMH} &= max(\Delta V_E)/(V_{IPH} - V_{IPL}) \\ INL_{CML} &= min(\Delta V_E)/(V_{IPH} - V_{IPL}) \\ INL_{CM} &= INL_{CMH}, \quad |INL_{CMH}| \geq |INL_{CML}| \\ &= INL_{CML}, \quad \text{otherwise} \end{aligned}$$

Where:

$$\Delta V_E = V_E - V_{E\_LIN}$$

1.6.4 DIFFERENTIAL GAIN ERROR AND NONLINEARITY

The differential errors are extracted from differential gain measurements (see **Section 1.5.2, DC Differential Gain Test Circuit**), based on Equation 1-3. These errors are then split into the differential gain error (g_E) and the input nonlinearity error INL_{DM}.

The error V_{ED} is calculated by subtracting the ideal output from V_{OUT}, then dividing by the ideal gain G_{DM}.

EQUATION 1-9:

$$V_{ED} = (V_{OUT} - (V_{REF} + G_{DM} \cdot V_{DM}))/G_{DM}$$

Figure 1-13 shows V_{ED} vs. V_{DM}, as well as a linear fit line (V_{ED_LIN}) based on V_{DM} and g_E. The amplifier is in one of the standard condition sets. The linear fit line (V_{ED_LIN}) goes through the center point (V_C, V_2) and has the same slope as the end points.

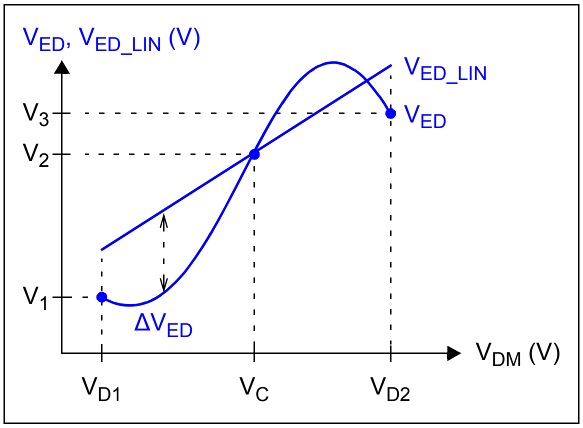


FIGURE 1-13: *Differential Input Error vs. Differential Input Voltage.*

Based on the measured V_{ED} data, we obtain the following linear fit:

EQUATION 1-10:

$$V_{ED\_LIN} = V_2 + (V_{DM} - V_C)g_E$$

Where:

$$V_C = (V_{D1} + V_{D2})/2$$
$$g_E = (V_3 - V_1)/(V_{D2} - V_{D1})$$

The remaining error (ΔV_{ED}) is described by the Differential Nonlinearity spec:

EQUATION 1-11:

$$\begin{aligned} INL_{DMH} &= max(\Delta V_{ED})/(V_{D2} - V_{D1}) \\ INL_{DML} &= min(\Delta V_{ED})/(V_{D2} - V_{D1}) \\ INL_{DM} &= INL_{DMH}, \quad |INL_{DMH}| \geq |INL_{DML}| \\ &= INL_{DML}, \quad \text{otherwise} \end{aligned}$$

Where:

$$\Delta V_{ED} = V_{ED} - V_{ED\_LIN}$$

The aging spec Δg_E is not included here, for simplicity. V_{DM} sweeps are not always centered on V_{DM} = 0V; the INL_{DM} spec will interact with the V_{OS} spec.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-9, Figure 1-10 and Figure 1-11.

2.1 DC Precision

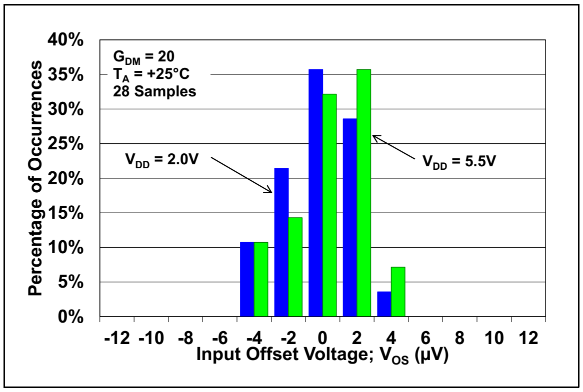


FIGURE 2-1: *Input Offset Voltage, G_{DM} = 20.*

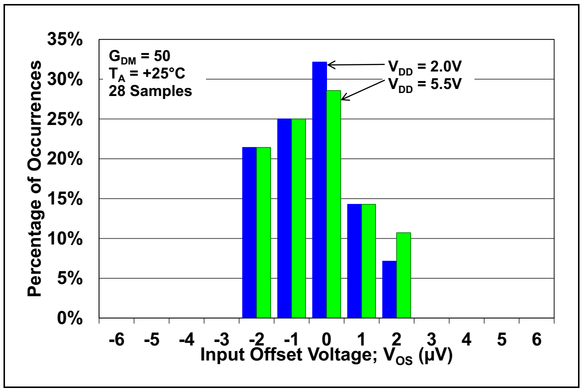


FIGURE 2-2: *Input Offset Voltage, G_{DM} = 50.*

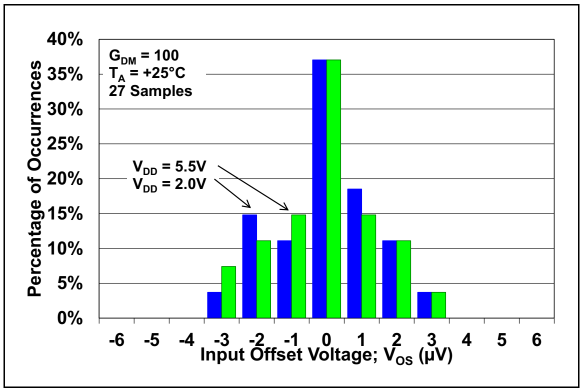


FIGURE 2-3: *Input Offset Voltage, G_{DM} = 100.*

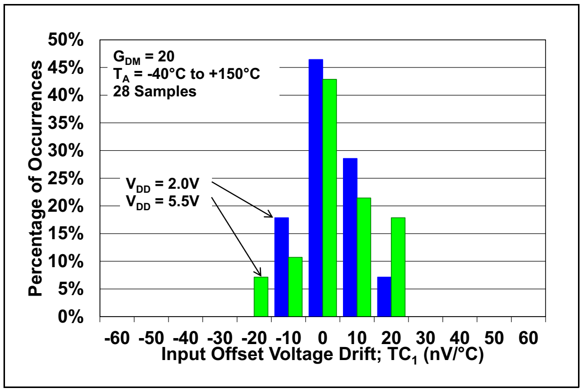


FIGURE 2-4: *Linear Input Offset Voltage Drift, G_{DM} = 20.*

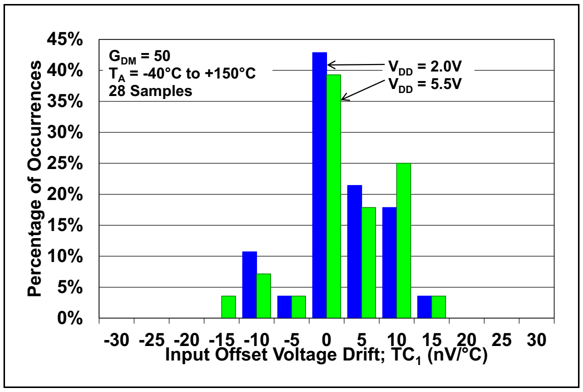


FIGURE 2-5: *Linear Input Offset Voltage Drift, G_{DM} = 50.*

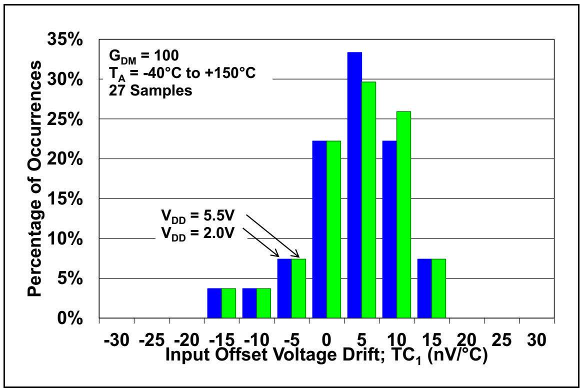


FIGURE 2-6: *Linear Input Offset Voltage Drift, G_{DM} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-9, Figure 1-10 and Figure 1-11.

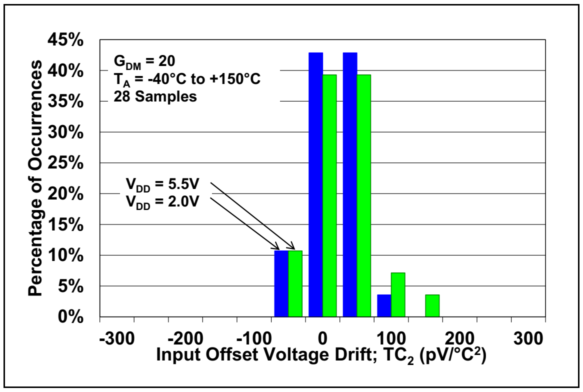


FIGURE 2-7: Quadratic Input Offset Voltage Drift, G_{DM} = 20.

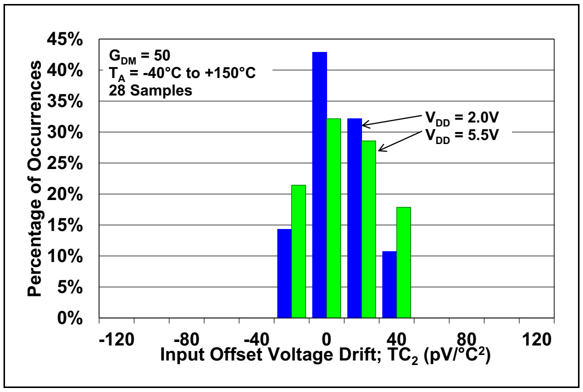


FIGURE 2-8: Quadratic Input Offset Voltage Drift, G_{DM} = 50.

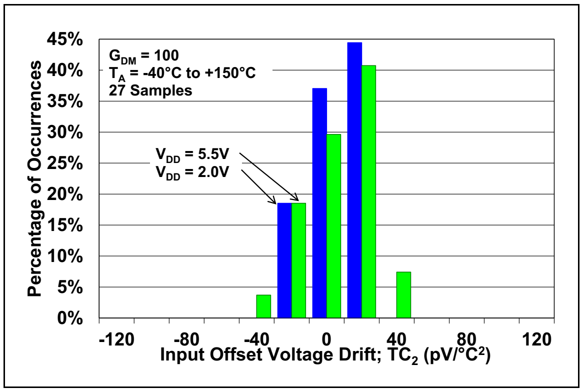


FIGURE 2-9: Quadratic Input Offset Voltage Drift, G_{DM} = 100.

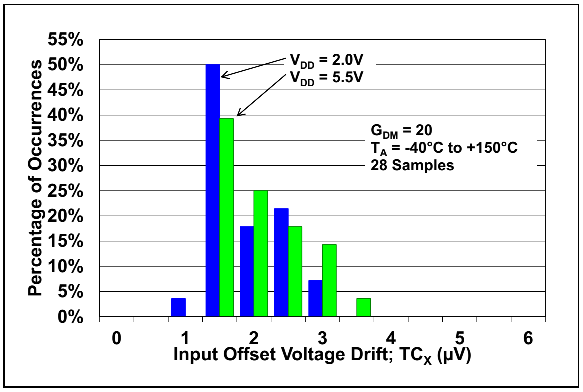


FIGURE 2-10: Exponential Input Offset Voltage Drift, G_{DM} = 20.

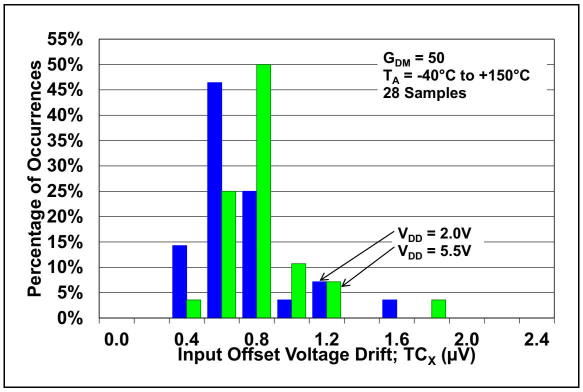


FIGURE 2-11: Exponential Input Offset Voltage Drift, G_{DM} = 50.

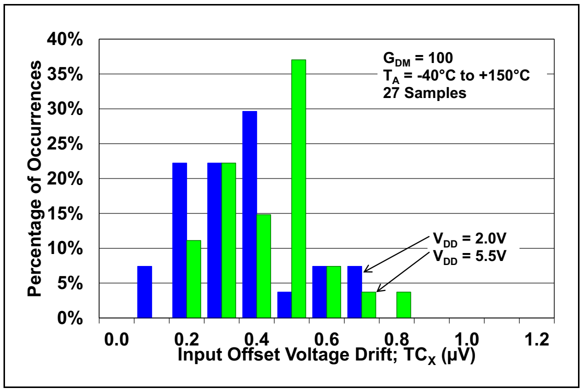


FIGURE 2-12: Exponential Input Offset Voltage Drift, G_{DM} = 100.

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

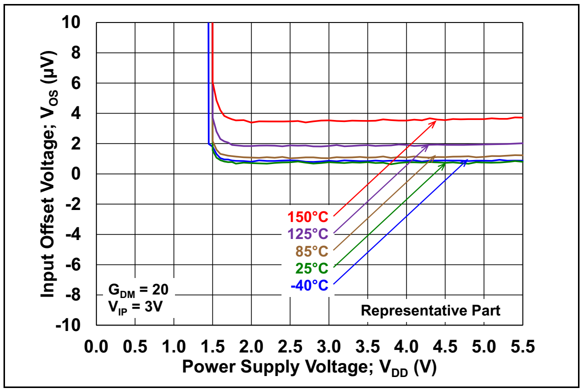


FIGURE 2-13: *Input Offset Voltage vs. Power Supply Voltage, with G_{DM} = 20.*

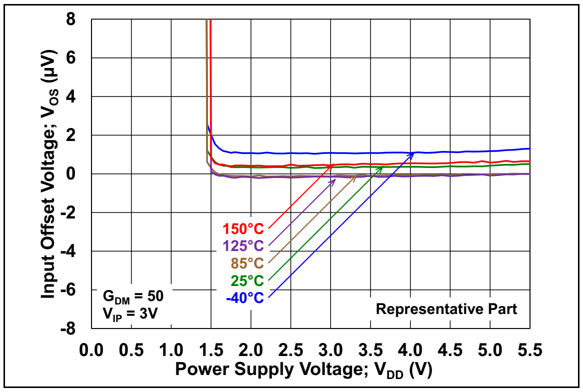


FIGURE 2-14: *Input Offset Voltage vs. Power Supply Voltage, with G_{DM} = 50.*

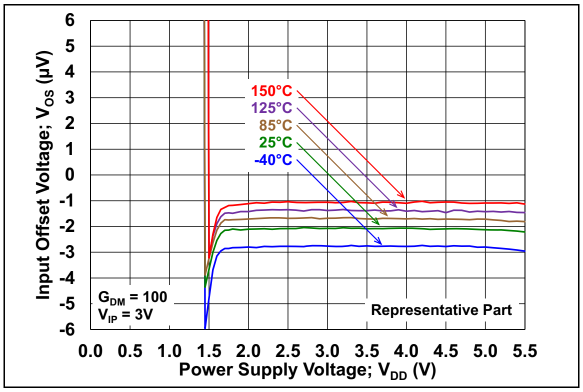


FIGURE 2-15: *Input Offset Voltage vs. Power Supply Voltage, with G_{DM} = 100.*

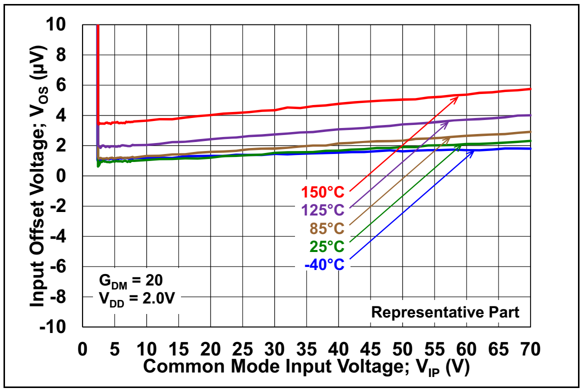


FIGURE 2-16: *Input Offset Voltage vs. Common-Mode Input Voltage, with G_{DM} = 20.*

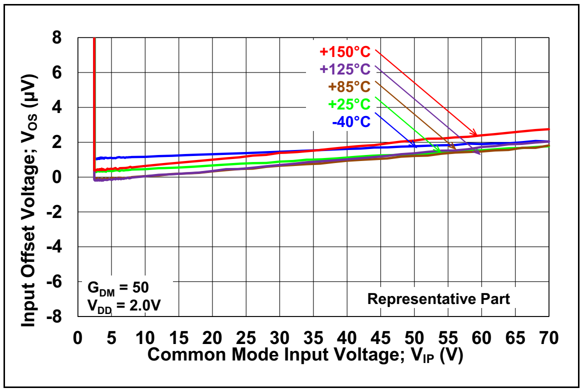


FIGURE 2-17: *Input Offset Voltage vs. Common-Mode Input Voltage, with G_{DM} = 50.*

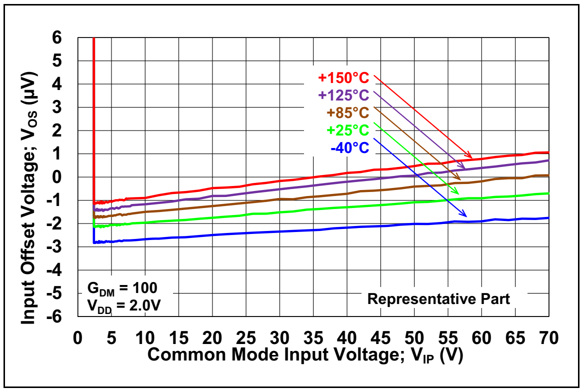


FIGURE 2-18: *Input Offset Voltage vs. Common-Mode Input Voltage, with G_{DM} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-9, Figure 1-10 and Figure 1-11.

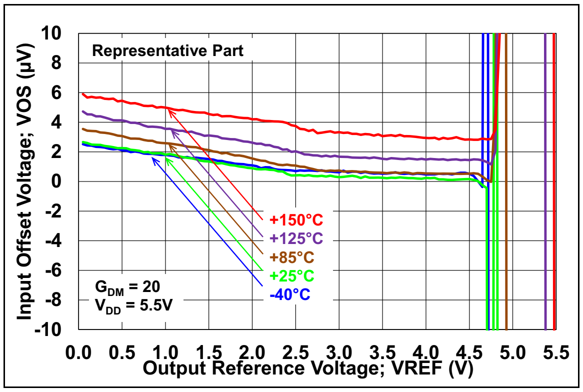


FIGURE 2-19: *Input Offset Voltage vs. Reference Voltage, with G_{DM} = 20.*

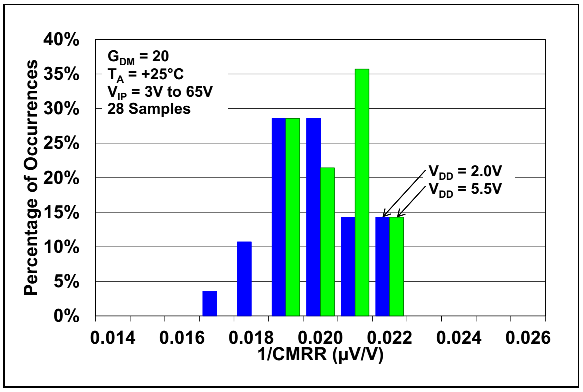


FIGURE 2-22: *1/CMRR, with G_{DM} = 20.*

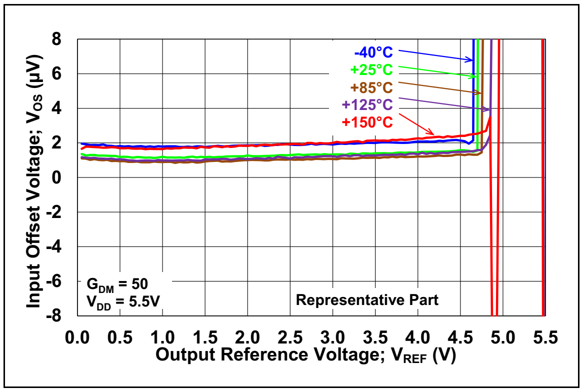


FIGURE 2-20: *Input Offset Voltage vs. Reference Voltage, with G_{DM} = 50.*

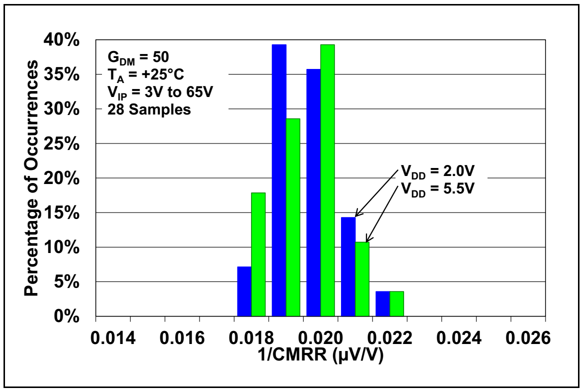


FIGURE 2-23: *1/CMRR, with G_{DM} = 50.*

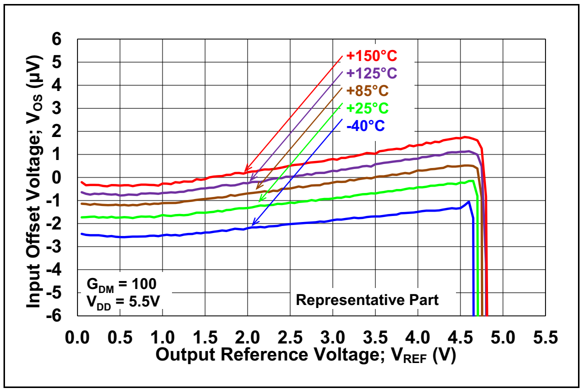


FIGURE 2-21: *Input Offset Voltage vs. Reference Voltage, with G_{DM} = 100.*

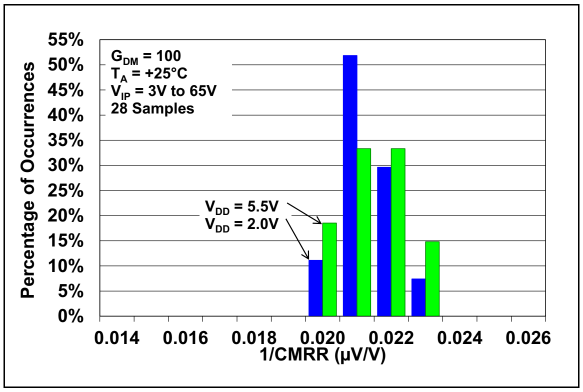


FIGURE 2-24: *1/CMRR, with G_{DM} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-9, Figure 1-10 and Figure 1-11.

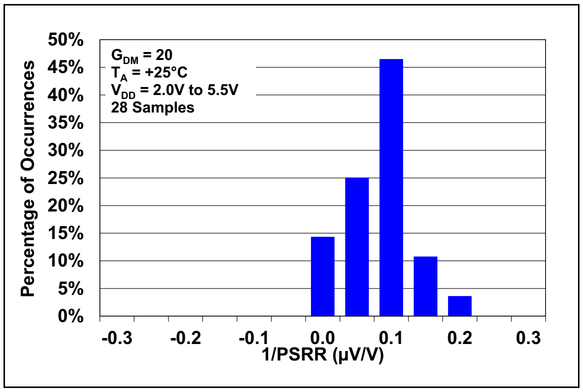


FIGURE 2-25: *1/PSRR, with G_{DM} = 20.*

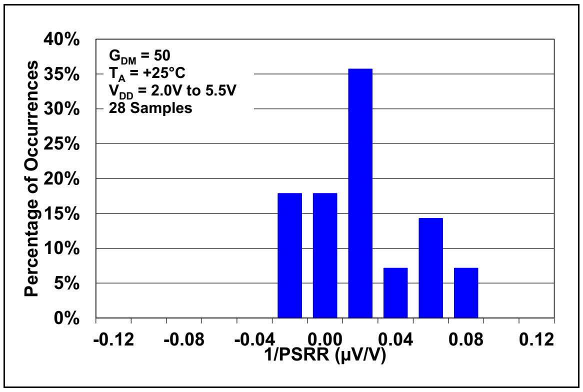


FIGURE 2-26: *1/PSRR, with G_{DM} = 50.*

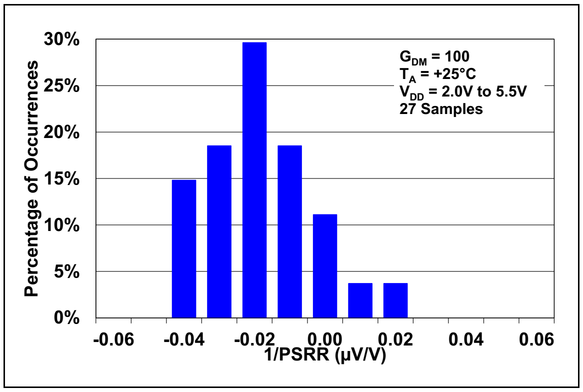


FIGURE 2-27: *1/PSRR, with G_{DM} = 100.*

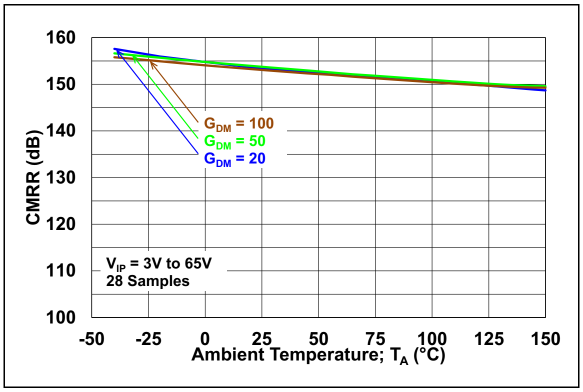


FIGURE 2-28: *CMRR vs. Ambient Temperature.*

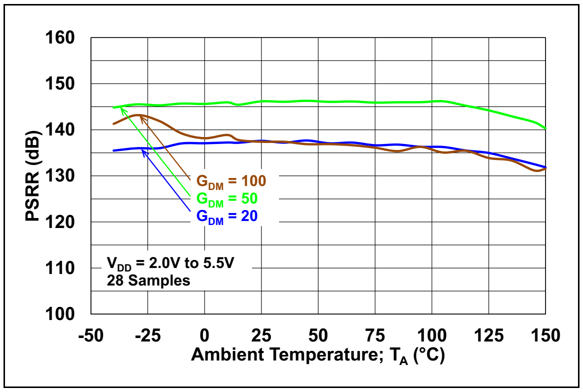


FIGURE 2-29: *PSRR vs. Ambient Temperature.*

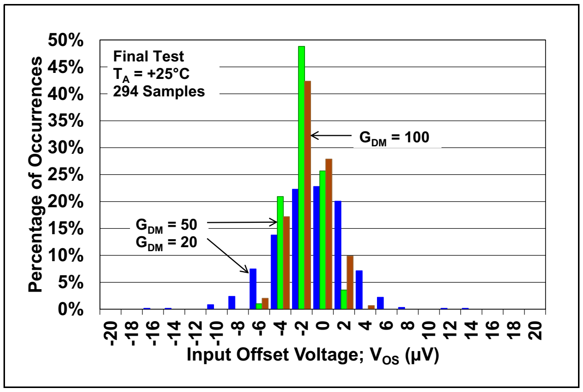


FIGURE 2-30: *Input Offset Voltage - Final Test Results.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, V_{REF} = V_{DD}/4, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF; see Figure 1-9, Figure 1-10 and Figure 1-11.

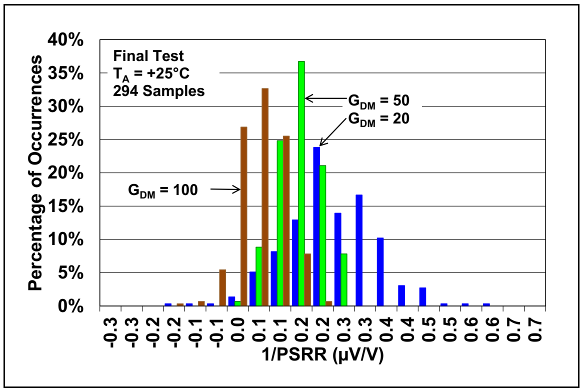


FIGURE 2-31: *PSRR - Final Test Results.*

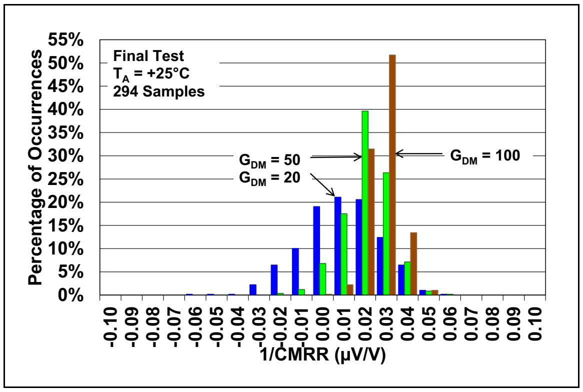


FIGURE 2-32: *CMRR - Final Test Results.*

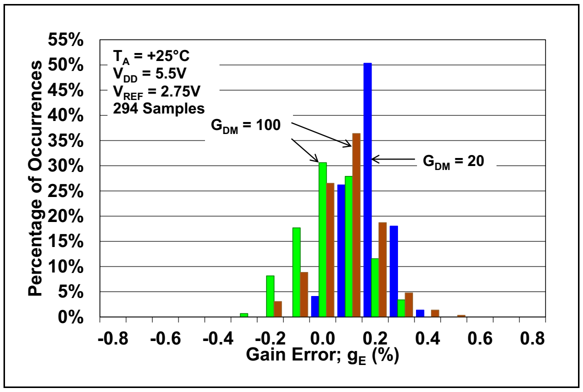


FIGURE 2-33: *Gain Error.*

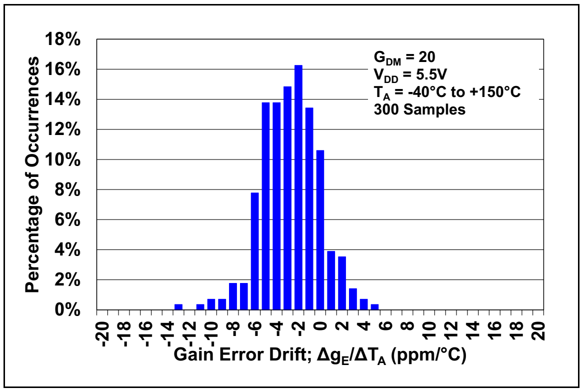


FIGURE 2-34: *Gain Error Temperature Drift.*

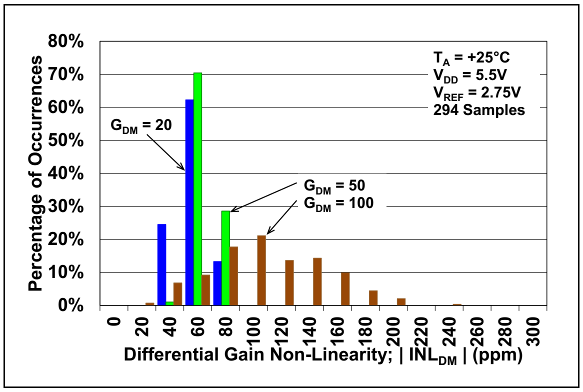


FIGURE 2-35: *Differential Gain Nonlinearity.*

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

2.2 Other DC Voltages and Currents

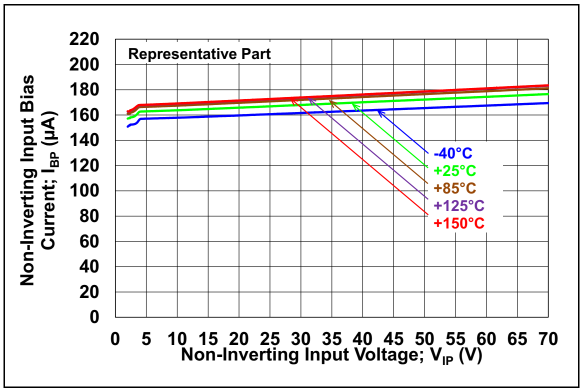


FIGURE 2-36: *V_{IP} Pin Input Bias Current vs. Input Common-Mode Voltage.*

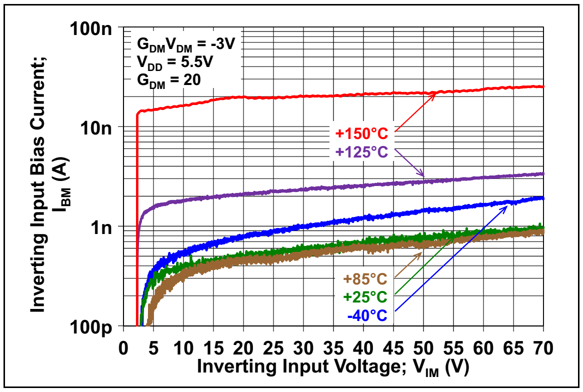


FIGURE 2-37: *V_{IM} Pin Input Bias Current vs. Input Common-Mode Voltage, $V_{DM} = V_{DML}$.*

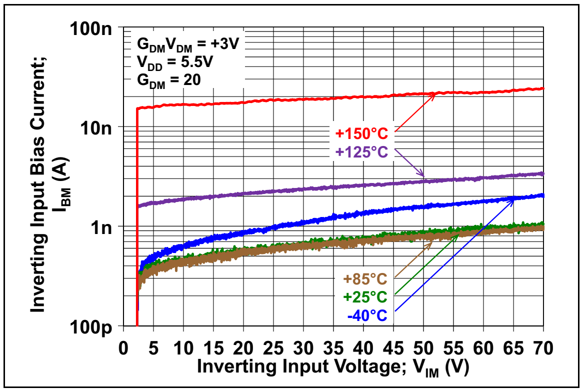


FIGURE 2-38: *V_{IM} Pin Input Bias Current vs. Input Common-Mode Voltage, $V_{DM} = V_{DMH}$.*

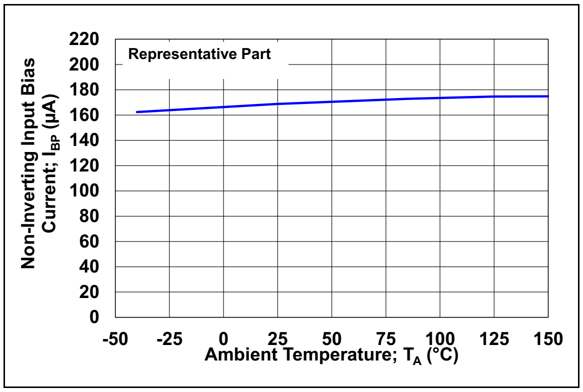


FIGURE 2-39: *V_{IP} Pin Input Bias Current vs. Ambient Temperature.*

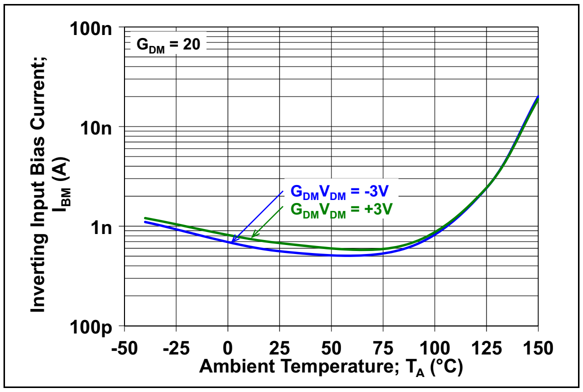


FIGURE 2-40: *V_{IM} Pin Input Bias Current vs. Ambient Temperature.*

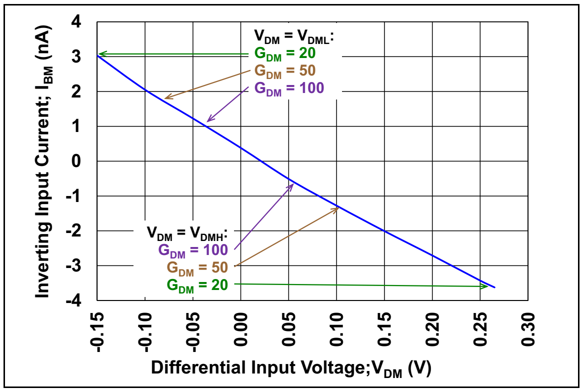


FIGURE 2-41: *V_{IM} Pin Input Bias Current vs. Differential Input Voltage.*

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

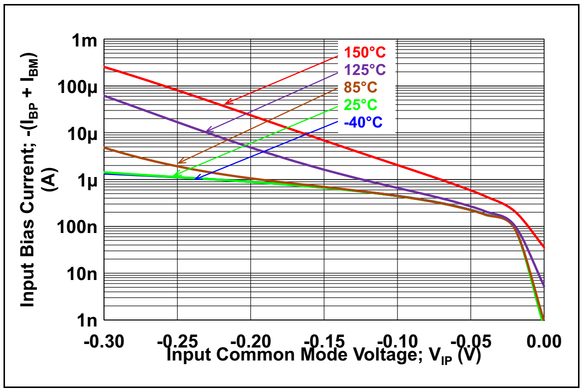


FIGURE 2-42: Input Bias Current vs. Input Common-Mode Voltage (below V_{SS}).

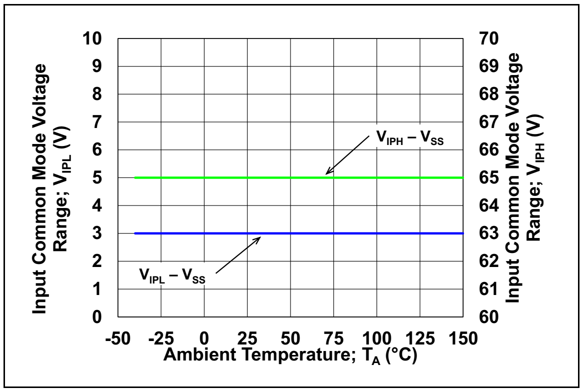


FIGURE 2-43: Common-Mode Input Range vs. Ambient Temperature.

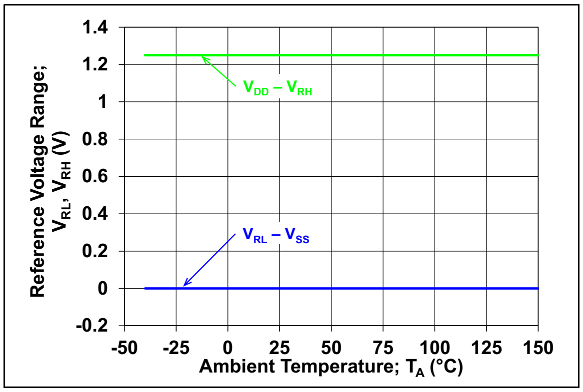


FIGURE 2-44: Reference Voltage Range vs. Ambient Temperature.

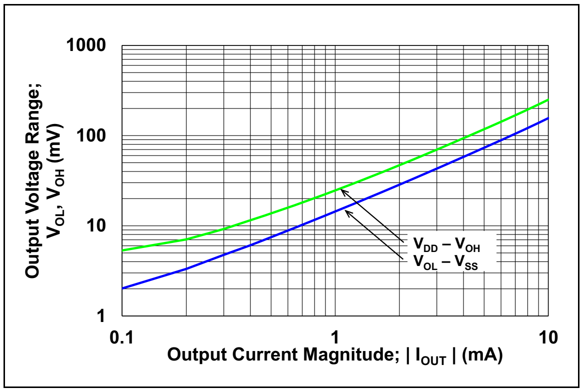


FIGURE 2-45: Output Voltage Range vs. Output Current.

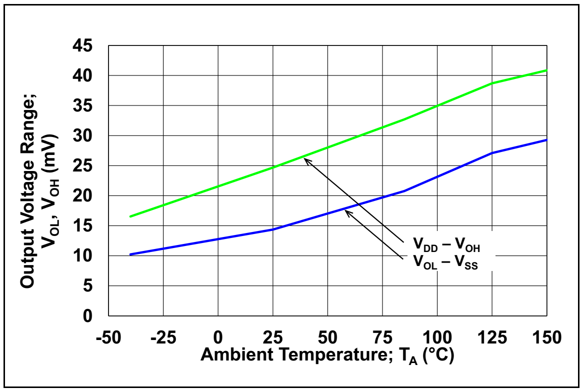


FIGURE 2-46: Output Voltage Range vs. Ambient Temperature.

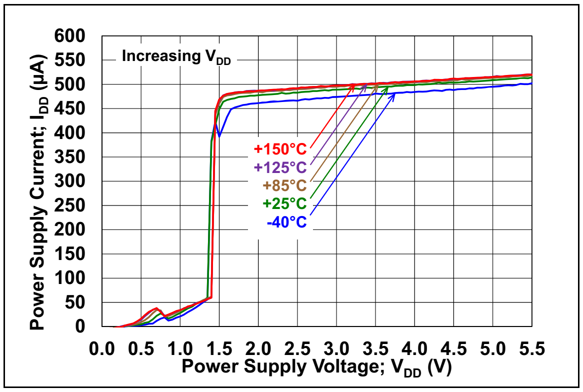


FIGURE 2-47: Supply Current vs. Power Supply Voltage.

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

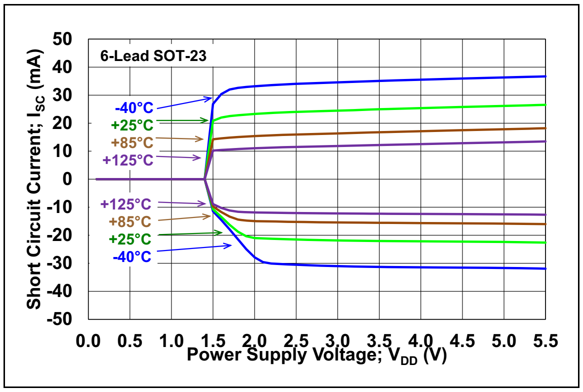


FIGURE 2-48: Output Short Circuit Current vs. Power Supply Voltage for E-Temp Parts.

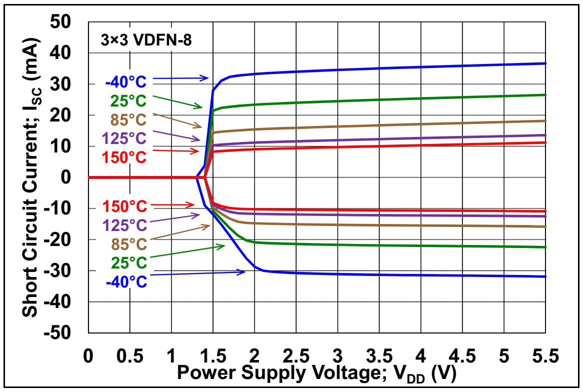


FIGURE 2-49: Output Short Circuit Current vs. Power Supply Voltage for H-Temp Parts.

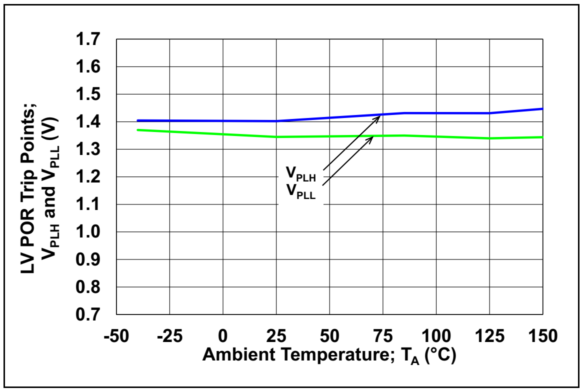


FIGURE 2-50: LV POR (for V_{DD}) Trip Points vs. Ambient Temperature.

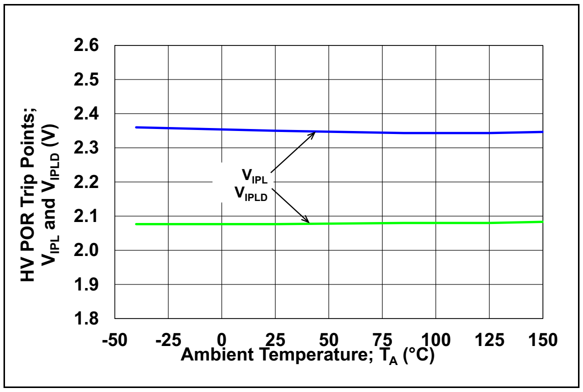


FIGURE 2-51: HV POR (for V_{IP}) Trip Points vs. Ambient Temperature.

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

2.3 Frequency Response

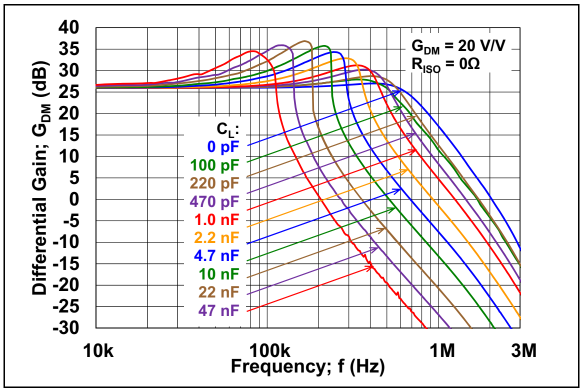


FIGURE 2-52: *Gain vs. Frequency, with Capacitive Load.*

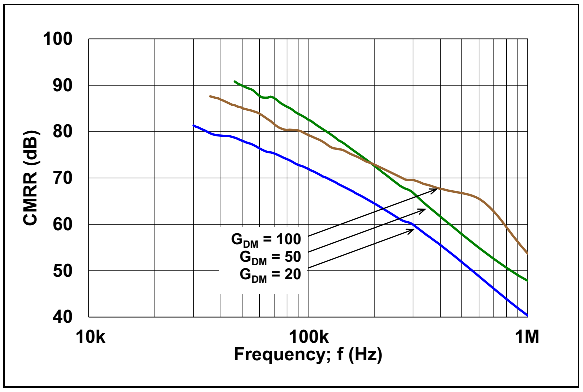


FIGURE 2-53: *CMRR vs. Frequency.*

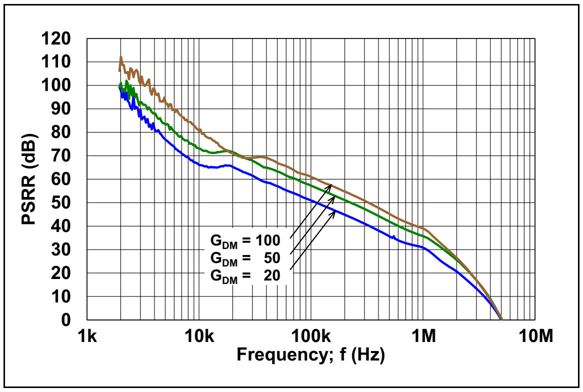


FIGURE 2-54: *PSRR vs. Frequency.*

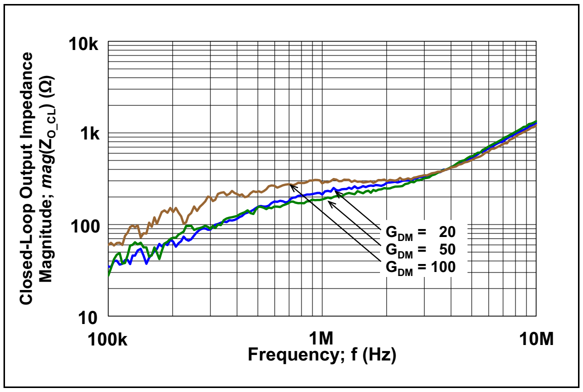


FIGURE 2-55: *Closed-Loop Output Impedance Magnitude vs. Frequency.*

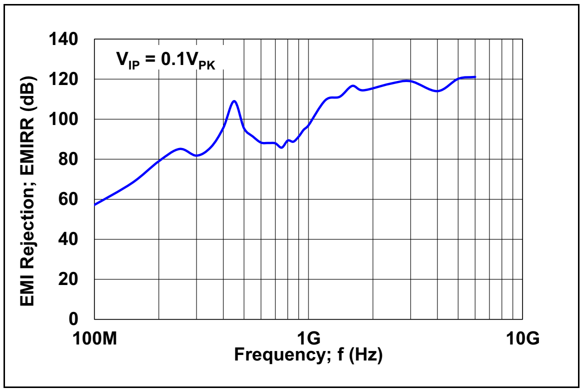


FIGURE 2-56: *EMI Rejection Ratio vs. Frequency.*

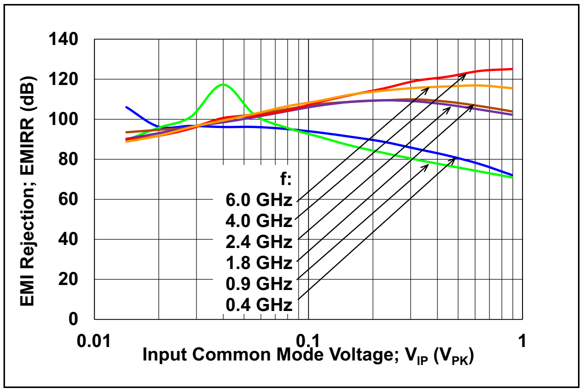


FIGURE 2-57: *EMI Rejection Ratio vs. Signal Strength.*

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

2.4 Noise and Intermodulation Distortion

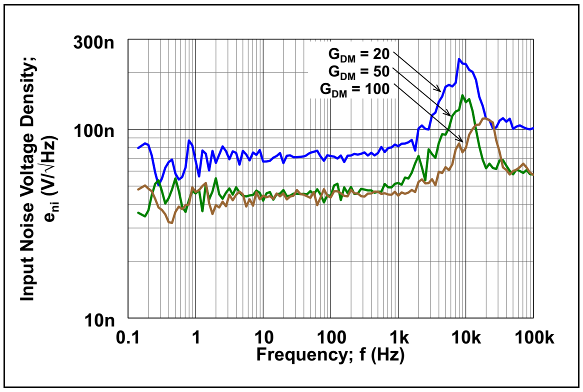


FIGURE 2-58: *Input Noise Voltage Density vs. Frequency.*

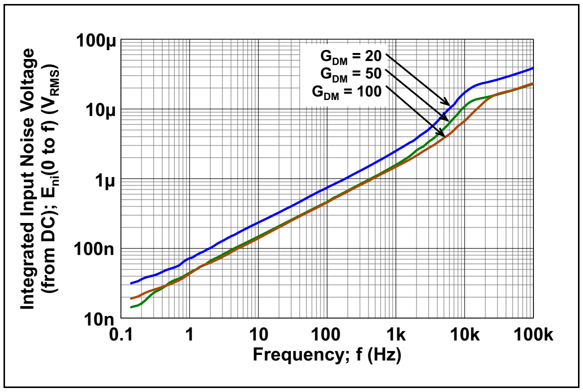


FIGURE 2-59: *Input Noise Voltage vs. Frequency.*

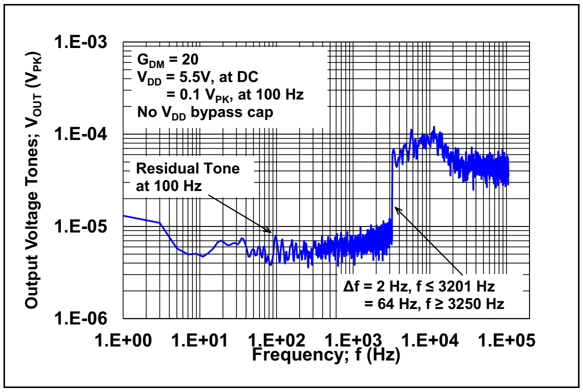


FIGURE 2-60: *Intermodulation Distortion vs. Frequency, with V_{DD} Disturbance.*

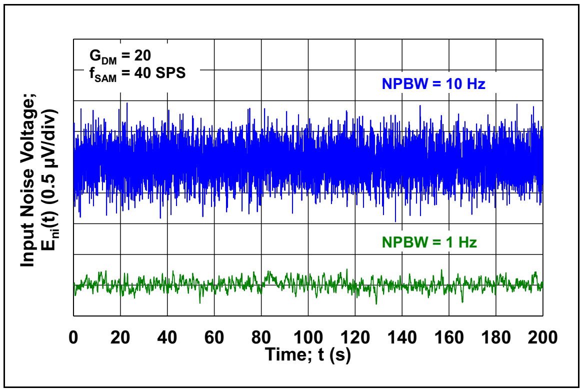


FIGURE 2-61: *Input Noise Voltage vs. Time, G_{DM} = 20.*

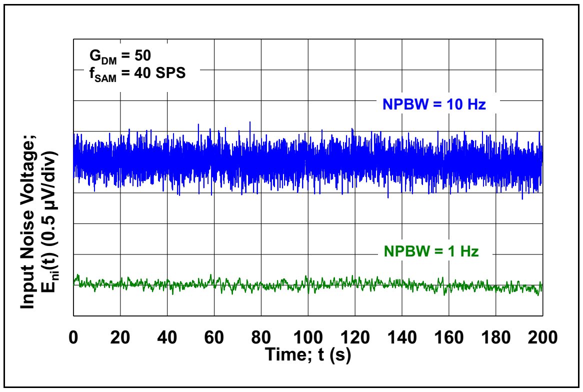


FIGURE 2-62: *Input Noise Voltage vs. Time, G_{DM} = 50.*

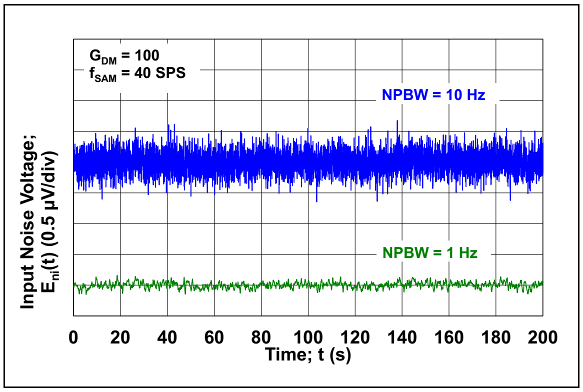


FIGURE 2-63: *Input Noise Voltage vs. Time, G_{DM} = 100.*

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

2.5 Time Response

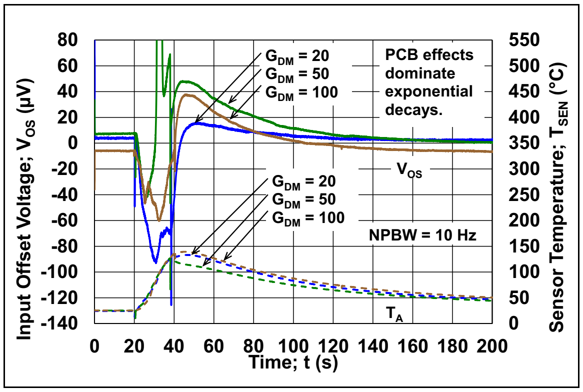


FIGURE 2-64: Input Offset Voltage vs. Time, with Temperature Change.

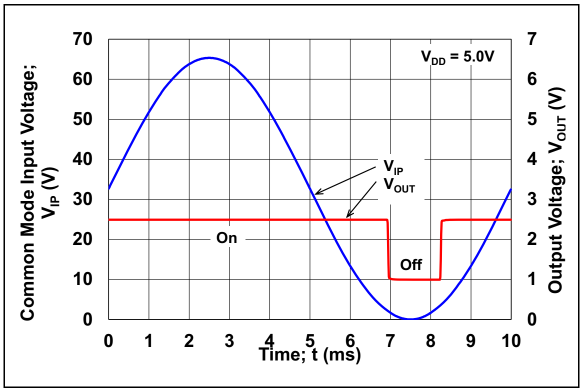


FIGURE 2-67: The MCP6C02 Shows No Phase Reversal vs. Input Common-Mode Overdrive.

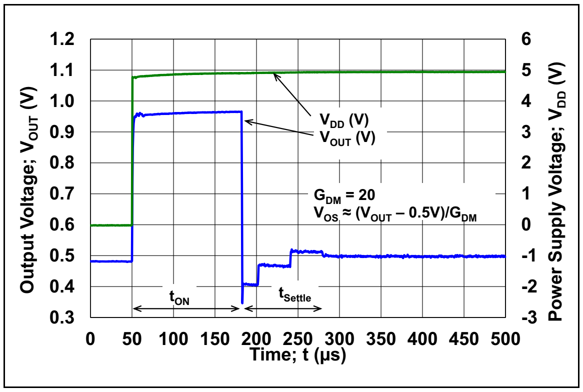


FIGURE 2-65: Input Offset Voltage vs. Time, at Power-Up.

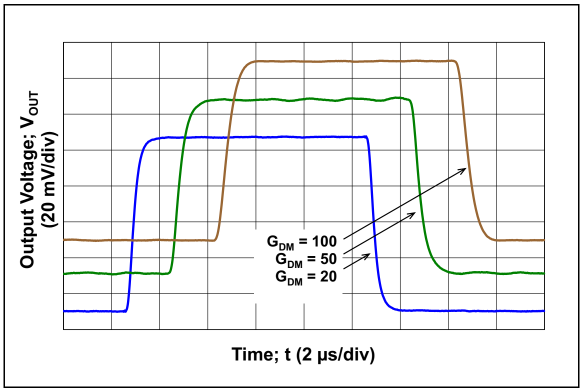


FIGURE 2-68: Small Signal Step Response to Differential Input Voltage.

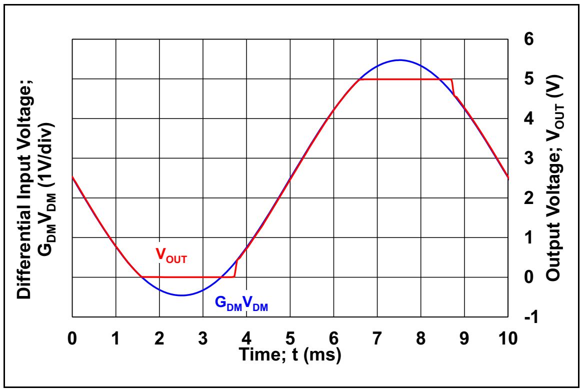


FIGURE 2-66: The MCP6C02 Shows No Phase Reversal vs. Differential Input Overdrive.

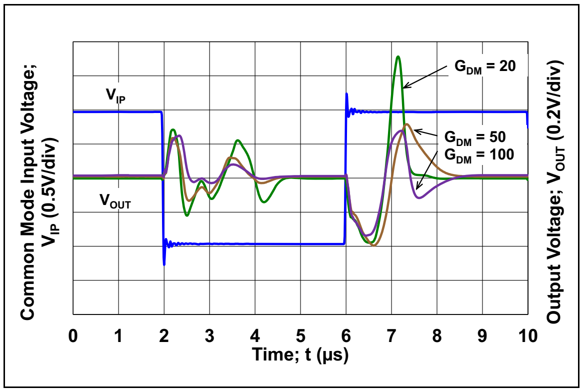


FIGURE 2-69: Small Signal Step Response to Common-Mode Input Voltage.

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 2.0V$ to $5.5V$, $V_{SS} = GND$, $V_{IP} = 34V$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$; see Figure 1-9, Figure 1-10 and Figure 1-11.

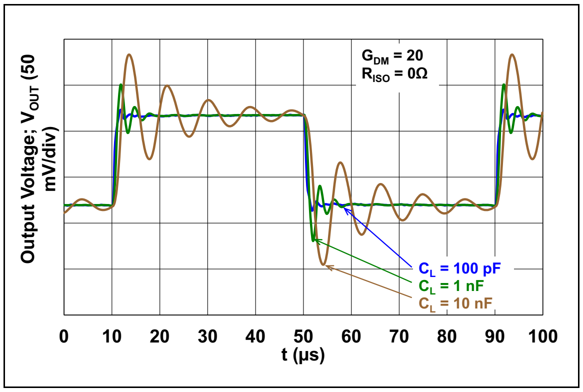


FIGURE 2-70: Small Signal Step Response to Differential Input Voltage, with Capacitive Load (C_L).

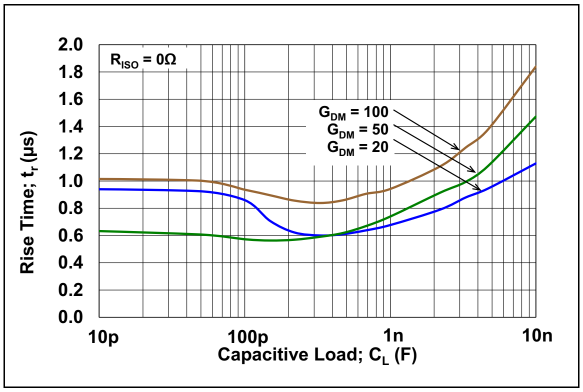


FIGURE 2-72: Small Signal Step Response Rise Time, with Capacitive Load (C_L).

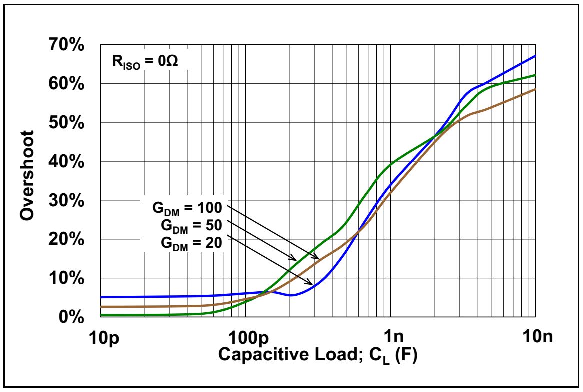


FIGURE 2-71: Small Signal Step Response Overshoot, with Capacitive Load (C_L).

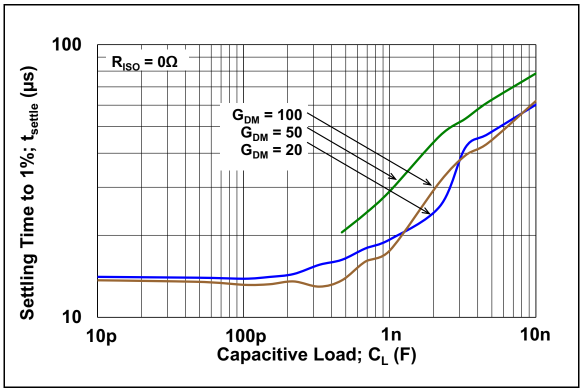


FIGURE 2-73: Small Signal Step Response Settling Time, with Capacitive Load (C_L).

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6C02		Sym.	Description
SOT-23	3×3 VDFN		
1	5	V_{OUT}	Output voltage
2	2	V_{SS}	Negative power supply
3	1	V_{IP}	Noninverting input (at load's R_{SH}) and positive (high-side) power supply
4	8	V_{IM}	Inverting input (at load's R_{SH})
5	7	V_{REF}	Output reference
6	6	V_{DD}	Positive (low-side) power supply
—	3,4	NC	No connection
—	9	EP	Exposed thermal pad; must be connected to V_{SS}

Note 1: The SOT package is for E-temp and the VDFN package is for H-temp.

3.1 Noninverting Analog Signal Input (V_{IP})

The noninverting input (V_{IP}) is a high-impedance CMOS input. It is designed to operate over a wide voltage range, with a voltage source to drive it. In this data sheet, it is treated as the Common-mode input voltage.

V_{IP} is the high voltage power supply pin, and is normally between V_{SS} + 3V and V_{SS} + 65V. It supplies the current needed to operate the high voltage circuitry. V_{IP} needs a good bypass capacitor (e.g., 10 nF). $V_{IP} – V_{SS}$ triggers the HV POR.

The edge rate applied to V_{IP} ($\Delta V_{IP}/\Delta t$) needs to be limited, so the ESD diodes do not clamp.

V_{IP} is treated as the common mode voltage in this data sheet, due to the inputs' architecture. Since V_{DM} is relatively small, this simplification is accurate; it also simplifies the specifications and applications information.

3.2 Inverting Analog Signal Input (V_{IM})

The inverting input (V_{IM}) is a high-impedance CMOS input, with low input bias current. V_{IM} is designed to operate near the V_{IP} voltage. The difference voltage V_{DM} (or $V_{IP} – V_{IM}$) is the input signal for this amplifier.

3.3 Analog Output Reference Voltage (V_{REF})

The analog output reference voltage is a high-impedance CMOS input. V_{REF} is set to a DC voltage, which shifts V_{OUT}. Its dynamic response helps reject power surges and glitches at the V_{IP}, V_{DD} and V_{SS} pins.

3.4 Analog Output (V_{OUT})

The analog output pin (V_{OUT}) is a low-impedance voltage source.

3.5 Low-Side Power Supplies (V_{DD}, V_{SS})

V_{DD} is normally between V_{SS} + 2.0V and V_{SS} + 5.5V, while the V_{REF} and V_{OUT} pins are usually between V_{SS} and V_{DD}. $V_{DD} – V_{SS}$ triggers the LV POR.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need good bypass capacitors.

In split supply configurations, including dual supplies, ground is between V_{SS} and V_{DD}. Both supply pins will need good bypass capacitors.

In a single (negative) supply configuration, V_{DD} connects to ground and V_{SS} connects to the supply. V_{SS} will need good bypass capacitors.

3.6 Exposed Pad (EP)

The Exposed Thermal Pad (EP) connects internally to the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

NOTES:

4.0 DEVICE OPERATION

This chapter includes additional information on basic operations and major functions.

4.1 Basic Performance

4.1.1 IDEAL PERFORMANCE

Figure 4-1 shows the basic circuit; inputs, supplies and output. When the inputs (V_{IP}, V_{IM}, V_{DD}, V_{SS} and V_{REF}) and output (V_{OUT}) are in their specified ranges, and the part is nearly ideal, the output voltage is:

EQUATION 4-1:

$$V_{OUT} \approx V_{REF} + G_{DM} V_{DM}$$

Where:

G_{DM} = Differential-Mode Gain

V_{REF} = Output Reference Voltage

V_{DM} = Differential-Mode Input ($V_{IP} - V_{IM}$)

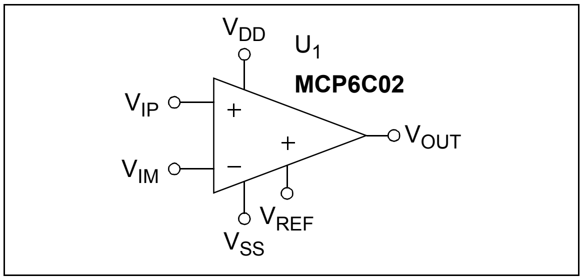


FIGURE 4-1: *Basic Circuit.*

For normal operation, keep:

- V_{IP} between V_{IPL} and V_{IPH}
- V_{DM} between V_{DML} and V_{DMH}
- V_{REF} between V_{RL} and V_{RH}
- V_{OUT} between 0.1V to V_{DD} – 0.1V, usually
  - V_{OL} and V_{OH} are hard limits

4.1.2 ANALOG ARCHITECTURE

Figure 4-2 shows the block diagram for these high-side current sense amplifiers, without any details on offset correction.

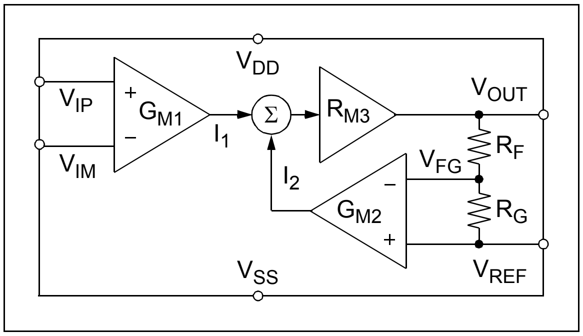


FIGURE 4-2: *MCP6C02 Block Diagram.*

The input (differential) signal is applied to G_{M1}. Due to its architecture, the MCP6C02's signal inputs are best described by V_{IP} and V_{DM}. The inverting input is then:

EQUATION 4-2:

$$V_{IM} = V_{IP} - V_{DM}$$

The negative feedback loop includes G_{M2}, R_{M3}, R_F and R_G. These blocks set the DC open-loop gain (A_{OL}) and the nominal differential gain (G_{DM}):

EQUATION 4-3:

$$A_{OL} = G_{M2} R_{M3}$$
$$G_{DM} = 1 + R_F / R_G$$

A_{OL} is very high, so the current into R_{M3} ($I_1 + I_2$) is nearly zero. This makes the differential inputs to G_{M1} and G_{M2} equal in magnitude and opposite in polarity. Ideally, this gives:

EQUATION 4-4:

$$V_{FG} - V_{REF} = V_{DM}$$
$$V_{OUT} = V_{REF} + G_{DM} V_{DM}$$

For an ideal part, within the operating ranges, changing V_{IP}, V_{SS} or V_{DD} produces no change in V_{OUT}. V_{REF} shifts V_{OUT} as needed in the design.

The different G_{DM} options change G_{M1}, G_{M2}, R_F, R_G and the internal compensation capacitor. This results in the performance trade-offs highlighted in Table 1.

4.1.3 DC PERFORMANCE

4.1.3.1 DC Voltage Errors

Section 1.6, Explanation of DC Error Specifications covers some DC specifications. The input offset error (with temperature coefficients), gain error and nonlinearities are discussed in detail.

Plots in **Section 2.1, DC Precision** and **Section 2.2, Other DC Voltages and Currents** give useful information.

In this data sheet, CMRR is based on changes in V_{IP} (i.e., CMRR = $\Delta V_{IP}/\Delta V_{OS}$); this is accurate, since V_{DM} is relatively small. This CMRR describes the rejection of errors at the high voltage supply, without any contribution from V_{DM}.

4.1.3.2 DC Current Errors

Figure 4-3 shows the resistors and currents that change the DC bias point. The input bias currents (I_{BP}, I_{BM} and I_{BR}), together with a circuit's external input resistances, give an DC error (see Equation 1-2).

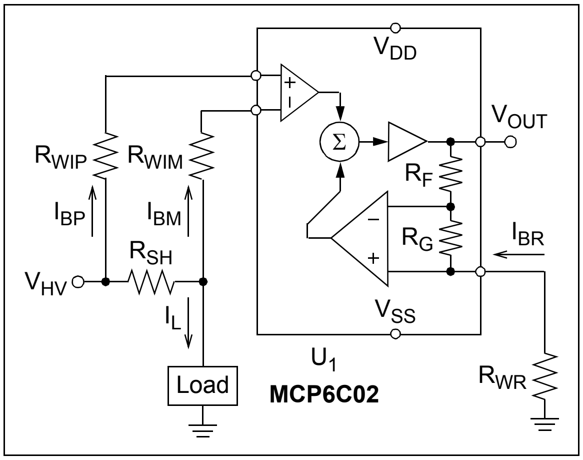


FIGURE 4-3: *DC Bias Resistors and Currents.*

R_{SH} is set by the design requirements, given the load current (I_L). For most applications, R_{SH} would be between 100 µΩ and 1Ω.

The DC input offset error due to the input currents is:

$$\begin{aligned} V_{OS\_IR} &= V_{DM} - I_L R_{SH} \\ &= I_{BM}(R_{SH} + R_{WIM}) - I_{BP}R_{WIP} \end{aligned}$$

Since these currents do not correlate, minimize the magnitude of each resistance. $I_{BP}R_{IP}$ will dominate in many designs.

R_{WR} modifies the gain error and the DC output offset error (V_{OUT} changes I_{BR}):

EQUATION 4-5:

$$\begin{aligned} \Delta V_{REF} &= -I_{BR}R_{WR} \\ \Delta g_E &\approx (-R_{WR}G_{DM})/(R_F + R_G) \\ V_{OUT} &\approx (V_{REF} + \Delta V_{REF}) + G_{DM}V_{DM}(1 + g_E + \Delta g_E) \end{aligned}$$

4.1.4 AC PERFORMANCE

The bandwidth of these parts (f_{BW}) is set internally to either 500 kHz ($G_{DM} = 20$ or 50) or 390 kHz ($G_{DM} = 100$).

The large signal bandwidth is close to the small signal bandwidth; slew rate (SR) has little effect on V_{OUT} (a benefit of our current-mode architecture).

The bandwidth at the maximum output swing is called the Full Power Bandwidth (f_{FPBW}). It is limited by the Slew Rate (SR) for many amplifiers, but is close to f_{BW} for these parts. This is a benefit of the current-mode architecture these parts have.

These parts are compensated to have a stable response. For instance, step response overshoot is low.

In this data sheet, the AC CMRR is measured at V_{IP}; this is accurate, since V_{DM} is relatively small.

4.1.5 TEMPERATURE PERFORMANCE

The input offset voltage's temperature drift is detailed in Equation 1-6. Other temperature responses are shown in **Section 1.3, Specifications** and **Section 2.0 "Typical Performance Curves"**.

Since there are three power supply pins (V_{IP}, V_{DD} and V_{SS}), and V_{IP} reaches 65V, power and temperature rise calculations are important.

The power dissipated is calculated as follows (I_{OUT} is positive when it flows out of the V_{OUT} pin):

EQUATION 4-6:

$$P_{TOT} = P_{DD} + P_{BP} + P_{OUT}$$

Where:

$I_{OUT} = (V_{OUT} - V_L)/R_L$
$P_{DD} = (V_{DD} - V_{SS})\, I_{DD}$
$P_{BP} = (V_{IP} - V_{SS})\, I_{BP}$
$P_{OUT} = (V_{DD} - V_{OUT})\, I_{OUT}, \; I_{OUT} \geq 0A$
$= (V_{SS} - V_{OUT})\, I_{OUT}, \; I_{OUT} < 0A$

Now we can estimate the junction temperature of the device (see Table 1-4):

EQUATION 4-7:

$$T_J = T_A + P_{TOT}\theta_{JA}$$

4.1.6 NOISE PERFORMANCE

This part is designed to have low input noise voltage density at lower frequencies. The offset correction (**Section 4.2.2, Chopping Action**) modulates high frequency white noise down to DC; it also modulates low frequency 1/f noise to higher frequencies.

The measured input noise voltage density is shown in Figure 2-58. That figure also shows Integrated Input Noise Voltage (E_{ni}, in units of V_{RMS}) between 0 Hz and f (between 0.1 Hz and 100 kHz).

The Input Noise Voltage Density (e_{ni}) changes with V_{DM}. However, that relationship is a weak one.

4.2 Overview of Zero-Drift Operation

Figure 4-4 shows a diagram of the MCP6C02; It explains how slow voltage errors at the input are reduced in this architecture (much better V_{OS}, TC_1 TC_2, CMRR, CMRR2, PSRR and 1/f noise).

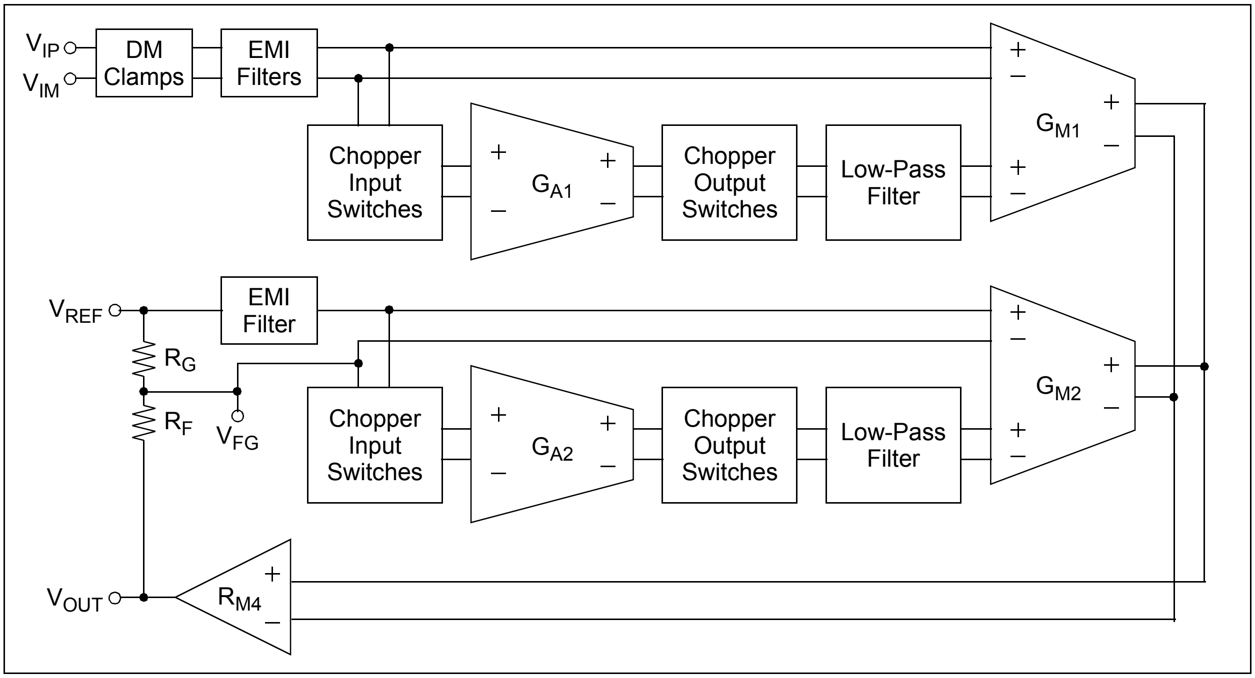


FIGURE 4-4: *MCP6C02 Block Diagram.*

4.2.1 BUILDING BLOCKS

The Main Amplifiers (G_{M1} and G_{M2}) are designed for high gain and bandwidth, with a differential topology. The main input pairs (+ and - pins at the top left) are for the higher frequency portion of the input signal. The auxiliary input pairs (+ and - pins at the bottom left) are for the low frequency and high precision portion of the input signal and correct the input offset voltage. Both inputs are added together internally.

The Auxiliary Amplifiers (G_{A1} and G_{A2}), the Chopper Input Switches and the Chopper Output Switches provide a high DC gain to the input signal. DC errors are modulated to higher frequencies and white noise to low frequencies.

The Low-Pass Filter reduces high-frequency content, including harmonics of the Chopping Clock.

The Output Buffer (R_{M4}) converts current to voltage, drives the external load at V_{OUT} and creates a negative feedback loop through R_F and R_G. R_F and R_G help set the differential gain.

The Oscillator runs at f_{CLK} = 50 kHz for the gains of 20 and 50, and at f_{CLK} = 100 kHz for the gain of 100. f_{CLK} is divided by 2, to produce the Chopping Clock rate (25 kHz and 50 kHz, respectively).

The internal LV POR (for $V_{DD} – V_{SS}$) starts the part in a known good state, protecting against power supply brown-outs. The internal HV POR (for $V_{IP} – V_{SS}$) ensures protection of the low voltage circuitry, as well as proper functioning.

4.2.2 CHOPPING ACTION

Figure 4-5 shows the amplifier connections for the first phase of the Chopping Clock and Figure 4-6 shows them for the second phase. The slow voltage errors alternate in polarity, making the average error small.

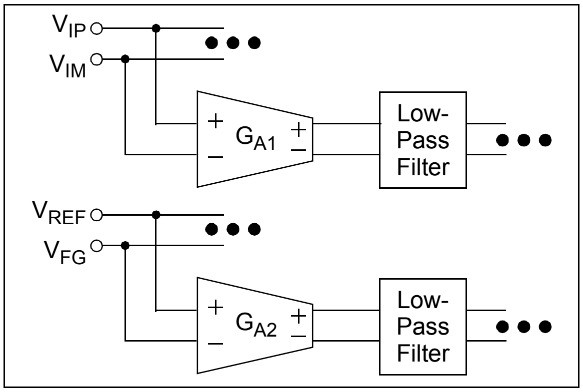


FIGURE 4-5: *First Chopping Clock Phase; Simplified Diagram.*

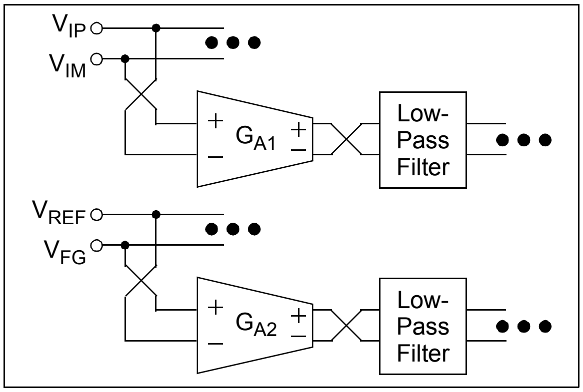


FIGURE 4-6: Second Chopping Clock Phase; Simplified Diagram.

4.2.3 FINAL TEST VS. BENCH

Due to limitations in the final test environment (e.g., equipment accuracies, thermocouple effects crosstalk and test time), final test measurements are not as accurate as bench measurements. For this reason, the input offset voltage related specifications (V_{OS}, TC_1, TC_2, ..., CMRR and PSRR) are significantly wider than the histograms from bench measurements.

The bench results will give good guidance on how to design your circuit. The specified limits (for final test) give min/max limits used to screen outliers in production.

4.2.4 INTERMODULATION DISTORTION (IMD)

These amplifiers will show intermodulation distortion (IMD) products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the zero-drift circuitry's nonlinear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock's harmonics has a series of IMD tones centered on it.

4.3 Protection

The MCP6C02 helps the designer provide enough protection against undesired conditions and signals in their environment.

4.3.1 INTERNAL PROTECTION DEVICES

All of the ESD structures clamp their inputs when they try to go too far below V_{SS}. Their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.

The supply inputs ($V_{IP} – V_{SS}$ and $V_{DD} – V_{SS}$) are also connected to PORs, so that internal power up sequencing is well controlled.

The V_{IP} and V_{IM} input pins have an ESD structure designed to limit $V_{IP} – V_{SS}$ and V_{DM}. The double parallel diode structure that limits ESD damage through V_{DM} also limits V_{DM} in other conditions.

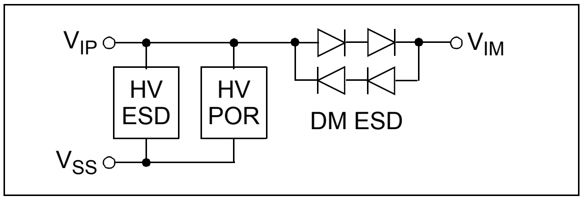


FIGURE 4-7: Input Protection for V_{DM} (i.e., for V_{IM}) and $V_{IP} – V_{SS}$.

The V_{REF}, V_{OUT} and V_{DD} pins have ESD structures that limit their voltages above V_{SS} (i.e., limit $V_{REF} – V_{SS}$, $V_{OUT} – V_{SS}$ and $V_{DD} – V_{SS}$).

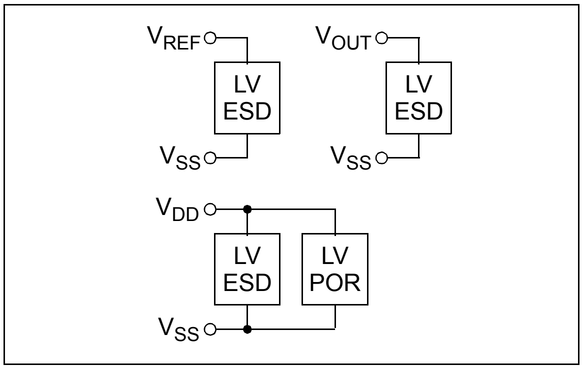


FIGURE 4-8: Input Protection for V_{REF}, V_{OUT} and V_{DD}.

4.3.2 PHASE REVERSAL

This part is designed to not exhibit phase inversion when the input signals (V_{IP}, V_{DM} and V_{REF}) exceed their specified ranges (but not their absolute ranges).

5.0 APPLICATIONS

This chapter includes design recommendations and typical application circuits.

The Common-mode rejection (see Figure 2-16, Figure 2-17, Figure 2-18 and Figure 2-53) supports applications in noisy environments. Our Current-mode architecture gives high CMRR at higher frequencies than was traditional (e.g., 80 dB near 80 kHz, instead of near 60 Hz).

The power supply rejection (see Figure 2-54) also has excellent rejection at higher frequencies than traditional.

5.1 Recommended Design Practices

Some simple design practices help take advantage of the MCP6C02's performance in high side current sensing applications.

5.1.1 INPUT VOLTAGE LIMITS

To prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the V_{IP} and V_{IM} input pins, as well as the differential input voltage V_{DM} (see **Section 1.1, Absolute Maximum Ratings †**). These requirements are independent of the current limits discussed below.

The ESD protection on the V_{IP} and V_{DM} inputs was discussed in **Section 4.3.1, Internal Protection Devices**. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize input bias currents (I_{BP} and I_{BM}).

To protect the inputs, always drive V_{IP} with a low impedance source and use a shunt resistor (R_{SH}) with low resistance (designed to not fail open). Placing zener diode(s) or a transorb across R_{SH} will also help protect the inputs.

5.1.2 INPUT CURRENT LIMITS

To prevent damage to (or improper operation of) these amplifiers, the circuit must limit the currents into the V_{IP} and V_{IM} input pins (see **Section 1.1, Absolute Maximum Ratings †**). This requirement is independent of the voltage limits discussed above.

One way to ensure the input currents are limited is to always drive V_{IP} with a low impedance source, and to use a shunt resistor (R_{SH}) with low resistance (designed to not fail open). Placing zener diode(s) or a transorb across R_{SH} will also help protect the inputs.

5.1.3 BYPASS CAPACITORS

Be sure to specify capacitors that will support your application. Be sure to look at:

- Voltage Rating (well above the maximum value for its pins)
- Dielectrics (good Temp. Cos. and reasonable Volt. Cos.
- Size
- Surface Mount vs. Leaded
- Cost vs. availability

If possible, connect V_{SS} to ground. This will make your design simpler.

Bypass V_{IP} to V_{SS} with a local bypass capacitor next to these pins (e.g.,10 nF). If needed, a bulk bypass capacitor can also be added (e.g.,1 µF).

Bypass V_{DD} to V_{SS} with a local bypass capacitor next to these pins (e.g.,100 nF). A bulk bypass capacitor should also be added close by (e.g.,2.2 µF); placing it next to the local bypass capacitor is a good choice.

5.1.4 PROTECTING THE INPUTS

Designs using the MCP6C02 will need (common) protection methods in the circuit design. When working on the bench, be careful to use the same protection methods (e.g., do not hot-swap the supply voltages). The following subsections give ideas that might be useful in your design.

5.1.4.1 Protecting the V_{IP} Input

Always place a bypass capacitor (C_{IP} in Figure 5-1) from V_{IP} to ground. This helps protect this HV supply input from fast glitches. A 10 nF capacitor is reasonable for many designs.

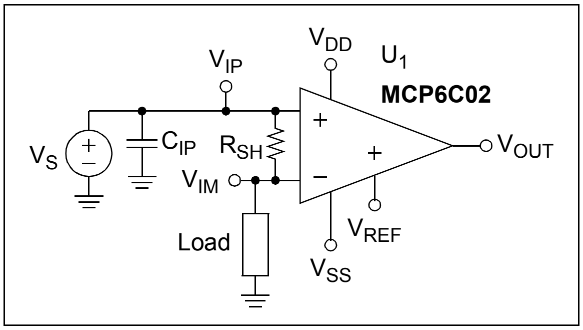


FIGURE 5-1: Protecting V_{IP}

The $\Delta V_{IP}/\Delta t$ spec in Table 1-3 gives the maximum edge rate that should be input to the V_{IP} pin. Limit the source (V_S in Figure 5-1) to slower edge rates.

Limiting the current out of V_S, depending on the application, can also help protect V_{IP}.

5.1.4.2 Protecting V_{DM} (and V_{IM})

The shunt resistor (R_{SH} in Figure 5-2 keeps V_{DM} in range, as long as the load current is not too high. If extra protection is needed in your design, ideas to consider include:

- Limiting V_S's output current
- Setting V_S's output ESR high enough to reduce overshoot
  - The ESR should be a dynamic resistance, not a physical one
- Limit V_{DM} (see Figure 5-2)
  - Add anti-parallel diodes between V_{IP} and V_{IM}, in case RSH fails open
  - Add a capacitor between the V_{IP} and V_{IM} pins

When V_{IP} and V_{DM} are protected, then V_{IM} is too.

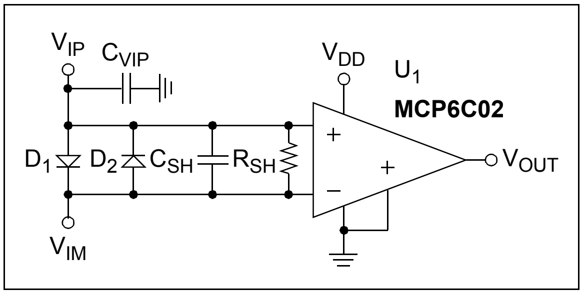


FIGURE 5-2: *Protecting V_{DM} with Diodes.*

5.1.4.3 Protection for Capacitive Loads

Limiting the current from V_S helps protect the circuit in Figure 5-3. The resistance seen by V_S (R_{VS} (V_S's ESR) and R_{CL} (C_L's ESR)) helps reduce step response overshoot, which provides more protection. Using C_{SH} (see Figure 5-2) will create a voltage divider for fast edges; be careful to limit the resulting V_{DM}.

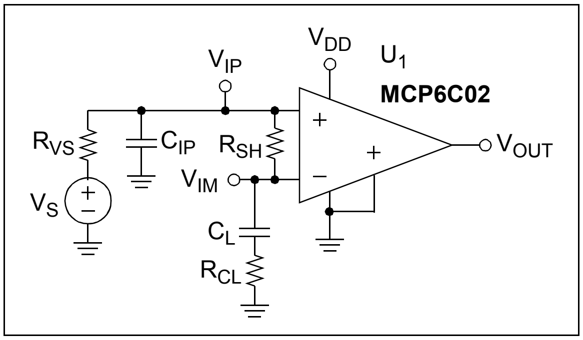


FIGURE 5-3: *Protection for Capacitive Loads.*

5.1.4.4 Protection for Motor Loads

Limiting the current and/or edge rates from V_S helps protect the circuit in Figure 5-4. The resistance R_{VS} (V_S's ESR) might help in some designs. The catch diode (D_1) keeps decaying motor currents near ground, which protects the inputs.

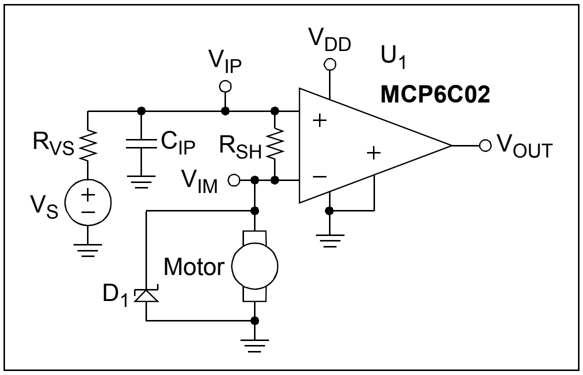


FIGURE 5-4: *Protection for Motor Loads.*

5.1.5 SETTING THE VOLTAGES AT V_{IP} AND V_{IM}

V_{IP} is tied to a voltage source, to minimize glitches and crosstalk. This part's excellent CMRR versus frequency helps reject Common-mode (i.e., at V_{IP}) noise and glitches. A local pass capacitor to V_{SS} can help, when the design allows it; 10 nF is usually a good choice (see the Typical Application Circuit on Page 1).

A shunt resistor (R_{SH}) is connected between V_{IP} and V_{IM}, then to the load (which is grounded). It is selected for the trade-off between accuracy (high R_{SH}) and power dissipation (low R_{SH}). Low power dissipation also leads to reduced size and cost. R_{SH} also helps protect these pins against large glitches; make sure it will never fail open.

The bypass capacitor on V_{IP} reduces the risk of high overvoltage events, when the current changes abruptly (such as an inductive load opening).

A good layout is necessary to minimize DC and AC errors. Figure 5-5 shows a layout that minimizes input resistances seen by I_{BN} and I_{BM}. The critical paths are between R_{SH} and the pins V_{IP} and V_{IM} (R_{WIP} and R_{WIM}).

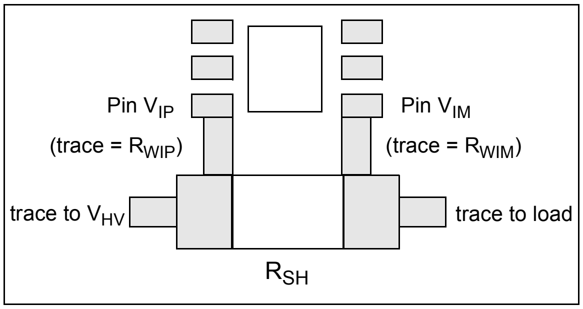


FIGURE 5-5: *PCB Layout for R_{SH} (connections to V_{IP} and V_{IM}).*

For accuracy, the wiring resistances at the device inputs need to be small:

EQUATION 5-1:

$$R_{WIP} \le 4\ m\Omega$$
$$R_{WIM} \le 0.1\Omega$$

5.1.6 SETTING THE VOLTAGE AT V_{REF}

For designs with $V_{REF} = V_{SS}$, short the V_{REF} and V_{SS} pins together; connect them to ground (or other reference) using one low impedance via (or trace). This minimizes DC and AC errors.

For designs with $V_{REF} \ge V_{SS} + 0.1V$, connect V_{REF} and V_{SS} with a relatively large capacitor. Since V_{REF} needs a low impedance source, we recommend the following two design approaches.

The DC resistance seen at V_{REF} needs to be small. This resistance includes trace resistance, via resistance and output resistance of any driving amplifiers. For good gain error in the signal band, maintain this resistance in that band.

EQUATION 5-2:

$$R_{WR} \le 1\Omega$$

The AC impedance seen at V_{REF} needs to support stability at frequencies near the bandwidth. See **Section 5.1.8.1, Driving VREF** for more information.

Figure 5-6 shorts V_{REF} and V_{SS} together. The ADC connects its negative input to V_{REF}, so it can reject glitches on V_{SS} and V_{REF} (notice only one connection to V_{SS} is shown, for good precision).

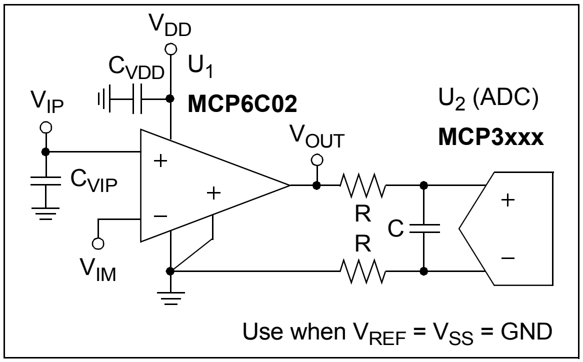


FIGURE 5-6: V_{REF} Bypass Circuit #1.

Figure 5-7 uses an IC VREF to generate $V_{REF} - V_{SS}$, an R-C low-pass filter to reject fast glitches seen at $V_{REF} - V_{SS}$ and an op amp buffer (≥ 1 MHz) to drive V_{REF} with a low impedance source (see Equation 1-2) (notice only one connection to V_{SS} is shown, for good precision).

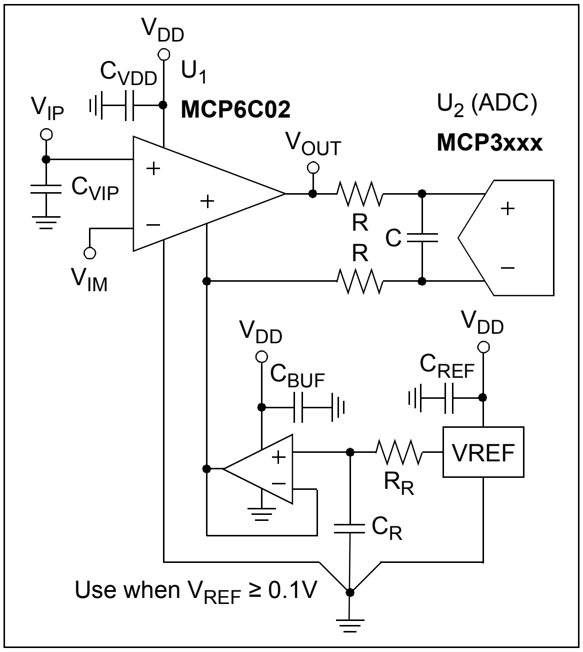


FIGURE 5-7: V_{REF} Bypass Circuit #2.

Driving the V_{REF} pin instead with a simple divider and capacitor will cause potential issues. The equivalent resistance needs to be low (see Equation 5-2), so the divider will draw a lot of current. The capacitor will need to be large, to set a reasonable pole, increasing cost and PCB space.

We strongly recommend against designs with $V_{SS} < V_{REF} < V_{SS} + 0.1V$, since AC glitches may become an problem.

5.1.7 TEMPERATURE RISE

Make sure that T_J does not exceed the Absolute Maximum Junction Temperature spec (see **Section 1.1, Absolute Maximum Ratings †**). This is a strong concern when T_A is high (e.g., above 125°C), when I_{OUT}'s magnitude is large (e.g., near the short circuit limit) or when V_{IP} is high.

Formulas needed for this part of the design are found in **Section 4.1.5, Temperature Performance**.

Figure 2-64 shows that temperature ramp rates need to be limited, for best performance. The decay rates shown there are limited by the PCB and other components.

5.1.8 ENSURING STABILITY

A few simple design techniques will help take advantage of these stable parts. Simulations and bench measurements help to verify the solutions (e.g., look at step response overshoot and ringing).

5.1.8.1 Driving V_{REF}

The voltage source driving the V_{REF} pin must be low impedance (see Equation 1-2), so that the signal gain is constant within the signal bandwidth.

When the frequency is near the bandwidth (e.g., between BW/4 and 4 BW), the source's impedance magnitude should be below 50Ω.

5.1.8.2 Source Impedances

The recommended DC source resistances (at V_{IP}, V_{IM} and V_{REF}; see Equation 5-2) will help ensure stability, by keeping R-C time constants very fast.

5.1.8.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth reduces. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. Lower gains (G_{DM}) exhibit greater sensitivity to capacitive loads.

When driving large capacitive loads with these parts (e.g., > 80 pF), a small series resistor at the output (R_{ISO} in Figure 5-8) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

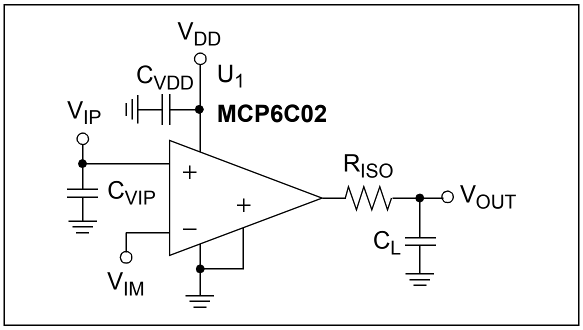


FIGURE 5-8: *Recommended R_{ISO} Values for Capacitive Loads.*

Figure 5-9 shows the typical responses versus C_L, when R_{ISO} is a short circuit (also see Figure 2-70 to Figure 2-73).

Figure 5-10 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the load capacitance (C_L).

After selecting R_{ISO} for the circuit, double check the resulting frequency response peaking and step response overshoot on the bench. Modify R_{ISO}'s value until the response is reasonable.

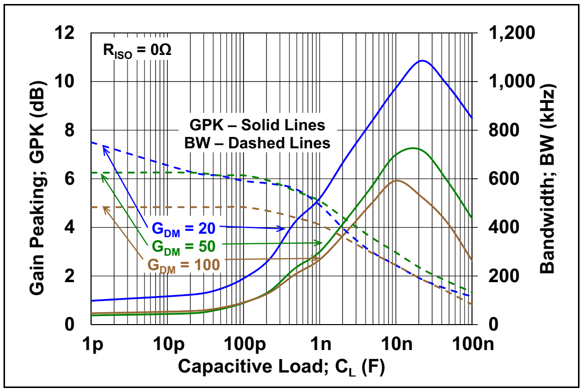


FIGURE 5-9: *Bandwidth and Gain Peaking vs. Capacitive Load, without R_{ISO}.*

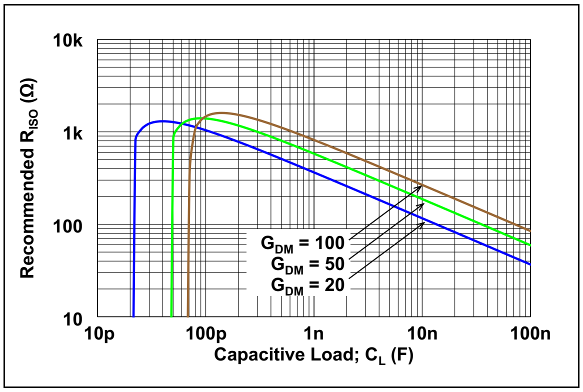


FIGURE 5-10: *Recommended R_{ISO} vs. Capacitive Load.*

5.1.9 NOISE DESIGN

As shown in Figure 2-58 and Table 1-3, the input noise voltage density is white (and low) at low frequencies. This supports accurate averages (DC estimates) in applications.

1/f noise is negligible for almost all applications. As a result, the time domain data in Figure 2-61, Figure 2-62 and Figure 2-63 is well behaved.

Figure 2-58 also shows a curve of the Integrated Input Noise Voltage (E_{ni}, in units of V_{RMS}) between 0 Hz and f (between 0.1 Hz and 100 kHz). To estimate E_{ni} between the frequencies f_1 and f_2, simply take the RMS difference (i.e., $E_{ni}|_{f1 \text{ to } f2}$ = *sqrt*($E_{ni2}^2 – E_{ni1}^2$)).

The Input Noise Voltage Density (e_{ni}) changes with V_{DM}; however, that it is a weak relationship, so it can be neglected in designs.

Figure 5-11 and Figure 5-12 show the device noise as a Signal-to-Noise ratio (SNR), assuming the signal is a full-scale sine wave (at V_{OUT}). The x-axis is the circuit's bandwidth (BW), to make it easy to evaluate a particular design.

The input offset voltage is shown as a Signal-to-Offset ratio (SVosR), to indicate where the DC offset dominates the error.

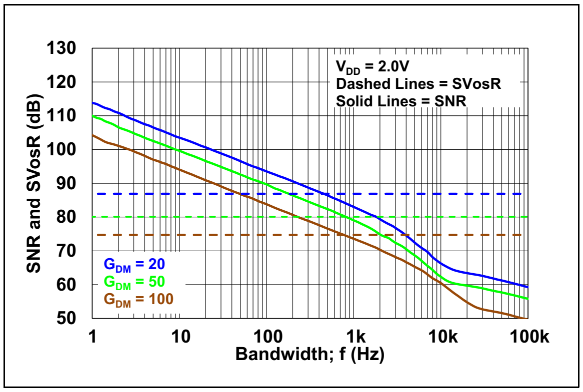


FIGURE 5-11: *SNR vs. Bandwidth Estimates, V_{DD} = 2.0V.*

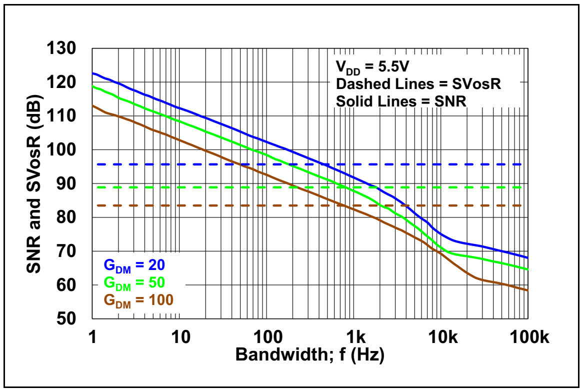


FIGURE 5-12: *SNR vs. Bandwidth Estimates, V_{DD} = 5.5V.*

5.1.10 UNIDIRECTIONAL APPLICATIONS

In unidirectional applications where $V_{REF} = V_{SS}$, it is important to minimize output headroom (V_{OL}). The lower V_{OL} is, the more accurate the zero scale reading is.

To reduce V_{OL}, make I_{OUT} as low as possible. This is done by making R_L high and by tying V_L to V_{SS}.

Figure 5-6 shows how to connect V_{REF} and V_{SS} for best performance.

5.1.11 BIDIRECTIONAL APPLICATIONS

Figure 5-7 shows ways to connect V_{REF} and V_{SS} for best performance.

To maximize headroom, reduce V_{OL} and V_{OH} by setting R_L high.

5.1.12 SUPPLY PINS

As described in **Section 3.5 "Low-Side Power Supplies (VDD, VSS)"**, the ground potential (GND) can be set where needed in your design. The most common design approach has V_{SS} = GND (positive single supply). Other common design approaches have V_{DD} = GND (negative single supply) or V_{SS} < GND < V_{DD} (dual, or split, supplies).

Setting V_{SS} = GND has the potential to increase rejection of crosstalk and glitches. In any case, a good ground design (e.g., ground plane on a PCB) and appropriate bypass capacitors are needed to realize these benefits. It pays to be sure that your capacitor's voltage rating and dielectric will support your needs over your voltage and temperature ranges. With some dielectrics, it pays to also take aging (changes over time) into account too.

5.2 Typical Application Circuits

The following circuits give guidance on using the MCP6C02 within common applications. They leave out details and the design requirements followed.

5.2.1 MOTOR CURRENT MONITORS

Figure 5-13 shows a simplified DC Motor Current Monitor circuit with a regulated voltage supply. The MCP6C02 and its circuit are all connected to the same ground, for better glitch performance. In this case, since I_L is non-negative, we choose $V_{REF} = V_{SS}$.

The ADC operates on a different supply; its ground will be different due to I-R drops and glitches. The differential input is tied to V_{REF}, so that its CMRR can reject differences between grounds.

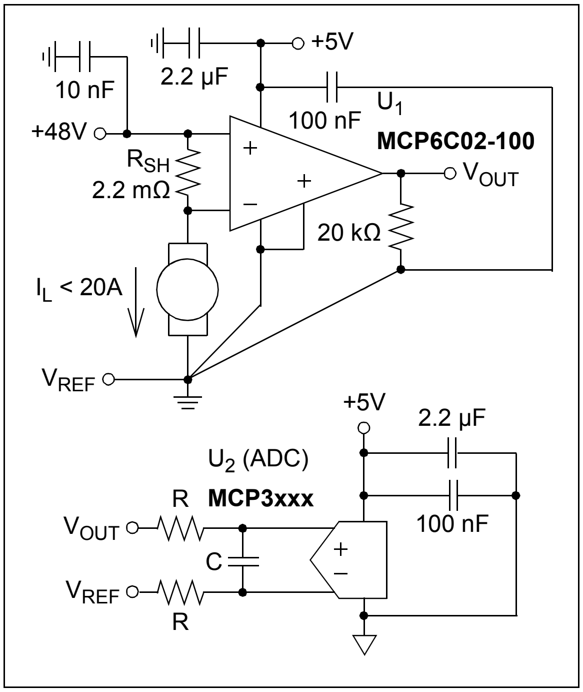


FIGURE 5-13: *Motor Current Monitor for Regulated Supply Voltage.*

H-Bridge motor drive circuits can place their current monitors in several positions. Figure 5-14 shows a few possibilities:

- Position A – This uses a unidirectional monitor (MCP6C02 at V_{A1} and V_{A2}), with current polarity determined by the timing of the switches (SW_{LT}, etc.)

- Positions B and C – This uses two unidirectional monitors (on MCP6C02 at V_{B1} and V_{B2} and the other at V_{C1} and V_{C2}), with each one representing one current polarity
- Position D – This uses a bidirectional monitor (MCP6C02 at V_{D1} and V_{D2}), with current polarity determined by the output
  - The monitor must function at and below ground
  - The monitor must withstand large switching steps and glitches
  - We caution that the MCP6C02 should not be used in these conditions.

Obviously, choosing different locations for the monitor(s) gives trade-offs in accuracy and complexity. For instance, the monitor at Position D directly measures the motor current, but will have large voltage swings at its V_{IP} pin.

The switches are discrete semiconductor switches (i.e., CMOS, Bipolar, IGFET, etc.).

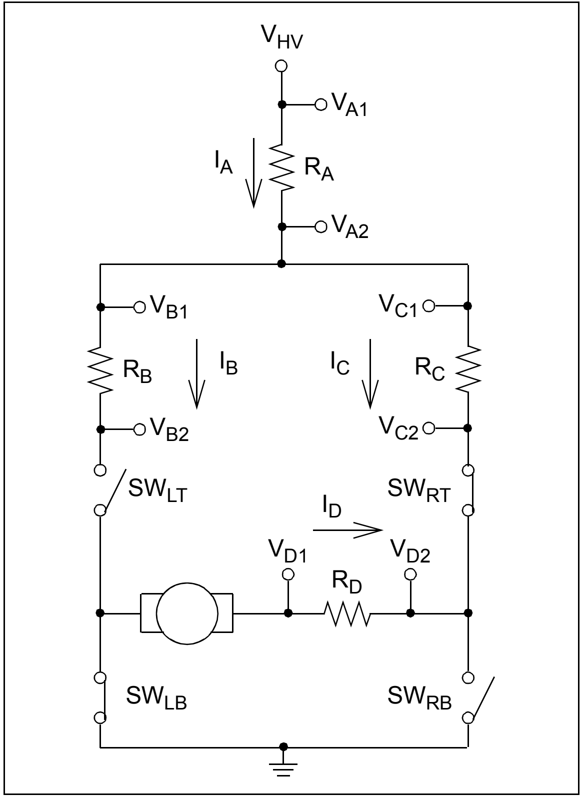


FIGURE 5-14: *H-Bridge Motor Current Monitor, With a Few Possible Monitor Locations.*

5.2.2 ANALOG LEVEL SHIFTER

The MCP6C02 can be used to shift analog voltages from a high positive voltage down to a low voltage. Many possibilities exit; Figure 5-15 is just one possible implementation.

The input attenuator (R_1 and R_2) allow a wider range of voltages to be measured. No resistor is placed between V_1 and the noninverting input, so that the input current I_{BP} doesn't cause an offset shift. The attenuator resistors' accuracy and values may affect the circuit's gain error and offset.

The +2.5V reference level allows bidirectional voltage sensing; it needs to be very low impedance and reject glitches on the supply or ground (see Figure 5-7 for recommendations on this part of the circuit).

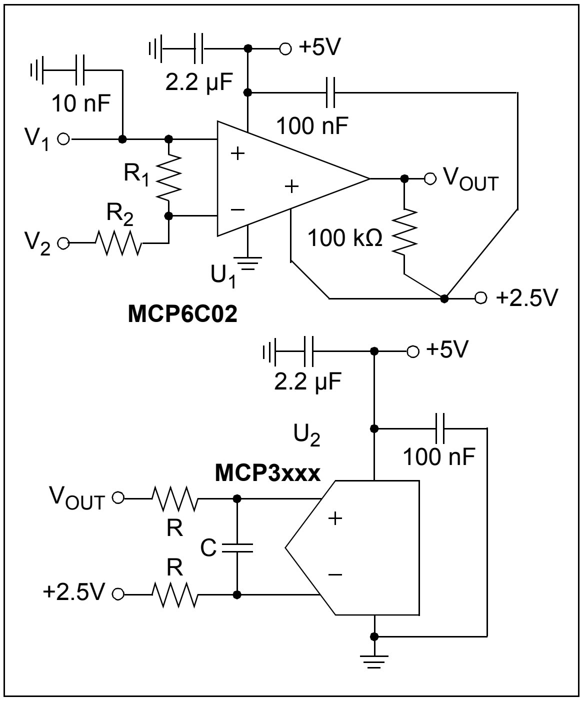
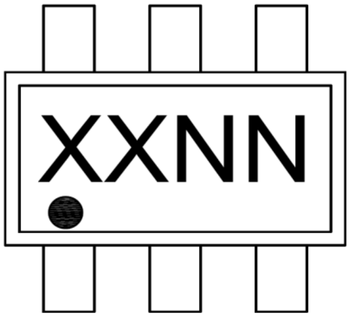


FIGURE 5-15: *Analog Level Shifter.*

6.0 PACKAGING INFORMATION

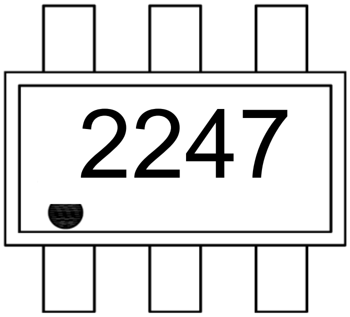
6.1 Package Marking Information

6-Lead SOT-23

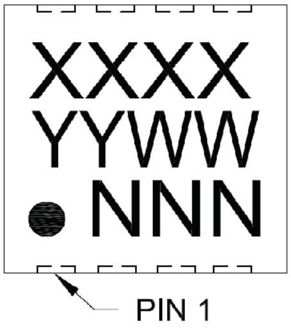


Part Number	Code
MCP6C02T-020E/CHY	22
MCP6C02T-050E/CHY	25
MCP6C02T-100E/CHY	21
MCP6C02T-020E/CHYVAO	22
MCP6C02T-050E/CHYVAO	25
MCP6C02T-100E/CHYVAO	21

Example

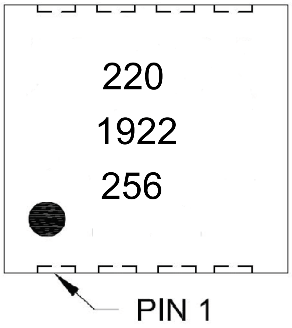


8-Lead VDFN



Part Number	Code
MCP6C02T-020H/Q8B	220
MCP6C02T-050H/Q8B	250
MCP6C02T-100H/Q8B	2100
MCP6C02T-020H/Q8BVAO	220
MCP6C02T-050H/Q8BVAO	250
MCP6C02T-100H/Q8BVAO	2100

Example

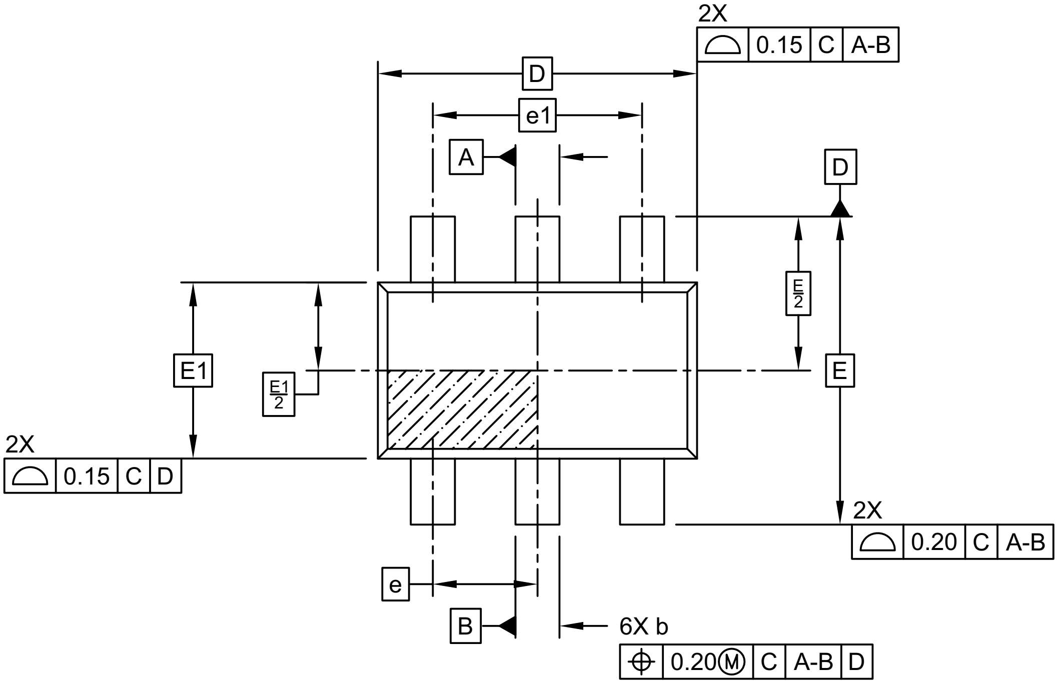


Legend:	XX...X	Device-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

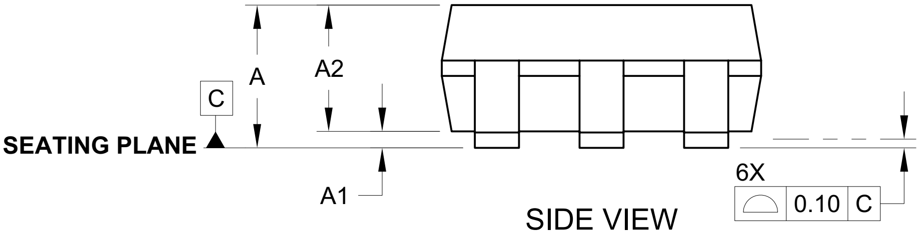
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

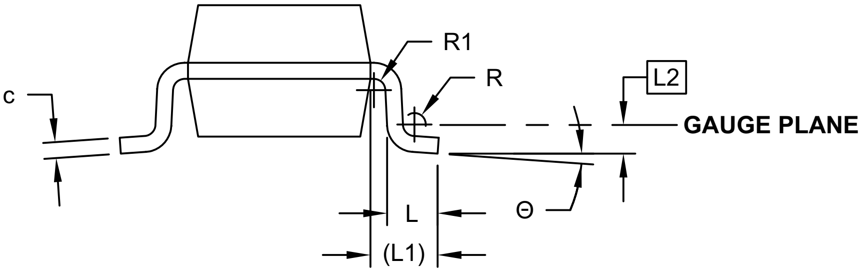
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

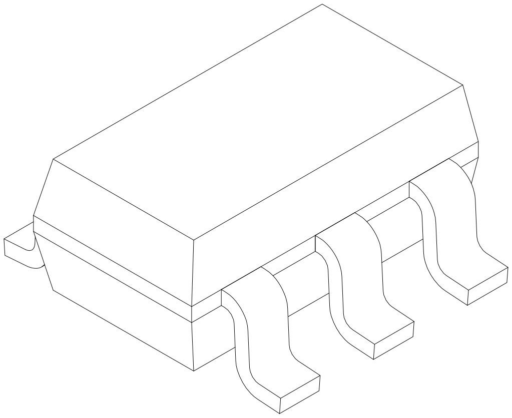


END VIEW

Microchip Technology Drawing C04-028C (CH) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Seating Plane to Gauge Plane	L1		0.25 BSC	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

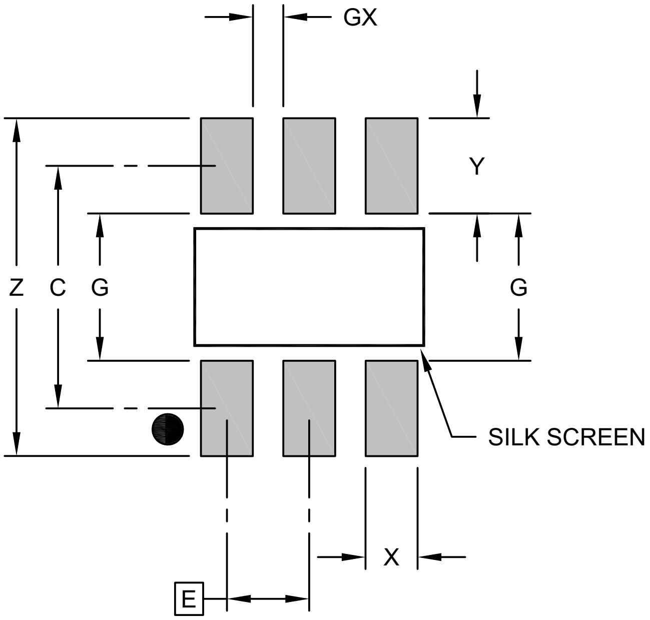
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028C (CH) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

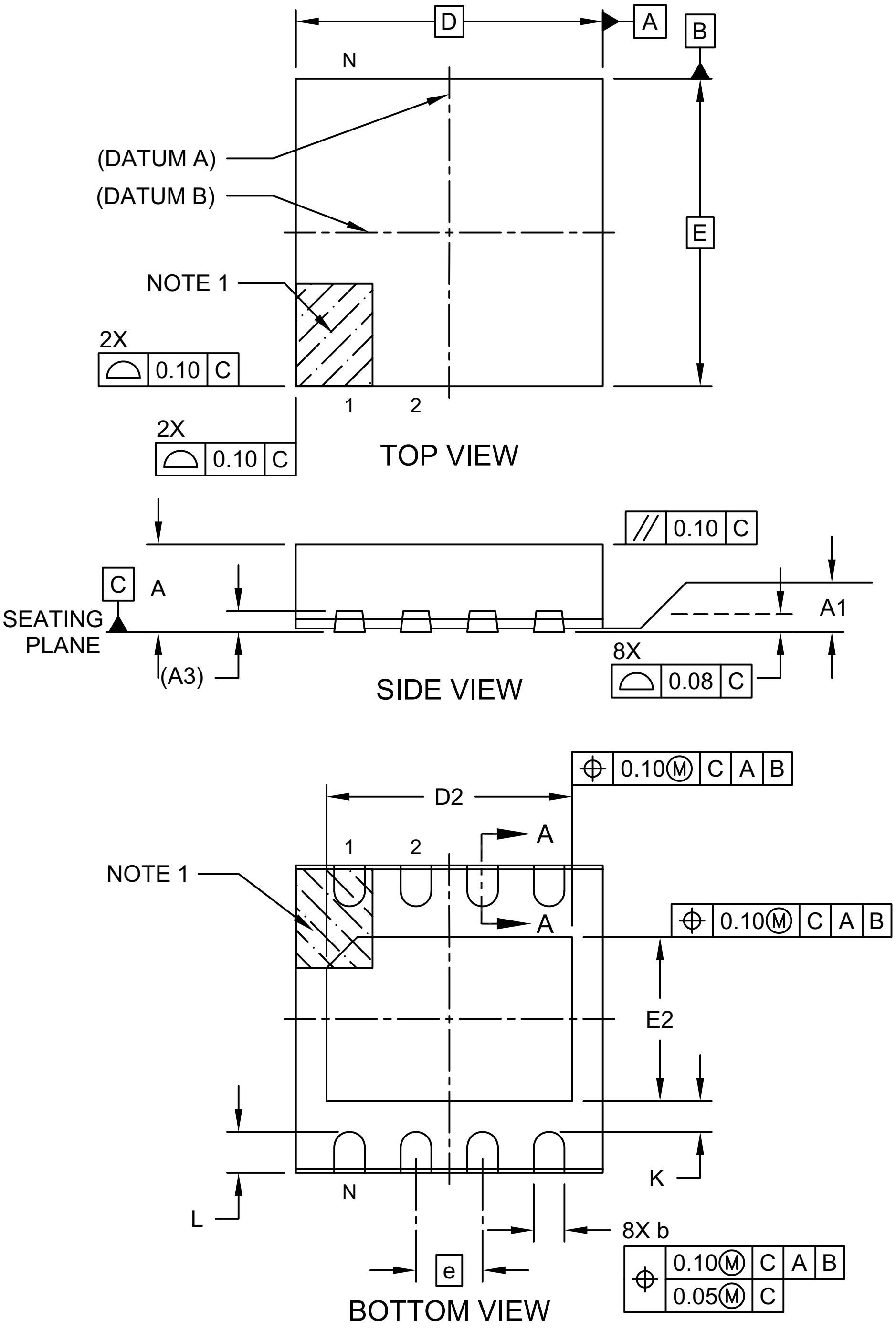
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028B (CH)

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

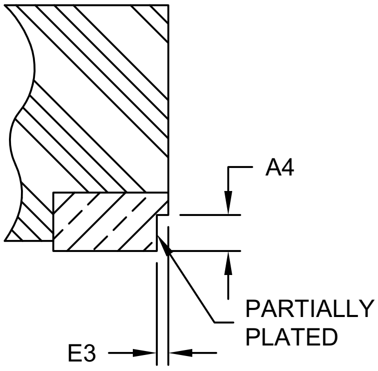
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



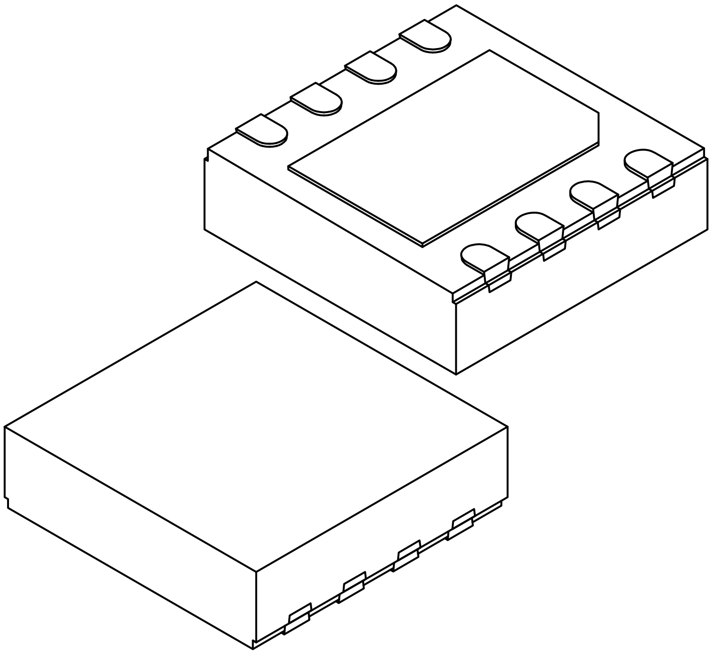
Microchip Technology Drawing C04-21358 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A–A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

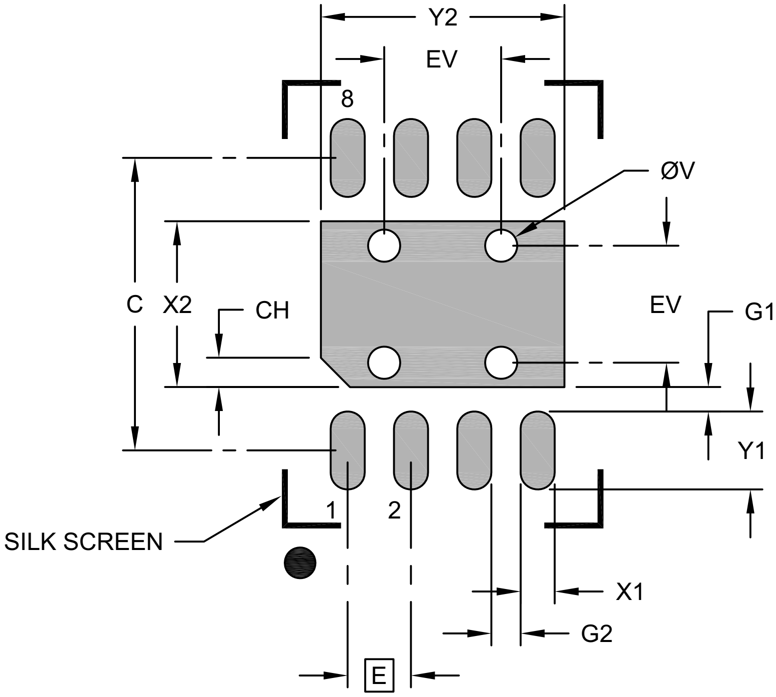
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev B

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (September 2019)

The following is the list of modifications.

1. Added the H-Temp part in an 8 lead 3 × 3 VDFN package.
2. Clarified specifications, timing diagrams and power calculations.
3. Added discussion on circuit protection.

Revision A (November 2018)

- Initial release of this document.

NOTES:

APPENDIX B: OFFSET TEST SCREENS

Input offset voltage specifications in the DC spec table (Table 1-1) are based on bench measurements (see **Section 2.1, DC Precision**). These measurements are much more accurate than at test, because:

- More compact circuit
- Parts soldered on the PCB
- More time spent averaging (reduced noise)
- Better temperature control
    - Reduced temperature gradients
    - Greater accuracy

We use production screens to support the quality of our V_{OS} specification in outgoing products. The screen limits are wider and are used to eliminate fliers; see **Table B-1**.

TABLE B-1: OFFSET TEST SCREENS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.0V to 5.5V, V_{SS} = GND, V_{IP} = 34V, V_{DM} = 0V, $V_{REF} = V_{DD}/4$, $V_L = V_{DD}/2$ and R_L = 10 kΩ to V_L; see Figure 1-9 and Figure 1-10.

Parameters	Sym.	Min.	Max.	Units	Gain	Conditions
input Offset Voltage	V_{OS}	-34	+34	µV	20	Test Screen
		-24	+24		50	
		-20	+20		100	

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XXX	X(2)	/XXX(2)	XXX(3)
Device	Tape and Reel Option	Gain Option	Temperature Range	Package	Class

Device: MCP6C02: Zero-Drift, 65V High-Side Current Sense Amp

Tape and Reel Option:
T = Tape and Reel(1)

Gain Option:
020 = Differential Gain of 20 V/V
050 = Differential Gain of 50 V/V
100 = Differential Gain of 100 V/V

Temperature Range:
E = -40°C to +125°C(2) (Extended)
H = -40°C to +150°C(2) (High)

Package:
CHY = Plastic Small Outline Transistor (SOT-23(2)), 6-Lead
Q8B = Very Thin Plastic Dual Flat Outline (3x3 VDFN(2)), 8-Lead

Class:
(Blank) = Non-Automotive
VAO = Automotive

Examples:

a) MCP6C02T-020E/CHY:	Tape and Reel, Differential Gain = 20, Extended Temperature, 6LD SOT-23
b) MCP6C02T-050E/CHY:	Tape and Reel, Differential Gain = 50, Extended Temperature, 6LD SOT-23
c) MCP6C02T-100E/CHY:	Tape and Reel, Differential Gain = 100, Extended Temperature, 6LD SOT-23
d) MCP6C02T-020H/Q8B:	Tape and Reel, Differential Gain = 20, High Temperature, 8LD VDFN
e) MCP6C02T-050H/Q8B:	Tape and Reel, Differential Gain = 50, High Temperature, 8LD VDFN
f) MCP6C02T-100H/Q8B:	Tape and Reel, Differential Gain = 100, High Temperature, 8LD VDFN
g) MCP6C02T-020E/CHYVAO:	Automotive, Tape and Reel, Differential Gain = 20, Extended Temperature, 6LD SOT-23
h) MCP6C02T-050E/CHYVAO:	Automotive, Tape and Reel, Differential Gain = 50, Extended Temperature, 6LD SOT-23
i) MCP6C02T-100E/CHYVAO:	Automotive, Tape and Reel, Differential Gain = 100, Extended Temperature, 6LD SOT-23
j) MCP6C02T-020H/Q8BVAO:	Automotive, Tape and Reel, Differential Gain = 20, High Temperature, 8LD VDFN
k) MCP6C02T-050H/Q8BVAO:	Automotive, Tape and Reel, Differential Gain = 50, High Temperature, 8LD VDFN
l) MCP6C02T-100H/Q8BVAO:	Automotive, Tape and Reel, Differential Gain = 100, High Temperature, 8LD VDFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: E-Temp parts are only in the SOT-23 package. H-Temp parts are only in the 3×3 VDFN package.

3: Automotive parts are AEC-Q100 qualified. SOT-23 packaged parts are Grade 1 and VDFN packaged parts are Grade 0.

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