MCS7720

USB 1.1 to Dual Serial Controller

Features

- USB Specification 1.1 Compliant
- Single 5V Operation
- On-Chip Regulator
- Low Power
- Dual Serial Ports
- Supports up to 920Kbps Data Rate
- Supports 8,7,6 & 5 Data Widths
- Supports Even, Odd, Mark, Space & None Parities
- Supports 1, 1.5 & 2 Stop Bits
- Internal Power-On Reset
- Available in 48-pin QFP Package

Applications

- High-Speed Modems
- Monitoring Equipment
- Serial Networking

Application Note

- AN-7720

Evaluation Board

- MCS7720-EVB

General Description

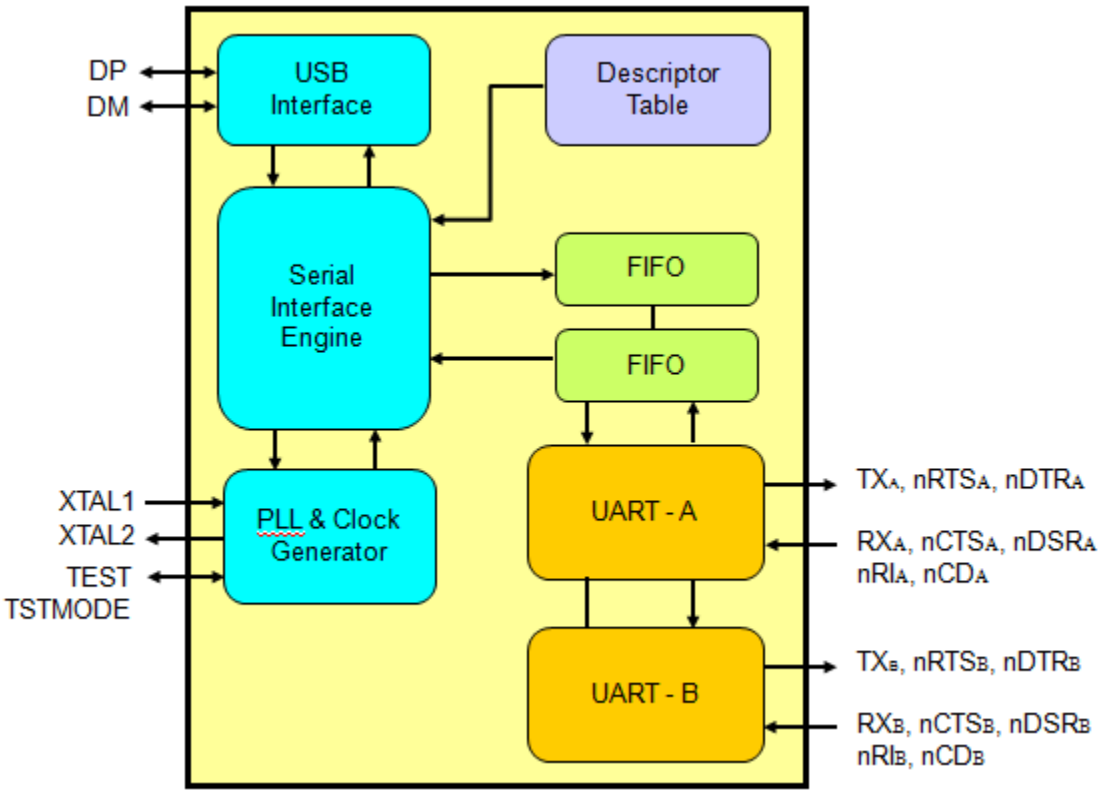
The MCS7720 controller provides bridging between the Universal Serial Bus (USB) input and two enhanced UART ports. This device contains all the necessary logic to communicate with the host computer via the USB Bus.

In addition, the MCS7720 contains a 3.3V regulator, operates in Bus-Powered mode, and has a reduced frequency (6 MHz) crystal oscillator.

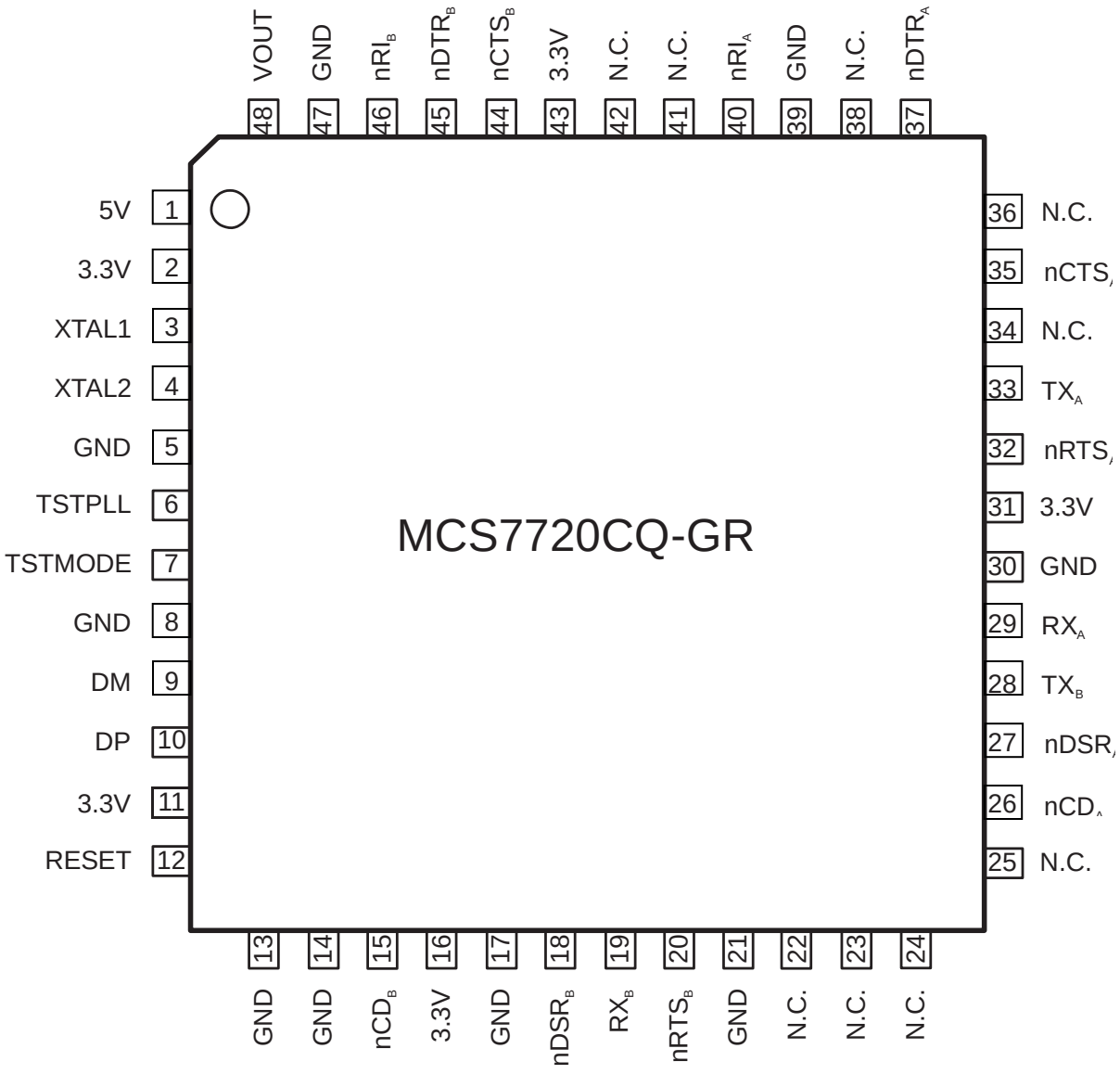
This combination of features allows significant cost savings in system design, along with straightforward implementation of serial port functionality into PC peripherals using the host's USB port.

Ordering Information		
Commercial Grade (0° C to +70° C)		
MCS7720CQ-GR	48-LQFP	RoHS

Block Diagram



Pin-Out Diagram



Pin Assignments

Name	Pin	Type	Description
XTAL1	3	I	Crystal oscillator input or external clock input (6 MHz). This signal input is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external (10 pF) capacitors connected from each side of the crystal to GND are required to form a crystal oscillator
XTAL2	4	O	Crystal oscillator output. See XTAL1 description.
TSTPLL	6	I	Test Mode (active low, internal pull-up) input. When this pin is tied to GND, the internal PLL is bypassed and an external 48 MHz clock is used as the reference clock.
TSTMODE	7	I	Internal Test Mode (internal pull-up). When this pin is tied to GND, the internal test mode is enabled.
DM	9	I/O	Upstream USB port Differential data Minus (D-), analog.
DP	10	I/O	Upstream USB port Differential data Plus (D+), analog.
RESET	12	I	System Reset (Active high). Resets all internal registers, sequencers, and signals to a consistent state. Connect to GND to enable the internal Power-On Reset circuit.
nCD_B	15	I	Carrier-Detect signal (B). When low this indicates that the modem or data set has detected the data carrier. nCD has no effect on the transmitter.
$nDSR_B$	18	I	Data-Set-Ready signal (B). When low, this indicates the modem or data set is ready to establish a communication link.
RX_B	19	I	Serial Data Input (B).
$nRTS_B$	20	O	Request-To-Send signal (B). It is set high (inactive) after a hardware reset or during internal loop-back mode. When low, this indicates that the UART is ready to exchange data. nRTS has no effect on the transmitter or receiver.
nCD_A	26	I	Carrier-Detect signal (A). When low this indicates that the modem or data set has detected the data carrier. nCD has no effect on the transmitter.
$nDSR_A$	27	I	Data-Set-Ready signal (A). When low, this indicates the modem or data set is ready to establish a communication link.
TX_B	28	O	Serial Data Output (B).
RX_A	29	I	Serial Data Input (A).

Name	Pin	Type	Description
$nRTS_A$	32	O	Request-To-Send signal (A). It is set high (inactive) after a hardware reset or during internal loop-back mode. When low, this indicates that the UART is ready to exchange data. nRTS has no effect on the transmitter or receiver.
TX_A	33	O	Serial Data Output (A).
$nCTS_A$	35	I	Clear-To-Send signal (A). When low this indicates that the modem or data set is ready to exchange data. nCTS has no effect on the transmitter.
$nDTR_A$	37	O	Data-Terminal-Ready signal (A). It is set high (inactive) after a hardware reset or during internal loop-back mode. When low, this output indicates to the modem or data set that the UART is ready to establish a communication link. nDTR has no effect on the transmitter or receiver.
nRI_A	40	I	Ring-Detect signal (A).
$nCTS_B$	44	I	Clear-To-Send signal (B). When low this indicates that the modem or data set is ready to exchange data. nCTS has no effect on the transmitter.
$nDTR_B$	45	O	Data-Terminal-Ready signal (B). It is set high (inactive) after a hardware reset or during internal loop-back mode. When low, this output indicates to the modem or data set that the UART is ready to establish a communication link. nDTR has no effect on the transmitter or receiver.
nRI_B	46	I	Ring-Detect signal (B).
VOUT	48	PWR	+3.3V Voltage Regulator Output.
GND	5, 8, 13, 14, 17, 21, 30, 39, 47	PWR	Power and signal grounds.
3.3V	2, 11, 16, 31, 43	PWR	Device Supply inputs. All should be connected to the VOUT pin. The VOUT voltage is gated by RESET.
5V	1	PWR	Main Power Input. Connect to USB VBUS or local VDD.

Note: All names with “n” prefix are active low.

USB Description

Analog Transceivers

The on-chip transceivers are connected directly to USB cables through external series resistors. They transmit and receive serial data at both full-speed (12Mbit/s) and low-speed (1.5Mbit/s) data rates. Slew rates are automatically adjusted according to the speed of the device connected and lie within the range defined in the *USB Specification Rev. 1.1*.

Serial Interface Engine

This engine implements the complete USB protocol layer including: parallel /serial conversion, synchronization pattern recognition, CRC checking/ generation, bit (de)stuffing, packet identifier (PID) verification/generation, address recognition and handshake evaluation/generation.

Bit Clock Recovery

The bit clock recovery circuit recovers the clock from the incoming USB data stream using 4x over sampling. It is able to track in the presence of jitter and frequency drift as specified by the USB Specification Rev. 1.1.

3.3V Source

A 5V to 3.3V DC-DC regulator is integral to the chip relieving the need for a +3.3V source. It supplies the analog transceivers and internal logic and can be used to supply the 1.5kΩ pull-up resistor on the DP line of the upstream connection.

PLL Clock Multiplier

An integral Phase-Locked Loop (PLL) performs 6 to 48MHz clock multiplication and requires no external components except the crystal. This allows for the use of low-cost 6MHz crystals which reduce high frequency radiated Electro-Magnetic Interference (EMI).

USB Interface

All standard USB requests received from the host are processed on-board without the need of firmware intervention. The MCS7720 supports Bus-Powered operation only. The USB interface to the host controller includes a Control endpoint, a Bulk-In endpoint, a Bulk-Out endpoint and an Interrupt endpoint. The USB controller supports the USB- specification. Hence, it supports all standard functionality associated with device enumeration, standard USB device requests, etc. In addition, there are Vendor Specific commands provided to allow a USB driver to access registers and ROM in the USB controller.

UART Register Set:
The UART has 10 registers. Mapping is dependent on the Line Control Register (LCR).

Register Name	Offset	R/W	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
THR	0	W	Data to be transmitted (Transmitting Holding Register)							
RHR	0	R	Data to be received (Receiver Holding Register)							
IER	1	R/W	Reserved			Sleep Mode	Modem Interrupt Mask	Rx Stat Interrupt Mask	THRE Interrupt Mask	RxRdy Interrupt Mask
FCR	2	W	RHR Trigger Level		Reserved		Reserved	Flush THR	Flush RHR	FIFO Enable
ISR	2	R	FIFOs Enabled		Reserved		Interrupt Priority			Interrupt Pending
LCR	3	R/W	DLE	Tx Break	Force Parity	Odd/Even Parity	Parity Enable	Stop Bits	Data Length	
MCR	4	R/W	Reserved		RTS/CTS Flow Control	Loop	Unused		RTS	DTR
LSR	5	R	Data Error	Tx Empty	THR Empty	Rx Break	Framing Error	Parity Error	Overrun	RxRdy
MSR	6	R	DCD	RI	DSR	CTS	Delta DCD	TERI	Delta DSR	Delta CTS
SPR	7	R/W	Scratch Pad Register							

Additional Standard Registers – these are accessed when LCR[7] = 1

DLL	0	R/W	Divisor Latch bits[7:0]
DLM	1	R/W	Divisor Latch bits[15:8]

Register: **THR**
Description: **Data to be transmitted**
Offset: **0**
Permissions: **Write**
Access Condition: **LCR[7] =0, only write condition can access this register**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Data to be transmitted							

Register: **RHR**
Description: **Data to be received**
Offset: **0**
Permissions: **Read**
Access Condition: **LCR[7] =0, only read condition can access this register**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Data to be received							

Interrupt Enable Register:
Serial channel interrupts are enabled using the Interrupt Enable Register (IER).

Register: **IER**
Description: **Interrupt Enable Register**
Offset: **1**
Permissions: **Read/Write**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Reserved			Sleep Mode	Modem Interrupt Mask	Rx Stat Interrupt Mask	THRE Interrupt Mask	RxRdy Interrupt Mask

Bit	Name	Description
0	RxRdy Interrupt Mask	Logic 0 = Disable the Receiver Ready Interrupt Logic 1 = Enable the Receiver Ready Interrupt
1	THRE Interrupt Mask	Logic 0 = Disable the Transmitter Ready Interrupt Logic 1 = Enable the Transmitter Ready Interrupt
2	Rx Stat Interrupt Mask	Logic 0 = Disable the Receiver Status Interrupt (Normal Mode) Logic 1 = Enable the Receiver Status Interrupt (Normal Mode)
3	Modem Interrupt Mask	Logic 0 = Disable the Modem Status Interrupt Logic 1 = Enable the Modem Status Interrupt
4	Sleep Mode	Logic 0 = Disable Sleep-Mode Logic 1 = Enable Sleep-Mode (the internal clock of the channel is switched off)
5	Reserved	Reserved
6	Reserved	Reserved
7	Reserved	Reserved

FIFO Control Register:
The FCR controls the UART behavior in various modes.

Register: **FCR**
Description: **FIFO Control Register**
Offset: **2**
Permissions: **Write**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
RHR Trigger Level		Reserved		Reserved	Flush THR	Flush RHR	Enable FIFO

Bit	Name	Description
0	Enable FIFO Mode	Logic 0 = Byte Mode Logic 1 = FIFO Mode
1	Flush RHR	Logic 0 = No change Logic 1 = Flushes the contents of RHR. This is operative only in FIFO Mode. The RHR is automatically flushed whenever changing between Byte Mode and FIFO Mode. The bit will return to zero after clearing the FIFOs.
2	Flush THR	Logic 0 = No change Logic 1 = Flushes the content of the THR, in the same manner as FCR[1] does the RHR
3	Reserved	Reserved
5, 4	Reserved	Reserved
7, 6	RHR Trigger Level	See the table below.

FCR[7:6] RHR Trigger Level:
In 550 mode, the receiver FIFO trigger levels are defined using FCR[7:6]. The interrupt trigger level & flow control trigger level where appropriate are defined by L2 in the table below. L1 defines lower flow control trigger levels that introduce a hysteresis element in hardware RTS/CTS flow control.
In Byte Mode (450 Mode) the trigger levels are all set to 1.

FCR[7:6]	550 Mode (FIFO = 16)	
	L1	L2
2'b00	1	1
2'b01	1	4
2'b10	1	8
2'b11	1	14

Interrupt Status Register:
The source of the highest priority interrupt pending is indicated by the contents of the Interrupt Status Register (ISR). There are five sources of interrupts, and four levels of priority (1 is the highest) as tabulated below.

Level	Interrupt Source	ISR[5:0]
-	No interrupt pending	6'b000001
1	Receiver Status Error or address bit detected in 9-bit mode	6'b000110
2a	Receiver Data Available	6'b000100
2b	Receiver Time Out	6'b001100
3	Transmitter THR Empty	6'b000010
4	Modem Status Change	6'b000000

Note: ISR[0] indicates whether any interrupt is pending

Register: **ISR**
Description: **Interrupt Status Register**
Offset: **2**
Permissions: **Read**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
FIFOs Enabled		Interrupt Priority (Enhanced Mode)		Interrupt Priority (All Modes)			Interrupt Pending

Interrupt Descriptions:
Level1: Receiver Status Error
Normal Mode: This interrupt is active whenever any of the LSR[1], LSR[2], LSR[3] or LSR[4] are set. These flags are cleared following a read of the LSR. The interrupt is masked with IER[2].

Level 2a: Receiver Data Available
The interrupt is active whenever the receiver FIFO level is above the interrupt trigger level.

Level 2b: Receiver Time-Out
A receiver time out event, (which may cause an interrupt) will occur when all of the following conditions are true:

- The UART is in the FIFO Mode.
- There is data in the RHR
- There has been no read of the RHR for a period of time greater than the timeout period. The time-out period of time is greater than the time out period. *The time out period is four times the character period (including start & stop bits) measured from the centre of the first stop bit of the first data item received*.

Reading the first data item in RHR clears this interrupt.

Level 3: Transmitter Empty
This interrupt is set when the transmit FIFO level falls below the trigger level. It is cleared on the ISR read to Level-3 interrupt or by writing more data to the THR so that the trigger level is exceeded.

Level 4: Modem Change
This interrupt is set by the modem change flag (MSR[0], MSR[1], MSR[2] or MSR[3]) becoming active due to changes in the input modem lines. This interrupt is cleared following the read of the MSR register.

Line Control Register:
The LCR specifies the data format that is common to both transmitter and receiver.

Register: **LCR**
Description: **Line Control Register**
Offset: **3**
Permissions: **Read/Write**
Access Condition: **LCR[7] =0**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
DLE	Tx Break	Force Parity	Odd/Even Parity	Parity Enable	Number of Stop Bits	Data Length	

LCR[1:0]: Determines the data length of serial characters.

LCR[1:0]	Data Length
2'b00	5 bits
2'b01	6 bits
2'b10	7 bits
2'b11	8 bits

LCR[2]: Defines the number of stop bits per serial character.

LCR[5:3]: The selected parity type will be generated during transmission and checked by the receiver, which may produce a parity error as a result. In 9-bit mode parity is disabled and LCR[5:3] are ignored.

LCR[2]	Data Length	Stop Bits
0	5,6,7,8	1
1	5	1.5
1	6,7,8	2

LCR[6]: Transmission Break
- Logic 0: Break transmission disabled
- Logic 1: Forces the transmitter data output (SOUT) low to alert the communications channel. It is the responsibility of the software driver to ensure that the break duration is longer than the character period for it to be recognized remotely as a break rather than data.

LCR[5:3]	Parity Type
3'bxx0	No parity
3'b001	Odd parity
3'b011	Even parity
3'b101	Parity bit forced to 1
3'b111	Parity bit forced to 0

LCR[7]: Divisor Latch Enable
- Logic 0: Accesses to DLL and DLM registers disabled
- Logic 1: Accesses to DLL and DLM registers enabled

Modem Control Register:

Register: **MCR**
Description: **Modem Control Register**
Offset: **4**
Permissions: **Read/Write**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
550 Mode							
Unused		CTS/RTS Flow Control	Internal Loop Back Enable	Out2 (Interrupt Enable)	Out1	RTS	DTR

Bit	Name	Description
0	DTR	Logic 0 = Forces DTR# output to inactive (high) Logic 1 = Forces DTR# output to active (low)
1	RTS	Logic 0 = Forces RTS# output to inactive (high) Logic 1 = Forces RTS# output to active (low)
2	Out1	Unused
3	Out2	Unused
4	Internal Loop Back Enable	Logic 0 = Normal operating mode Logic 1 = Enable Local Loop-Back Mode
5	CTS/RTS flow control	Logic 0 = CTS/RTS flow control Disabled in 550-Mode Logic 1 = CTS/RTS flow control Enabled in 550-Mode
6	Unused	Unused
7	Unused	Unused

Line Status Register:
This register provides the status of the data transfer to the CPU.

Register: **LSR**
Description: **Line Status Register**
Offset: **5**
Permissions: **Read**
Access Condition: **LCR[7] =0, ACR[6] = 0**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Data Error	Tx Empty	THR Empty	Rx Break	Framing Error	Parity Error	Overrun	RxRdy

Bit	Name	Description
0	RHR Data Available	Logic 0 = RHR is empty Logic 1 = RHR is not empty, data is available to be read
1	RHR Overrun	Logic 0 = No overrun error Logic 1 = Data was received when the RHR was full, An overrun has occurred. The error is flagged when the data would normally have been transferred to the RHR.
2	Received Data Parity Error	Logic 0 = No parity error in received data, or 9th bit is "0" in 9-bit mode. Logic 1 = Data has been received that did not have correct parity
3	Received Data Framing Error	Logic 0 = No framing error Logic 1 = data has been received with an invalid stop bit.
4	Received Break Error	Logic 0 = No receiver break error Logic 1 = the receiver received a break error
5	THR Empty	Logic 0 = Transmitter FIFO is not empty Logic 1 = Transmitter FIFO is empty
6	Transmitter & THR Empty	Logic 0 = The transmitter is not idle Logic 1 = THR is empty & the transmitter has completed the character in the shift register and is in the idle mode
7	Receiver Data Error	Logic 0 = Either there are no receiver data errors in the FIFO, or it was cleared by earlier read of LSR Logic 1 = At least one parity error, framing error or break indication in the FIFO.

Note : A break condition occurs when the SIN line goes low and stays low through out the start, data, parity & first stop bits. One zero character associated with break flag set will be transferred to the RHR and the receiver will then wait until the SIN line returns high. The LSR[4] flag break flag is set when this data item gets to the top of the RHR and it is cleared following the read to the LSR.

Modem Status Register:
This register provides the status of the modem control lines to CPU.

Register: **MSR**
Description: **Modem Status Register**
Offset: **6**
Permissions: **Read**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
DCD	RI	DSR	CTS	Delta DCD	Trailing Edge RI	Delta DSR	Delta CTS

Bit	Name	Description
0	Delta CTS	Logic 0 = no change in the CTS signal Logic 1 = indicates that the CTS input has changed since the last time the MSR was read
1	Delta DSR	Logic 0 = no change in the DSR signal Logic 1 = indicates that the DSR input has changed since the last time the MSR was read
2	Trailing Edge RI	Logic 0 = no change in the RI signal Logic 1 = indicates that the RI input has changed from low to high since the last time the MSR was read
3	Delta DCD	Logic 0 = no change in the DCD signal Logic 1 = indicates that the DCD input has changed since the last time the MSR was read
4	CTS	Logic 0 = CTS# line is 1 Logic 1 = CTS# line is 0
5	DSR	Logic 0 = DSR# line is 1 Logic 1 = DSR# line is 0
6	RI	Logic 0 = RI# line is 1 Logic 1 = RI# line is 0
7	DCD	Logic 0 = DCD# line is 1 Logic 1 = DCD# line is 0

Scratch Pad Register:
The scratch pad register does not effect operation of the rest of the UART in any way and can be used for the temporary data storage.

Register: **SPR**
Description: **Scratch Pad Register**
Offset: **7**
Permissions: **Read/Write**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Scratch Pad Register							

Divisor Latch Registers:
The divisor latch registers (DLL & DLM) are used to program the baud rate divisor. This is a value between 1 and 65535 by which the input clock is divided in order to generate serial Baud Rates. After a hardware Reset, the Baud Rate used by the transmitter & receiver is given by:

Baud Rate = Input Clock / 16 * Divisor

where divisor is given by: (256 * DLM) + DLL

Note: More flexible Baud Rate generation options are also available. These require the use of Advanced Features in other registers however.

Register: **DLL**
Description: **Divisor Latch Register**
Offset: **0**
Permissions: **Read/Write**
Access Condition: **LCR[7] =1**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Least significant Byte for divisor latch							

Register: **DLM**
Description: **Divisor Latch Register**
Offset: **1**
Permissions: **Read/Write**
Access Condition: **LCR[7] =1**

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Most significant Byte for divisor latch							

Baud Rate Generator Programming Table

Baud Rate	DLM (Hex)	DLL (Hex)
115.2K	00	01
57.6K	00	02
38.4K	00	03
19.2K	00	06
9600	00	0C
2400	00	30
1200	00	60
600	00	C0
300	01	80
150	03	00
50	09	00

Master Reset Values

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	0	0	0	0	0	0	0	0
THR	X	X	X	X	X	X	X	X
IER	0	0	0	0	0	0	0	0
FCR	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	X	X	X	X	0	0	0	0
SPR	0	0	0	0	0	0	0	0

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage	6 Volts
Input Voltage (I/O)	-0.3 to V_{CC} +0.3
Storage Temperature	-60° C to +150° C

Recommended Operating Conditions

Supply Voltage	4.5 to 5.5 Volts
Input Voltage (I/O)	0 to 5.5 Volts
Ambient Operating Temperature (free air)	0° C to +70° C
Junction Operating Temperature	0° C to +115° C

Static Characteristics (Supply Pins)

V_{CC} = 4.5V to 5.5V; GND = 0V; Temp = 0 to +70° C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{reg} (3.3V)	Regulated Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Operating Supply Current		-	18	-	mA

Static Characteristics

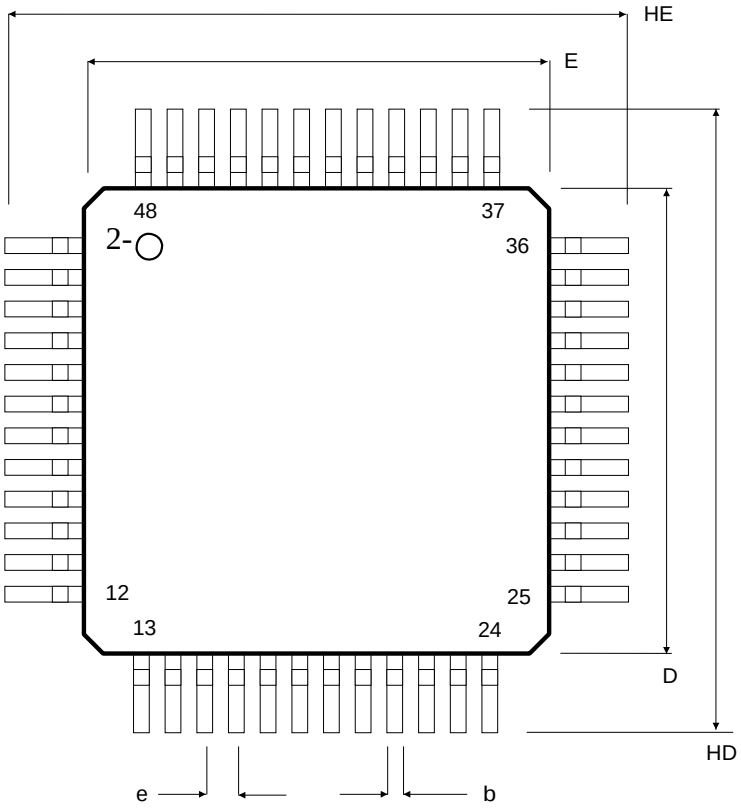
V_{CC} = 4.5V to 5.5V; GND = 0V; Temp = 0 to +70° C; unless otherwise specified

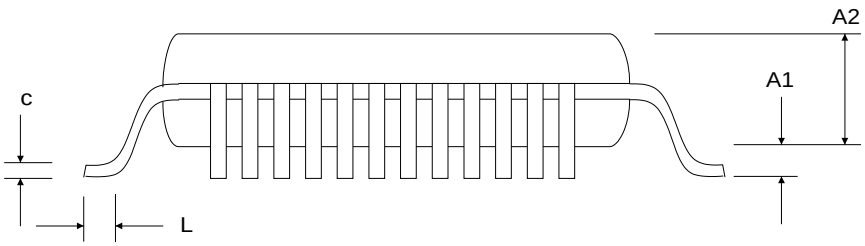
Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{IL}	LOW Level Input Voltage		-	-	0.3*Vcc	V
V_{IH}	HIGH Level Input Voltage		0.7*Vcc	-	-	V
V_{th}(LH)	Positive going Threshold Voltage		-	3.22	-	V
V_{th}(HL)	Negative going Threshold Voltage		-	1.84	-	V
I_{LI}	Input Leakage Current		-	-	±1	µA
I_{OZ}	Tri-State Leakage Current		-	-	±10	µA
V_{OL}	Output Voltage (Low)		-	-	0.4	V
V_{OH}	Output Voltage (High)		3.5	-	-	V

Dynamic Characteristics – Analog I/O Pins (DP, DM); Full-Speed Mode

V_{CC} = 4.5V to 5.5V; GND = 0V; Temp = 0 to +70° C; unless otherwise specified

Symbol	Parameter	Condition	Min	Typical	Max	Unit
T_{FR}	Rise Time	C_L = 50pF 10% to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	nS
T_{FF}	Fall Time	C_L = 50pF 10% to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	nS





48-Pin QFP
Package Dimensions

SYMBOL	MILLIMETERS			INCHES		
	MIN	TYPICAL	MAX	MIN	TYPICAL	MAX
A1	0.05		0.15	0.002		0.006
A2	1.35		1.45	0.053		0.057
b	0.17		0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
e		0.50			0.0197	
L	0.45		0.75	0.018		0.030
HD	8.80		9.20	0.346		0.362
D	7.20		6.80	0.283		0.268
HE	8.80		9.20	0.346		0.362
E	7.20		6.80	0.2.83		0.268

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Revision History

Revision	Date	Comment
1.0	7-Nov-2002	Preliminary Release
1.1	27-Mar-2006	Revised Data Sheet
2.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram.
2.01	2011/11/01	1. Updated the ordering information.

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