MCS7780

USB 1.1 to IrDA Controller

Features

- USB Specification 1.1 Compliant.
- Supports all USB Standard Commands.
- Full Compliance to IrDA 1.4
- WHQL Certified
- Low-Power CMOS Design
- Powered from USB port
- Single 12 MHz Crystal
- IrDA Data Rates from 2.4 Kbps to 115.2 Kbps in SIR mode
- Supports MIR (Medium IR) at 1.152 Mbps
- Supports FIR (Fast IR) mode with Data Rate of 4 Mbps
- Uses Standard IrDA Transceivers
- LED Driver capable of 650 mA @ 5V, 25% Duty Cycle
- Low-Profile 28-Pin SSOP Package

Applications

- High-Speed IrDA Communications
- Cell Phone Interface Cable

Application Note

- AN-7780

Evaluation Board

- MCS7780-EVB

"IrReady Qualified" in Demo Adapters
Customer boards require IrDA qualification

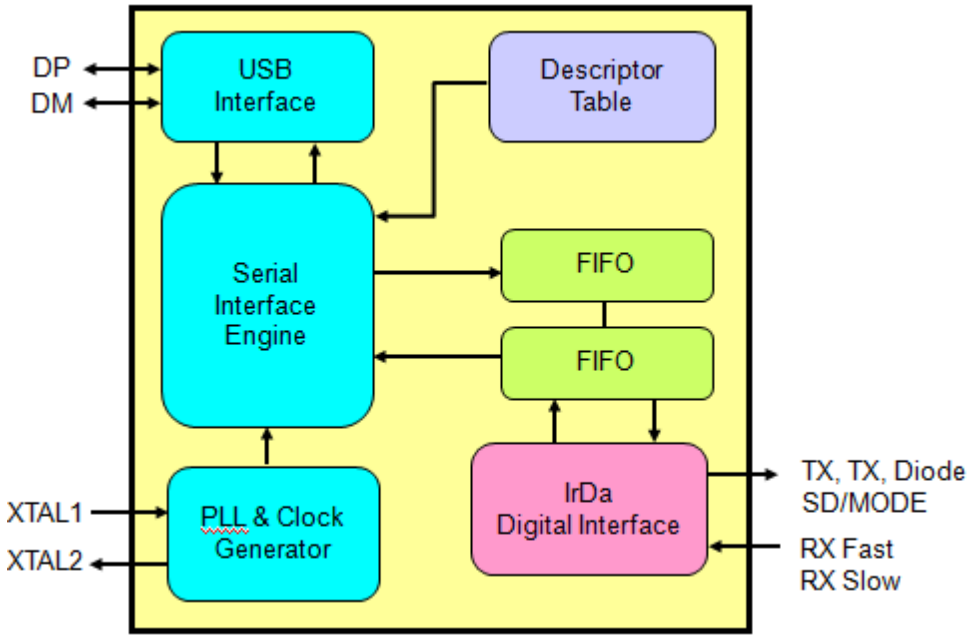
General Description

The MCS7780 controller provides bridging between the Universal Serial Bus (USB) input and an IrDA wireless data communication port. This device contains all the necessary logic to communicate with the host computer via the USB Bus.

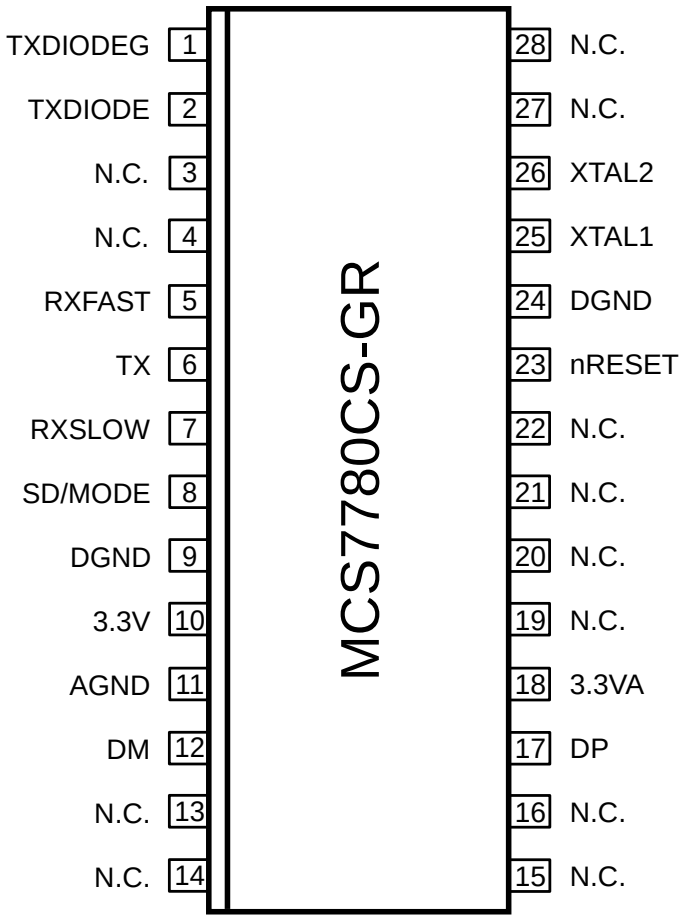
The MCS7780 operates in Bus-Powered mode, and uses a reduced frequency (12MHz) crystal oscillator. This combination of features allows significant cost savings in system design along with straight forward implementation of IrDA port functionality into PC peripherals using the host's USB port.

Ordering Information		
Commercial Grade (0° C to +70° C)		
MCS7780CS-GR	28-SSOP	RoHS

Block Diagram



28-Pin SSOP Package



Pin Descriptions

Pin Name	Pin	Type	Description
TXDIODEG	1	PWR	Optional LED Driver Output GND
TXDIODE	2	O	Optional Transmit LED Driver Output
RXFAST	5	I	Receive Data from IR module (Fast)
TX	6	O	Transmit Data output to IR module
RXSLOW	7	I	Receive Data from IR module (Slow)
SD/MODE	8	O	Mode Control to IR module
DM	12	I/O	USB Interface differential Data Negative
DP	17	I/O	USB Interface differential Data Positive
nRESET	23	I	Master Reset, (active low)
XTAL1	25	I	12 MHz Crystal/Clock Input
XTAL2	26	O	12 MHz Crystal/Clock Output
3.3VA	18	PWR	USB Transceiver Power Supply
3.3V	10	PWR	Digital Power Supply
AGND	11	PWR	USB Transceiver Power Supply Ground
DGND	9, 24	PWR	Digital Power Supply Ground

Functional Description

The MCS7780 consists of two major functional blocks, the USB controller, and the digital IR transceiver. The USB controller provides Control, Bulk-In, and Bulk-Out endpoints to the USB host. The digital IR transceiver consists of transmit and receive interfaces that connect to an analog IR front end.

This USB/IrDA Bridge Controller has full interface capability to connect between a USB Bus, and an IrDA compatible infrared transceiver device.

USB Interface

The USB Device Controller implements a USB protocol engine. It has one configuration with a single interface. Two Bulk endpoints with maximum packet size of 64 Bytes are used for data transfers. The MCS7780 uses Vendor Specific commands for IR configuration and control. Two vendor specific requests ("Write Word" & "Read Word") are defined for this purpose. The vendor specific requests are piped through the Control endpoint.

"Write Word" is a 2 phase transaction which can be used to write a single 16-bit register. The setup phase of this command supplies both the index and data value to be written into the register. There is no data phase in this transfer.

The "Read Word" request is used to read the register contents of the MCS7780. It allows reading one 16-bit register at a time. The setup phase specifies the register address to be read and the data is returned in the data phase.

Digital IR Transceiver

The Digital IR Transceiver is responsible for driving the transmit diode and receiving the digital input from an analog IR front end. The primary components are the transmit modulator, the receive demodulator, the FIFO, the analog transmit section, and the register array.

By programming the registers in the register array, the device's operation is determined. Various registers are used to specify operations such as the modulation scheme, the Baud rate, the current frame size in the FIFO, the RX input selection, etc.

In steady state transmit operation, the USB controller is filling the FIFO with data while the Digital IR Transceiver is emptying it via the transmit modulator. In steady state receive operation, the USB controller is emptying the FIFO while the RX demodulator is filling the FIFO.

IR FRAMING

Framing involves adding wrappers around the payload received from NDIS to make a valid IR frame. MCS7780 uses a custom framing style to achieve low gate count. The hardware and software together play a role in making of SIR, MIR, and FIR frames.

Mode Register: offset 0x00

Name	Bit	Access	Default	Description
FIR	0 *	R/W	0	1 = Puts the device in Fast Infrared mode (4MHz). 0 = Device uses SIR/MIR mode based on Baud Rate register.
SIR	1 *	R/W	0	1 = The SIR pulse width of 1.6 uS is used. 0 = The SIR pulse used is 3/16th of bit time.
BBTG	2	R/W	1	1 = Enables back to back transmission with no inter packet gap. Invalid in SIR mode.
ASK	3 *	Reserved		Reserved
PARITY	4 *	R/W	0	1 = Odd parity to be used by ASK. 0 = Even parity is used
RATE	[7:5] *	R/W	1	Baud Rate selector. (See Table Below)
PLLPWD	8	R/W	1	1 = Enable power down feature of the PLL 0 = power down feature of the PLL disabled.
DRIVER	9	R/W	0	1 = Upon initialization. 0 = Upon reset. *The Device Driver sets this bit as the first step of initialization to enable further access to the register set.*
DTD	10	R/W	1	1 = Device determines the transfer direction automatically. 0 = The direction is controlled by software by writing a 1 (TX) or 0 (RX) in DIR bit of this register
DIR	11	R/W	0	1 = Transmit 0 = Receive *This bit is valid only when DTD = 0.* *Software should check the CHGDIR bit before writing to this bit.*
SIPEN	12	R/W	1	1 = Enables automatic hardware generation of SIP pulse. 0 = Disables the auto SIP generation. Software must generate it through Vendor Specific commands.
SENDSIP	13	R/W	0	On detecting a transition from low to high on this bit, the device generates a SIP.
CHGDIR	14	R	1	1 = Software is allowed to change the transfer direction by writing to DIR bit. 0 = Direction change is not allowed. Software polls until this bit goes high before changing direction.
RESET	15	R/W	1	0 = Resets the bridge and IR TOP modules. *This bit is self clearing.*

** IR needs to be reset when this bit is changed.*

Baud Rate	Frequency Selected
0	2.4 Kbps
1	9.6 Kbps
2	19.2 Kbps
3	38.4 Kbps
4	57.6 Kbps
5	115.2 Kbps
6	0.576 Mbps
7	1.152 Mbps

Framing Register: offset 0x01

Name	Bit	Access	Default	Description
STAL	[7:0]	R/W	0x00	*The number of STAs to be used* * Bit-7 = 1, The 6 LSBs indicate the number of STAs to be used. * Bit-7 = 0, Uses the values hard coded in the design.
IPG	[15:8]	R/W	0x00	*Inter-packet gap* *Specified in terms of number of bit times (MIR) or chip time (FIR).* * Bit-15 = 1, The 6 LSBs indicate the inter-packet gap to be used. * Bit-15 = 0, Uses the values hard coded in the design.

** IR needs to be reset when this bit is changed.*

XCVR Register: offset 0x02

Name	Bit	Access	Default	Description
MODE0	0	R/W	0	Used to configure the transceiver. The usage varies with the transceiver make and is reflected in the transceiver truth table.
STFIR	1	R/W	0	Used to configure the transceiver. The usage varies with the transceiver make and is reflected in the transceiver truth table.
XCVR	2	R/W	0	1 = Puts the transceiver in Configuration Mode. 0 = Puts the transceiver in Data Transfer Mode.
RXFAST	3	R/W	0	1 = Causes the device to use RXFAST as the input pin for receive from transceiver. 0 = Causes the device to use RXSLOW as the receive signal.
TXCUR	[6:4]	R/W	0	Sets the current control bits of the pad that drives TX-LED. This controls the current supplied to TX-LED.
MODE1	7	R/W	0	Used to configure the transceiver. The usage varies with the transceiver make and is reflected in the transceiver truth table.
SMODE0	8	R/W	1	Value of MODE0 to be configured to put it into shut down. Varies with transceiver make.
SMODE1	9	R/W	0	Value of MODE1 to be configured to put it in shut down. Varies with transceiver make.
INVTX	10	R/W	0	1 = inverts the data bits being fed into transceiver for transmit. 0 = the transmit line works as active high signal.
INVRX	11	R/W		1 = RXD line from transceiver is treated as an active low signal 0 = RXD line from transceiver is treated as an active high signal.
EEDATA	[15:12]	R	0	Loaded from the EEPROM.

The table below shows the usage of XCVR Register for various Transceivers.

Vendor	Code	Dynamic Configuration			
		MODE0	MODE1	STC_FIR	Latched From
Vishay TDFU6614	0	1->0	0	0	TXD
Vishay TDFU6102	0	1->0	0	0	TXD
SHARP GP2W100YP	1	1->0	0	1	TXD
Agilent 3602/3600	2	Can switch pins dynamically. There is no latching mechanism			

SIP Resister: offset 0x03

Name	Bit	Access	Default	Description
SIPON	[6:0]	R/W	0x4C	Specifies pulse width of the SIP in terms of number of 48 MHz clocks.
SIPOFF	[15:7]	R/W	0x154	The SIP low time. Specified as of number of 48 MHz clocks.

MINRXPW Register: offset 0x04

Name	Bit	Access	Default	Description
MNRXW	[15:0]	R/W	0x00	*Minimum pulse width of the signal to be received.* 0 = Device uses the hard coded values. X = non zero Device uses the value specified from this register.

TXPW Register: offset 0x05

Name	Bit	Access	Default	Description
TXPW	[15:0]	R/W	0x00	*Pulse width of the signal transmitted.* 0 = device uses the hard coded values X = non zero value, device uses the value specified from this register.

RFIFO2 Register: offset 0x06

Name	Bit	Access	Default	Description
TIMEOT	[7:0]	R/W	0x0A	*Timeout specified in intervals of 50mS.* *Used in SIR mode to abort a receive if idle for long period specified by this register.* N => N*50 mS timeout.
TRSHD	[14:8]	R/W	0x40	FIFO Threshold
CLRFF	15	R/W	0	1 = Clear FIFO pointers 0 = FIFO pointers not cleared *This bit is self clearing*

RESV Register: offset 0x07

Name	Bit	Access	Default	Description
IRINTX	0	R	0	1 = Indicates that transmit is in progress 0 = Indicates that transmit is not in progress
IRINRX	1	R	0	1 = Indicates that the receive is in progress 0 = Indicates that receive is not in progress
RESV	[15:2]	R/W	0x0A	Reserved

Absolute Maximum Ratings

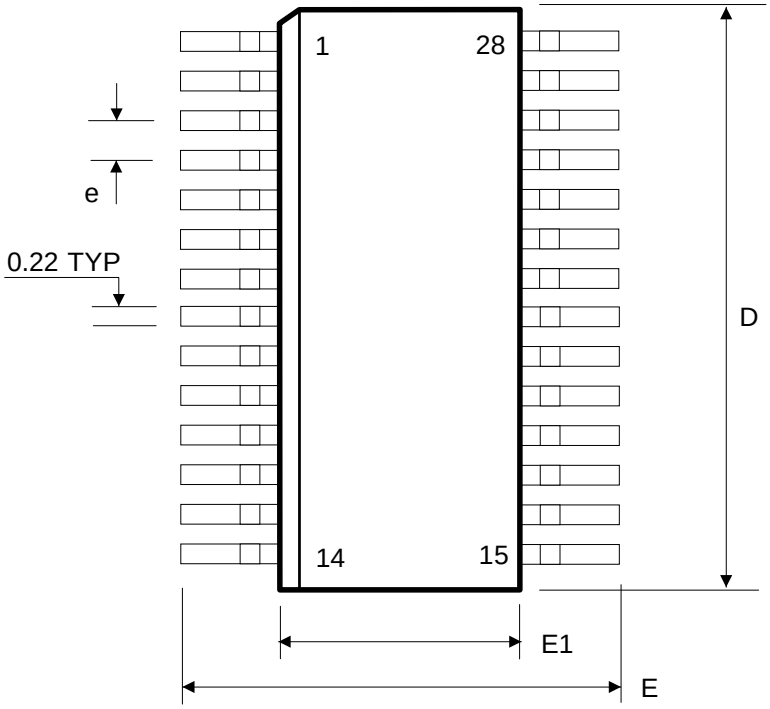
Supply Voltage	3.8 Volts
Voltage at any pin	GND - 0.3 to Vcc + 0.3
Operating Temperature	-45° C to +90° C
Storage Temperature	-65° C to +150° C
Package Dissipation	500 mW
ESD	±2000 Volts
Latch up	220 mA

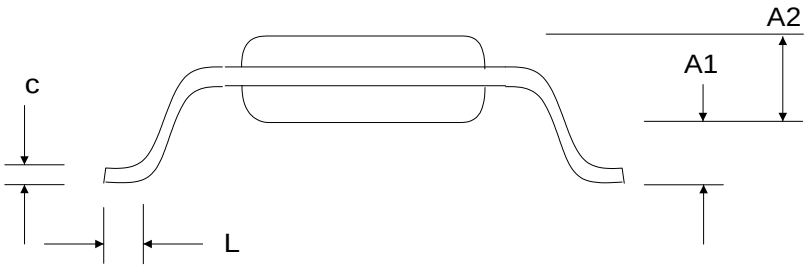
DC Electrical Specifications
Temp = 0° C to +70° C, Vcc = 3.3V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Max	Unit	Condition
Vcc	Supply Voltage	3.0	3.6	V	
$Vclk_L$	Clock input low level	-0.5	0.6	V	External
$Vclk_H$	Clock input high level	2.4	Vcc	V	External
Vi_L	Input low level		1.08	V	CMOS
Vi_H	Input high level	2.1		V	CMOS
Vo_L	Output low level		0.4	V	Io_L = 4 mA
Vo_H	Output high level	1.85		V	Io_H = 4 mA
Ii_L	Input leakage current	-10	+10	µA	
Icc	Operating current	12	19	mA	
Cp	Input pin Capacitance		5	pF	

AC Electrical Specifications
Temp = 0° C to +70° C, Vcc = 3.3V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Max	Unit	Condition
CLKA	USB clock frequency	12	12	MHz	±50PPM





28-Pin SSOP
Package Dimensions

SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A1	0.05		0.21	0.020		0.08
A2	1.65		1.80	0.650		0.708
C			0.25			
e		0.65			0.026	
D	10.00		10.4	3.93		4.09
E	7.4	7.8	8.2			
E1	5.2		5.4	2.05		2.12
L	0.55	0.75	0.95			

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Revision History

Revision	Date	Comment
1.0	Feb-2004	Corrections
1.1	9-Dec-2005	Corrected Package Dimensions
1.2	3-Jan-2006	Corrected Internal Register Details
2.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram.
2.01	2011/11/01	1. Updated the ordering information.

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