MCS7830

USB 2.0 to 10/100M Fast Ethernet Controller

Features

- USB 2.0 Device Controller
  - Integrated USB 2.0 PHY
  - USB Specification 2.0 Compliant
  - Supports all USB Standard Commands
  - Supports Five Vendor Specific Commands
  - Supports USB Suspend/Resume Detection Logic
- 10/100 Mbps Ethernet Controller
  - Integrated MAC and PHY
  - IEEE 802.3 Compliant
  - Supports Full Duplex Operation in 10/100 Mbps Modes
  - Exhaustive MAC Status Reporting
  - Supports PAUSE Control Frames
- Support Low Power Mode / Remote Wakeup
- Serial Interface to Read/Write to 93LC46B EEPROM through USB
- On-Chip FIFO's for Upstream and Downstream Data Transfers
- WHQL Certified
- Configurable Vendor and Product ID's through EEPROM
- Supports iSerial Number and Locally Administered Network Address
- Supports MII interface for External Ethernet PHY (128-pin package only)

Applications

- Add-On 10/100 Dongle
- Instrumentation
- Embedded Applications

Application Note

- AN-7830-DA-128
- AN-7830-DA-80

Evaluation Board

- MCS7830CQ-BCD
- MCS7830CV-BCD

General Description

The USB to MAC Ethernet Controller is a unique solution to interface 10/100 Base-T Ethernet devices to the Universal Serial Bus (USB-2.0).

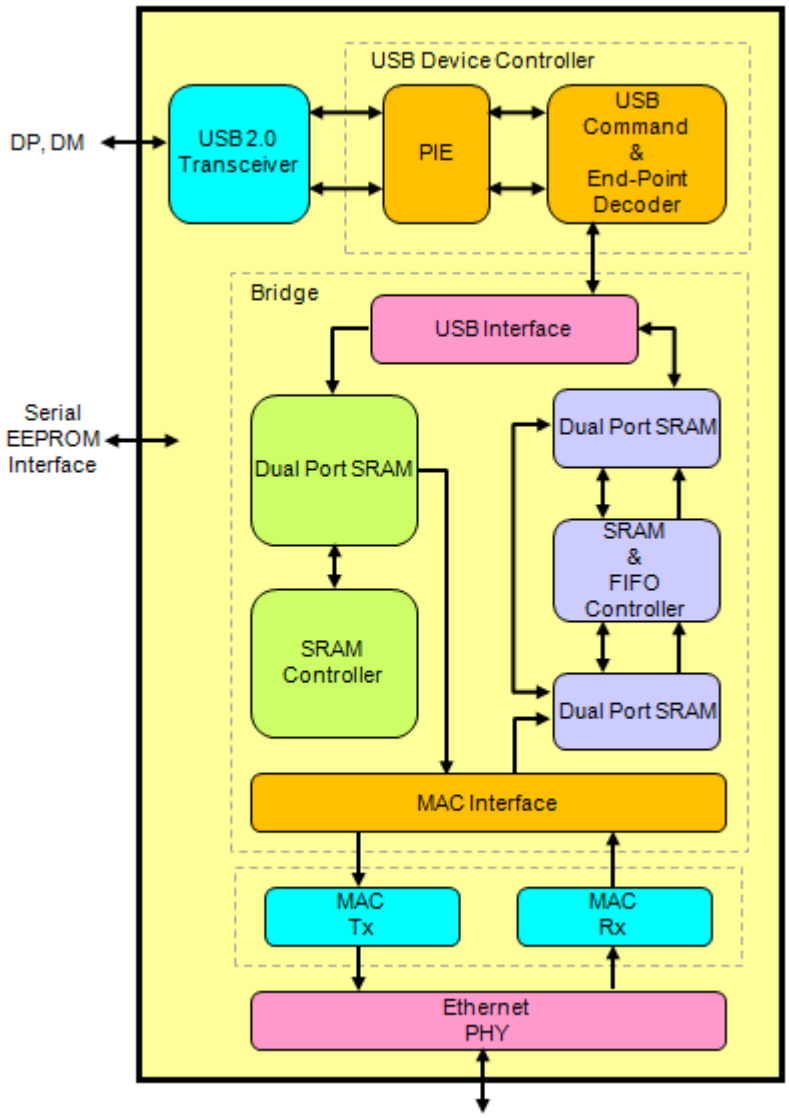
This device has been specifically designed to provide a simple solution to communicate with Ethernet applications. This is accomplished by its highly integrated functionality.

It is ideal for LAN (Local Area Network) applications. It provides internal buffering to enable parallel operations from USB ports on the host side, and MAC ports on the Ethernet side.

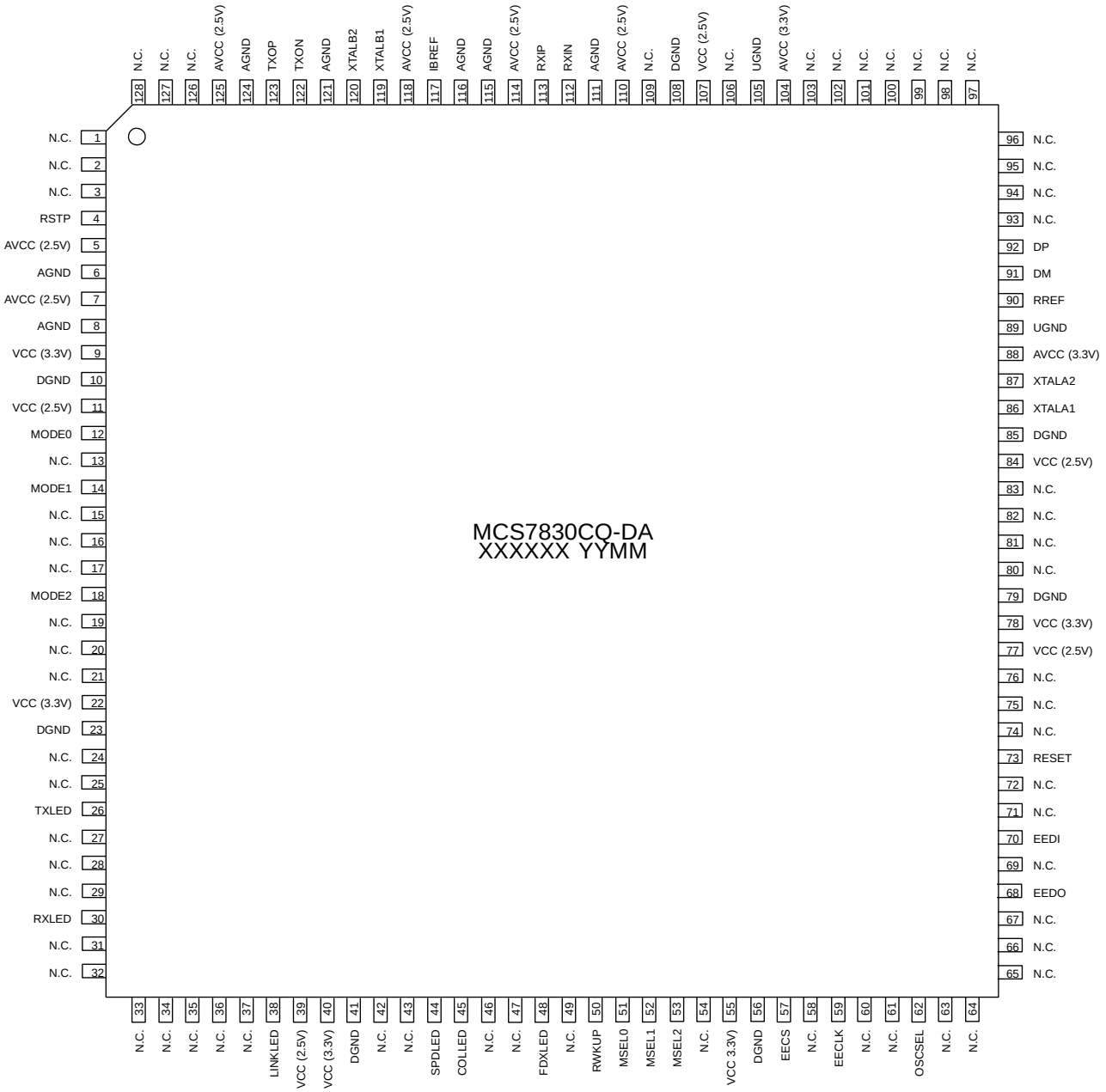
It also provides a serial interface for an EEPROM for storing the MAC-ID, VID, PID, and other configurable settings.

Ordering Information		
Commercial Grade (0 °C to +70 °C)		
MCS7830CQ-DA	128-LQFP	RoHS
MCS7830CV-DA	80-TQFP	RoHS

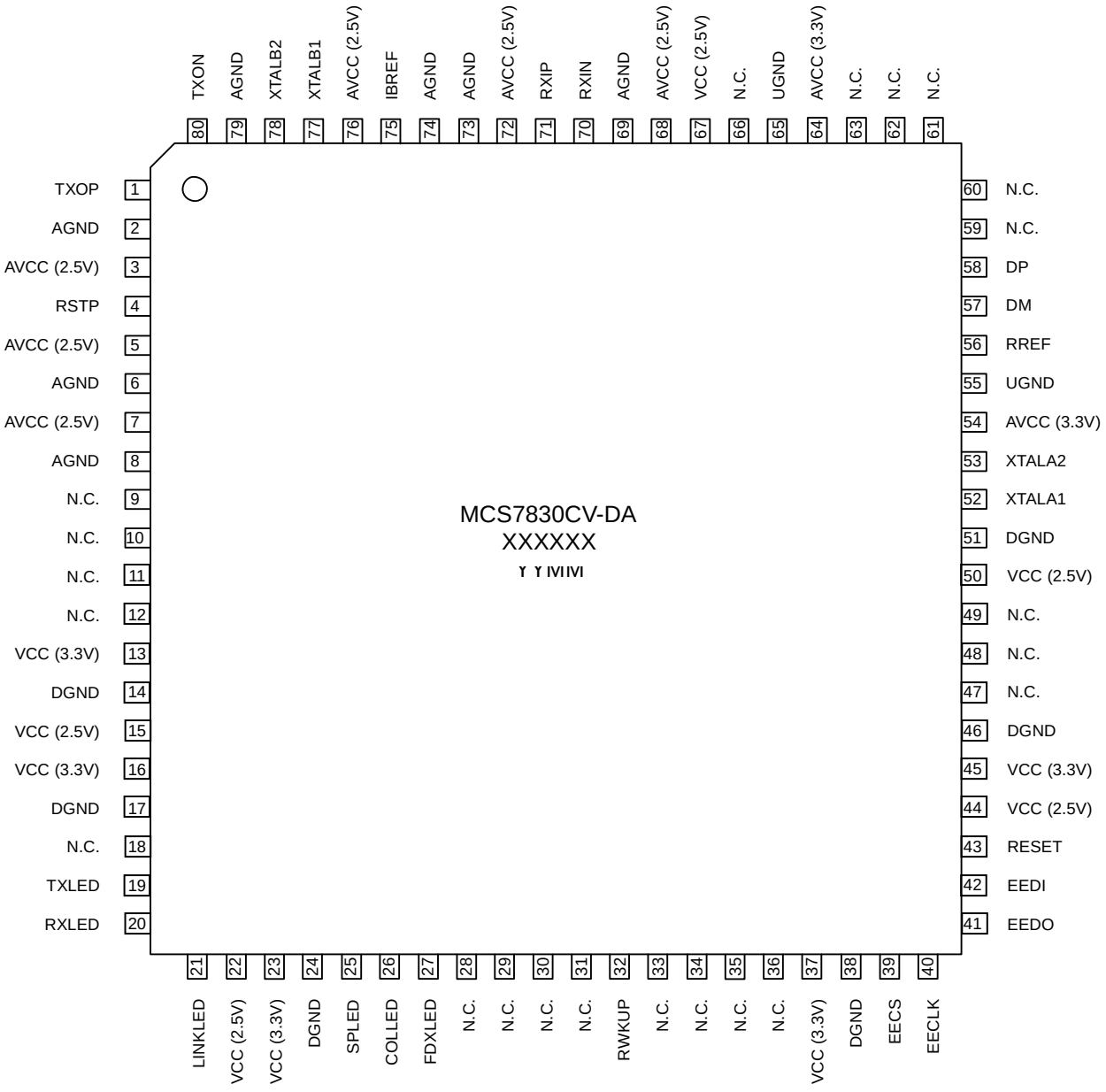
Block Diagram



Pin-Out Diagram (128-Pin Package)



Pin-Out Diagram (80-Pin Package)



Pin Assignments

Name	128-Pin	80-Pin	Type	Description
nRSTP	4	4	I	10/100 Ethernet PHY Power-On Reset input (Active Low).
MODE 0	12	-	I	***10/100 Operation Mode Select Pins (MODE <2:0>)*** 0 = Auto-Negotiation Enable with all capabilities. 1 = Auto-Negotiation with 100 Base-TX. 2 = Auto-Negotiation with 10 Base-T, FDX/HDX. 3 = Reserved. 4 = Manual selection of 100 Base-TX, FDX. 5 = Manual selection of 100 Base-TX, HDX 6 = Manual selection of 10 Base-T, FDX 7 = Manual selection of 10 Base-T, HDX This pin is internally pulled to GND.
MODE 1	14	-	I	See MODE 0 above. This pin is internally pulled to GND.
MODE 2	18	-	I	See MODE 0 Above. This pin is internally pulled to GND.
TXLED	26	19	O	Transmitting Frame signal (Active Low). This pin goes low when transmission occurs on the 10/100 interface. This signal would be seen as toggling in low data traffic conditions. In heavy traffic conditions, the user can see this as continuously glowing/toggling at a quick rate.
RXLED	30	20	O	Receiving Frame signal (Active Low). This pin goes low when receive occurs on the 10/100 interface. This signal would be seen as toggling in low data traffic conditions. In heavy traffic conditions, the user can see this as continuously glowing/toggling at a quick rate.
LINKLED	38	21	O	Link Status signal (Active High). This pin goes high when the 10/100 link is detected. Once the link is active, this pin toggles to indicate a data transfer when traffic occurs on the 10-/100 interface.
SPDLED	44	25	O	Speed Indicator for 10 / 100 Ethernet High for 100 Mbps.
COLLED	45	26	O	Collision Detected (Active Low). This pin goes low when a collision is detected on the 10/100 interface. Collisions occur in half-duplex mode of operation with traffic load on the 10/100 interface. This signal would be seen as toggling in low data traffic conditions. In heavy traffic conditions, the user can see this as continuously glowing/toggling at a quick rate.
FDXLED	48	27	O	Full Duplex mode (Active High). This pin goes high when the 10/100 interface is in full duplex mode.

Name	128-Pin	80-Pin	Type	Description
MSEL 0	51	-	I	***Mode Select Signals (MSEL<2:0>)*** 0 = Normal 1 = Functional block test 2 = USB 10/100 ATPG test mode 3 = USB BIST 10/100 functional test mode 4 = Reserved 5 = Reserved 6 = Memory Bist 7 = External 10/100 PHY mode This pin is internally pulled to GND.
MSEL1	52		I	See MSEL 0 above. This pin is internally pulled to GND.
MSEL 2	53	-	I	See MSEL 0 above. This pin is internally pulled to GND.
EECS	57	39	O	External EEPROM Chip Select (Active high). This pin enables the External EEPROM to load the Ethernet configuration data.
EECLK	59	40	O	External EEPROM clock (<1 MHz).
EEDO	68	41	O	Data output from MCS7830 to external EEPROM. Ethernet MAC will use this pin to serially write op codes and addresses into the serial EEPROM.
EEDI	70	42	I	Data output from external EEPROM to MCS7830. Ehternet MAC will read the contents of the EEPROM serially through this pin.
nRESET	73	43	I	System (USB) reset (active low).
XTALA1	86	52	I	Crystal, or External USB-2.0 Clock Input. (12/30 MHz)
XTALA2	87	53	O	Crystal Output.
OSCSEL	62	-	I	XTALA Crystal Clock Select Pin (Internal Pull-Down). 0 = 12 MHz Clock, 1 = 30 MHz Clock.
RREF	90	56	O	USB PHY Reference Signal. External resistor to GND is required.
DM	91	57	I/O	USB-2.0 PHY Data Minus pin.
DP	92	58	I/O	USB-2.0 PHY Data Plus pin.
RXIN	112	70	I	Twisted-Pair Input (RXIN, RXIP). Differential input pair for either 100 BASE-TX or 10 BASE-T reception.
RXIP	113	71	I	See RXIN.
IBREF	117	75	I	10/100 Ethernet PHY Transmit Reference. Connected to Analog Ground through resistor
XTALB1	119	77	I	10/100 Ethernet PHY 25 MHz Crystal Clock Input.
XTALB2	120	78	O	Crystal Output.
TXON	122	80	O	Twisted-Pair Output (TXON, TXOP), Differential driver pair for Ethernet PHY 100 BASE-TX or 10 BASE-T transmission.
TXOP	123	1	O	See TXON.
RWKUP	50	32	I	This pin can be used to initiate a host wake-up form the suspend state. Refer to the application schematic for system interface details.

Name	128-Pin	80-Pin	Type	Description
AVCC (2.5V)	5, 7, 110, 114, 118, 125	3, 5, 7, 68, 72, 76	Pwr	Analog 2.5V supply.
VCC (2.5V)	11, 39, 77, 84, 107	15, 22, 44, 50, 67	Pwr	Digital 2.5V supply.
AVCC (3.3V)	88, 104	54, 64	Pwr	Analog 3.3V supply.
VCC (3.3V)	9, 22, 40, 55, 78	13, 16, 23, 37, 45	Pwr	Digital 3.3V supply.
AGND	6, 8, 111, 115, 116, 121, 124	2, 6, 8, 69, 73, 74, 79	Pwr	Analog GND pins.
DGND	10, 23, 41, 56, 79, 85, 108	14, 17, 24, 38, 46, 51	Pwr	Digital GND pins.
UGND	89, 105	55, 65	Pwr	USB GND pins.
RESERVED PINS	1-3, 13, 15-17, 19-21, 24, 25, 27-29, 31-37, 42-43, 46, 47, 49, 54, 58, 60, 61, 63-67, 69, 71, 72, 74-76, 80-83, 93-103, 106, 109, 126-128	9-12, 18, 28-31, 33-36, 47-49, 59-63, 66		These pins are to be left as no-connects at the system level. Do not connect these pins to any other pins. All of these pins are reserved for internal test bus, etc. and are not available to customers.

Functional Description

The MCS7830 is ideal for Local Area Network (LAN) applications. This is accomplished by its highly integrated functionality by providing internal buffering to enable parallel operations from USB ports on the host side, and MAC port on the Ethernet side.

iSerial Feature: By writing a unique serial number into the EEPROM, each of the MCS7830 products can be uniquely identified by the Windows OS. The iSerial feature is supported with the EEPROM only.

Locally Administered Network Address: Every Ethernet card has a unique physical address assigned to it when it is manufactured. In some cases the user may need to change this address. This can be accomplished by assigning a "Locally Administered Network Address" to the device by the network administrator, thereby overriding the "Universally Administered Address." Refer to the application note for more details.

Lower Power Mode Support: The MCS7830 controller supports low power mode by taking less than 100 mA in Unconfigured mode and less than or equal to 2.5 mA in Suspend mode. The remote wake-up (Wake on LAN) feature and low power mode are mutually exclusive features. By default, low power mode is enabled. Remote wake-up can be enabled through system level component selection. Refer to application notes for more details.

Suspend / Wake up from Standby: The MCS7830 can wake up from Suspend/Standby using either magic packets, or by implementing external wake up switch. On wake-up, the device can resume back to the original operating mode from which it entered Suspend.

Wake up through magic packets is supported when the remote wake-up (Wake on LAN) feature is enabled. Similarly, wake-up through and external switch can be supported when low power mode is enabled.

MII Interface: The MCS7830 128-pin package supports and MII interface for use with an external Ethernet PHY. Refer to the MII application note of the MCS7830 for more details.

USB-2.0 Interface: This device has a USB-2.0 PIE (Parallel Interface Engine), allowing both High-Speed (HS) and Full Speed (FS) operation, either of which is able to control all USB transactions. CRC checking and generation is done in the PIE block only. The USB Control and Endpoint Decoder blocks will decode all the standard and vendor specific commands. The PIE and USB transceiver, which provide the hardware interface to the USB cable, together comprise the USB Engine. This device supports all standard USB commands, as well as five vendor specific commands.

The USB device controller uses one interface, one configuration, and three endpoints (Bulk-Out, Bulk-In and Interrupt-In) apart from Endpoint-0. The details of the device descriptor, configuration descriptor, interface descriptor, and endpoint descriptors are explained below.

Device Descriptor

Offset	Field	Size	Value	Description
0	Length	1	0x12	Device Descriptor
1	Descriptor Type	1	0x01	DEVICE
2	USB	2	0x0200	USB Release Number
4	DeviceClass	1	0xFF	Class Code
5	Device Sub class	1	0x00	Subclass Code
6	Device Protocol	1	0xFF	Protocol Code
7	Max Packet Size (0)	1	0x40	Max Packet Size For Endpoint-0
8	ID Vendor	2	0x9710	Vendor ID
10	I Product	2	0x7830	Product ID
12	Device	2	0x0100	Device Release Number
14	Manufacturer	1	0x00	Index of string descriptor for the Manufacturer
15	Product	1	0x00	Index of string descriptor for the Product
16	Serial Number	1	0x00	Index of string descriptor for the Serial Number
17	Num Configurations	1	0x01	Number of Possible Configurations

Configuration Descriptor 0

Offset	Field	Size	Value	Description
0	Length	1	0x09	Descriptor Size In Bytes
1	Descriptor Type	1	0x02	CONFIGURATION
2	Total Length	2	0x0027	Size of all data returned for this configuration in Bytes
4	Num Interfaces	1	0x01	Number of interfaces the configuration supports
5	Configuration Value	1	0x01	Identifier for Set_Configuration and Get_Configuration
6	Configuration	1	0x00	Index of string descriptor for the Configuration
7	Attributes	1	0xA0	Self/Bus Power and Remote Wakeup settings
8	Max Power	1	0x00FA	Bus Power Required

Interface Descriptor 0

Offset	Field	Size	Value	Description
0	Length	1	0x09	Descriptor Size In Bytes
1	Descriptor Type	1	0x04	INTERFACE
2	Interface Number	1	0x00	Number Identifying this Interface
3	Alternate Setting	1	0x00	Value used to select an alternate setting
4	Num End Points	1	0x03	Number of endpoints supported, except Endpoint-0
5	Interface Class	1	0xFF	Class Code
6	Interface Sub Class	1	0x00	Subclass Code
7	Interface Protocol	1	0xFF	Protocol Code
8	Interface	1	0x00	Index of string descriptor for the Interface

Endpoint-1 Descriptor Bulk-In

Offset	Field	Size	Value	Description
0	Length	1	0x07	Descriptor Size in Bytes
1	Descriptor Type	1	0x05	ENDPOINT
2	Endpoint Address	1	0x81	Endpoint Number and Direction
3	Attributes	1	0x02	Transfer Type Supported
4	Max Packet Size	2	0x0040 0x0200	Maximum Packet Size Supported (Full Speed) (High Speed)
5	Interval	1	0xFF	Polling Interval

Endpoint-2 Descriptor Bulk-Out

Offset	Field	Size	Value	Description
0	Length	1	0x07	Descriptor Size in Bytes
1	Descriptor Type	1	0x05	ENDPOINT
2	Endpoint Address	1	0x02	Endpoint Number and Direction
3	Attributes	1	0x02	Transfer Type Supported
4	Max Packet Size	2	0x0040 0x0200	Maximum Packet Size Supported (Full speed) (High speed)
5	Interval	1	0xFF	Polling Interval

Endpoint-3 Descriptor Interrupt-In

Offset	Field	Size	Value	Description
0	Length	1	0x07	Descriptor Size in Bytes
1	Descriptor Type	1	0x05	ENDPOINT
2	Endpoint Address	1	0x83	Endpoint Number and Direction
3	Attributes	1	0x03	Transfer Type Supported
4	Max Packet Size	2	0x0010	Maximum Packet Size Supported
5	Interval	1	0x01	Polling Interval

Data Flow (USB to Ethernet MAC/PHY)

Endpoint-2 (Bulk-Out) is in charge of sending the USB packets to Ethernet. An Ethernet packet is concatenated from multiple USB packets (64 Bytes in Full-Speed, and 512 Bytes in High-Speed). The end of the Ethernet packet is indicated with either a partial packet, or Zero-Length packets in this pipe. The Ethernet transmit status is stored in the internal FIFO of the Bridge. When the Bulk-Out endpoint is accessed, if space is available in the internal SRAM of the Bridge, data in the USB data stage is transferred to SRAM and ACK is returned. If SRAM is not free, then NAK is returned.

Dual-Port SRAM is used in this path (data flow from USB to Ethernet MAC). The SRAM Controller stores each individual USB packet (64 Bytes in Full Speed and 512 Bytes in High Speed) in internal SRAM. When the Endpoint Decoder signals *End Of Packet*, a complete Ethernet packet is stored in SRAM. The SRAM Controller then informs the Ethernet MAC to transmit this packet. Approximately three Ethernet packets of maximum size can be stored in SRAM. If the SRAM is full, then the controller will inform the Endpoint Decoder that SRAM is full, and the Endpoint Decoder will return NAK, if accessing the Bulk-Out endpoint is invoked. Thus additional USB packets won't be written into SRAM until it has free space.

Data Flow (Ethernet MAC/PHY to USB)

Endpoint-1 (Bulk-In) is in charge of sending received Ethernet packets to the USB host. The Ethernet packets received from the Ethernet MAC are stored in the internal SRAM of the Bridge. If at least one Ethernet frame is available in the SRAM, then the Bridge informs readiness to the USB Device Controller for transmission. If data is not ready in the SRAM for transmission, then NAK is returned to the USB host.

An Ethernet packet will be split to multiple USB packets (packet size is 64 Bytes in Full-Speed and 512 Bytes in High-Speed). The end of the Ethernet packet is indicated by a partial packet (less than 64 Bytes in Full-Speed and less than 512 Bytes in High-Speed) or a Zero-Length data transfer in this pipe. The Ethernet received status is appended to the data as the last Byte. While accessing this endpoint, if SRAM is full or any packet is inside, the data in SRAM is returned in the USB data stage. If ACK is received from the USB host, the next packet available in the SRAM will be transmitted in the next data stage. If no response or NAK is received from the USB host, then the same packet will be re-transmitted.

Received Ethernet packets are stored in the internal Dual-Port SRAM. A total of five Ethernet packets of maximum size can be stored in SRAM. If more than the maximum packet counts are received, then the subsequent incoming Ethernet packets will be discarded in the case of Half-Duplex mode. In the case of Full-Duplex mode, the Ethernet MAC stops receiving Ethernet packets from the PHY by using the *PAUSE* frame mechanism.

The FIFO Controller will load data from SRAM into the internal FIFO, and inform the USB Endpoint Decoder that data is ready. Before the FIFO Controller does this, any USB access to the Bulk-In endpoint will return NAK. If an Ethernet packet is being received and loaded into SRAM while the FIFO Controller is moving data from SRAM to the FIFO, the SRAM bus is shared by the controller for write and read operations in alternate cycles.

The 8-bit status of the Receiver is appended to the data as the last Byte in each Ethernet frame. The receiver status vector definition is as follows:

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Reserved		RX Ok	Large Frame	FCS Error	Alignment Error	Length Error	Short Frame

Bit	Description
0	0: Indicates the received frame length is greater than or equal to 64 Bytes and less than 1518 Bytes. It is a normal frame. 1: Indicates the received frame length is less than 64 Bytes (short frame).
1	0: Indicates the received frame does not have a length error. Received data length in the frame is exactly matched with the L/T field of the Ethernet frame. 1: Indicates the received frame has a length error. Received data length is not matched with the L/T field of the Ethernet frame.
2	0: Indicates there is no alignment error in the received frame. It has received an even number of nibbles. 1: Indicates there is an alignment error.
3	0: Indicates there is no CRC error. Received CRC is matched with the CRC calculated. 1: Indicates a CRC error.
4	0: Indicates the received frame is a normal frame. 1: Indicates the received frame is a large frame whose length is >1518 Bytes.
5	0: Indicates the received frame is not correct. 1: Indicates the received frame is a correct frame.
[7:6]	Reserved

So the status vector received as a last Byte at the end of each Ethernet frame is 0x20 if it is a correct frame.

Status Flow (Ethernet to USB):

Endpoint-3 (Interrupt-In) is in charge of returning the current Ethernet transfer status each polling interval. When this endpoint is accessed, eight words of data are returned. These eight words contain the status vectors of eight consecutive Ethernet frames transmitted from USB to Ethernet. These vectors describe frames pending information in the SRAM (from Ethernet to USB path), 10/100 Link Status etc. as explained below.

Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8
1/0	1/0	1/0	1/0	1/0	1/0	0	0

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	0	0	1/0	1/0	1/0	1/0

Bit	Description
0	0: Indicates the Ethernet frame transmitted is not correct. 1: Indicates the transmitted Ethernet frame is OK.
1	0: Indicates the number of retries is less than or equal to 16. 1: Indicates the number of retries is more than 16.
2	0: Indicates collision occurred before receiving 64 Bytes. 1: Indicates collision occurred after receiving 64 Bytes.
3	0: Normal 1: Indicates that the packet is aborted because of excessive deferral (if number of clock cycles waited to transmit a packet is (TX CLK) more than 6072.)
[9:4]	Reserved, (all zeros).
10	FULL_DUPLEX_EN: Indicates Full-Duplex or Half-Duplex operation. 0: Half-Duplex 1: Full-Duplex
11	0: Indicates 10 Mbps Ethernet speed. 1: Indicates 100 Mbps Ethernet speed.
12	MIIM_ INTERRUPT Used as interrupt pin when an external PHY is connected.
13	MIIM_LINK Indicates the status of the link when an external PHY is used.
14	0: Indicates least significant four bits do not indicate valid status. 1: Indicates the least significant four bits have a valid TX status.
15	0: Frames are not available in the Single-Port SRAM. 1: Indicates frames are pending in the Single-Port SRAM which have been received from the Ethernet RX.

Whenever the Interrupt-In endpoint is selected, eight status vectors are available in the FIFO. After reading these eight words, software is supposed to verify bit-15 and bit-14 of each word. If bit-15 is ‘1’ that indicates some frames are pending in the SRAM, if bit-14 is ‘1’ it indicates the least significant four bits of the word are a valid TX status vector. If bit-15 and bit-14 are both zeros, then the status vector should be ignored.

Control Path
Endpoint-0 is in charge of responding to USB Standard commands, and Vendor Specific commands. Setting of the Ethernet registers is also done through this endpoint. These commands are shown below.

Commands:
This device supports nine Standard USB commands, and five Vendor Specific commands. They are as follows:

USB Standard Commands:
- SET ADDRESS
- CLEAR FEATURE
- GET STATUS
- GET CONFIGURATION
- SET CONFIGURATION
- GET DESCRIPTOR
- SET FEATURE
- GET INTERFACE
- SET INTERFACE

The format of the Standard Commands is per the USB-1.1 / USB-2.0 Specifications.

Vendor Specific Commands:
- VENDOR SPECIFIC WRITE (Burst Write)
- VENDOR SPECIFIC READ (Burst Read)
- VENDOR SPECIFIC WRITES WITH MASK (write with mask)
- VENDOR SPECIFIC EEPROM ENABLE (for programming purposes)
- VENOR SPECIFIC EEPROM WRITE

Vendor Specific Commands:

VENDOR SPECIFIC WRITE (Burst Write)
Vendor Specific command to write into the HIF Registers of the Ethernet MAC.

Bm_Request	8'b 0100_0000
Brequest	8'b 0000_1101
W_Value	16'b 0000_0000_0000_0000
W_Index	Starting Address of Register Index
W_Length	Number of Bytes

W_Index Field is the starting address of the registers to be written.

W_Length field is the number of Bytes to be transferred in the data stage.

W_Value should be "0". If the W_Value field is non-zero, and the register address specified in the W_ Index is not available, the Device will respond with a *"STALL"*.

In the Data stage of the command, all the Bytes will be transmitted.

VENDOR SPECIFIC READ (Burst Read)
Vendor Specific command to read from the HIF Registers of the Ethernet MAC.

Bm_Request	8'b 1100_0000
Brequest	8'b 0000_1110
W_Value	16'b 0000_0000_0000_0000
W_Index	Starting Address of Register Index
W_Length	Number of Bytes

W_Index Field is the starting address of the registers to be read.

W_Length field is the number of Bytes to be transferred in the data stage.

W_Value should be "0". If the W_Value field is non-zero, and the register address specified in the W_ Index is not available, the Device will respond with a *"STALL"*.

VENDOR SPECIFIC WRITES WITH MASK (write with mask)

Bm_Request	8'b 0100_0000
Brequest	8'b 0000_1111
W_Value	MSB = Mask bit value LSB = value to be written
W_Index	Address of Register
W_Length	16'b 0000_0000_0000_0000

The MSB Byte in the W_Value gives the bits to be modified, and the LSB Byte gives the Value to be written into the bits specified by the mask value.

W_index gives the Byte to be modified as specified in W_value.

W_Length should be 16'h0000.

If the W_Length is not "0", and the register specified in the W_index is not available, the device will respond with *"STALL"*.

Serial EEPROM Support

The serial interface is used to provide access to an external EEPROM. The Ethernet MAC automatically loads the Device-ID from the EEPROM after Power-On Reset. It can also be used to program the EEPROM through the USB port.

VENDOR SPECIFIC EEPROM ENABLE (for programming purposes)

This command is used to enable the EEPROM for programming purposes.

Bm_Request	8'b 0100_0000
Brequest	8'b 0001_0000
W_Value	16'b 0000_0000_0000_0000
W_Index	16'b 0000_0000_0000_0000
W_Length	16'b 0000_0000_0000_0000

VENOR SPECIFIC EEPROM WRITE

Sends six Bytes of ETHERNET Address to EEPROM.

Bm_Request	8'b 0100_0000
Brequest	8'b 0001_0001
W_Value	16'b 0000_0000_0000_0000
W_Index	16'b 0000_0000_0000_0000
W_Length	16'b 0000_0000_0000_0006

EEPROM Content Layout

The contents of the EEPROM are listed in the following table.

Byte Offset	Number of Bytes	Name	Description
[1:0]	2	EE Check	EEPROM present check. Value = 0x9710.
[7:2]	6	MAC ID	To store the Ethernet physical address.
[9:8]	2	VID	Vendor ID = 0x9710.
[11:10]	2	PID	Product ID = 0x7830
[13:12]	2	Release Number	Release number = 0x0002.
[15:14]	2	Language ID	Language ID = 0x0409
[63:16]	48	Manufacturer ID	“MosChip Semiconductor”
[99:64]	36	Product Name	“USB-MAC Controller”
[115:100]	16	Serial Number	Serial Number.

Notes:

1. The serial number can be the same as the MAC ID.
2. A total of 116 bytes of data will be stored in the EEPROM.
3. Data from the EEPROM can be read at any time, not only at power on reset.
4. If the EEPROM is not present, details hard-coded in the design would be effective.

Example EEPROM Contents Layout

Location	Hex	ASCII	Location	Hex	ASCII	Location	Hex	ASCII	Location	Hex	ASCII
0	10		31	00		62	20	Space	93	00	
1	97		32	53	S	63	00		94	6C	l
2	00		33	00		64	55	U	95	00	
3	50		34	65	e	65	00		96	65	e
4	C5		35	00		66	53	S	97	00	
5	00		36	6D	m	67	00		98	72	r
6	47		37	00		68	42	B	99	00	
7	B5		38	69	i	69	00		100	20	Space
8	10		39	00		70	2D	-	101	00	
9	97		40	63	c	71	00		102	00	
10	30		41	00		72	4D	M	103	50	
11	78		42	6F	o	73	00		104	C5	
12	02		43	00		74	41	A	105	00	
13	00		44	6E	n	75	00		106	47	
14	09		45	00		76	43	C	107	B5	
15	04		46	64	d	77	00		108	20	Space
16	4D	M	47	00		78	20	Space	109	00	
17	00		48	75	u	79	00		110	20	Space
18	6F	o	49	00		80	43	C	111	00	
19	00		50	63	c	81	00		112	20	Space
20	73	s	51	00		82	6F	o	113	00	
21	00		52	74	t	83	00		114	20	Space
22	63	c	53	00		84	6E	n	115	00	
23	00		54	6F	o	85	00				
24	68	h	55	00		86	74	t			
25	00		56	72	r	87	00				
26	69	i	57	00		88	72	r			
27	00		58	20	Space	89	00				
28	70	p	59	00		90	6F	o			
29	00		60	20	Space	91	00				
30	20	Space	61	00		92	6C	l			

Description of Programmable Registers (HIF Registers)

HIF registers are the Host Interface registers, and these are a part of the Ethernet MAC design. The registers are written into and read from the bridge side by using the WR_DB and RD_DB signals. The bridge uses a 4-bit address bus 'ADDRESS_DB'. On the Ethernet MAC side (receiver), the HIF Registers are read using a 3-bit address bus which is used to access the first eight registers. A "HIF_ADDRESS_RD" signal is used to validate the address. The Ethernet MAC receiver accesses these registers every time it receives a multi-cast or a broadcast frame.

To check whether the received multi-cast frame is valid, the Ethernet MAC does something called "hash filtering". In hash filtering, the CRC-32 (cyclic redundancy check) value is used. The six most significant bits are taken from the 32 bits of the CRC. The Ethernet MAC uses the higher three bits of the six bits as "HIF_ADDRESS". Three bits can have values from '000' to '111', which is a total of eight numbers. So the first eight registers are accessible by the Ethernet MAC. When the Ethernet MAC receives the contents of the register addressed by it on the "HIF_DATA_OUT" (8 bits wide), it uses the remaining three bits of the six most significant bits for bit selection within the Byte.

The bits in the HIF Registers are arranged in an 8x8 matrix. The Ethernet MAC assumes the driver knows the multi-cast addresses which are to be accepted. Depending on the multi-cast address, it calculates the 32-bit CRC, and uses the six most significant bits to arrange those values in such a way that the Ethernet MAC can address any particular bit in the 8x8 matrix.

For the addresses the driver wants to accept, it writes a '1' into those bit positions in the 8x8 matrix. The Broadcast frame '1111_1111_1111' is an all '1' address, and is always accepted.

The address and the number of the HIF Registers are not the same. The address for Register-1 is 0x0000; Register-2 is 0x0001; and so on.

HIF Registers 1 through 8 are used for hash filtering.

HIF Registers 9 & 10 are used for IPG & IPG1 (Inter Packet Gap). This is configurable (refer to the 802.3 specification).

HIF Registers 11 & 12 are used as the MIIM_DR data register (data to be written into MIIM (PHY)).

HIF Registers 13 & 14 are used as the MIIM_CR command register (commands for accessing the MIIM registers).

HIF Register 15 is the MIIM (PHY) Configuration Register.

HIF Registers 16 through 21 hold the Ethernet MAC Address (Station Address).

HIF Register Map

The following table lists the HIF registers

Name	Address	Change	Default	Description
HIF1	0	R/W	0	Multicast address byte 0.
HIF2	1	R/W	0	Multicast address byte 1.
HIF3	2	R/W	0	Multicast address byte 2.
HIF4	3	R/W	0	Multicast address byte 3.
HIF5	4	R/W	0	Multicast address byte 4.
HIF6	5	R/W	0	Multicast address byte 5.
HIF7	6	R/W	0	Multicast address byte 6.
HIF8	7	R/W	80	Multicast address byte 7.
HIF9	8	R/W	18	Configurable inter-packet gap (IPG).
HIF10	9	R/W	10	Configurable inter-packet gap (IPG).
HIF11	10	R/W	0	Hold the least significant byte of the data read/ write from the Ethernet MAC PHY registers.
HIF12	11	R/W	0	Hold the most significant byte of the data read/ write from the Ethernet MAC PHY registers.
HIF13	12	R/W	0	Hold the command for the MIMM.
HIF14	13	R/W	0	Hold the command for the MIMM.
HIF15	14	R/W Except bit 3	0	Control register.
HIF16	15	R/W	0	MAC address.
HIF17	16	R/W	50	MAC address.
HIF18	17	R/W	C5	MAC address.
HIF19	18	R/W	0	MAC address.
HIF20	19	R/W	47	MAC address.
HIF21	20	R/W	B5	MAC address.
HIF22	21	R/W	0	Used as a frame drop counter.
HIF23	22	R/W	0	Used for pause threshold.
HIF24	23	RO	0	EEPROM status.

Note: All default values are in hexidecimal format. All registers are 8-bits wide.

Multicast Address Registers (HIF_REG1 to HIF_REG8):

The Ethernet MAC receiver accesses these registers every time it receives a multi-cast or a broadcast frame. To check whether the received multi-cast frame is valid, the Ethernet MAC does something called “hash filtering”. In hash filtering, the CRC-32 (cyclic redundancy check) value is used. The six most significant bits are taken from the 32 bits of the CRC. The Ethernet MAC uses the higher three bits of the six bits as “HIF_ADDRESS”. Three bits can have values from ‘000’ to ‘111’, which is a total of eight numbers. So the first eight registers are accessible by the Ethernet MAC. When the Ethernet MAC receives the contents of the register addressed by it on the “HIF_DATA_OUT” (8 bits wide), it uses the remaining three bits of the six most significant bits for bit selection within the Byte.

The bits in the HIF Registers are arranged in an 8x8 matrix. The Ethernet MAC assumes the driver knows the multi-cast addresses which are to be accepted. Depending on the multi-cast address, it calculates the 32-bit CRC, and uses the six most significant bits to arrange those values in such a way that the Ethernet MAC can address any particular bit in the 8x8 matrix.

For the addresses the driver wants to accept, it writes a ‘1’ into those bit positions in the 8x8 matrix. The Broadcast frame ‘1111_1111_1111’ is an all ‘1’ address, and is always accepted.

Address	Field	HW	SW	Default	Description
0x00	Multi-cast 0	R	R/W	0x00	Multi-cast Address. Byte 0
0x01	Multi-cast 1	R	R/W	0x00	Multi-cast Address. Byte 1
0x02	Multi-cast 2	R	R/W	0x00	Multi-cast Address. Byte 2
0x03	Multi-cast 3	R	R/W	0x00	Multi-cast Address. Byte 3
0x04	Multi-cast 4	R	R/W	0x00	Multi-cast Address. Byte 4
0x05	Multi-cast 5	R	R/W	0x00	Multi-cast Address. Byte 5
0x06	Multi-cast 6	R	R/W	0x00	Multi-cast Address. Byte 6
0x07	Multi-cast 7	R	R/W	0x00	Multi-cast Address. Byte 7

Inter-Packet Gap Registers (HIF_REG9 & HIF_REG10):

These registers hold the IPG (Inter-Packet Gap) values. This is the amount of time between the end of the last transmission and the start of the next one. The registers hold the number of clock cycles to wait. These values must be multiplied by the clock period to obtain the actual amount of time to wait.

Address	Field	HW	SW	Default	Description
0x08	IPG	R/W	R/W	0x18	Inter Packet Gap of 24 clocks
0x09	IPG1	R/W	R/W	0x10	Inter Packet Gap of 16 clocks

PHY Data Registers
(HIF_REG11 & HIF_REG12):
These Registers hold the data read/written from/to the Ethernet PHY. Software sets these registers when it writes to the PHY. Hardware sets these registers when it reads data from the PHY.

Address	Field	HW	SW	Default	Description
0x0A	PHY Data (low)	R/W	R/W	0x00	Holds low order byte of PHY.
0x0B	PHY Data (high)	R/W	R/W	0x00	Holds high order byte of PHY.

PHY Command Registers

These registers each hold part of the Command for the MIIM. These registers are used to perform read/write operations from/to the external PHY.

HIF_REG13:

Address	Field	HW	SW	Default	Description
0x0C	PHY Command	R	R/W	0x00	Opcode

Bit-7	Bit-[6:5]	Bit-[4:0]
Reserved	Opcode to read/write from/to PHY Reg.	Address of the PHY being accessed
	00 not defined 01 write operation 10 read operation 11 not defined	

HIF_REG14:

Address	Field	HW	SW	Default	Description
0x0D	PHY Command	R/W	R/W	0x00	Status and Control

Bit-7	Bit-6	Bit-5	Bit-[4:0]
Pending Flag	Ready Flag	not used	Address of the register within the Ethernet PHY being accessed.

Bit	Function	Description
[4:0]	Ethernet PHY Address	The address of the registers in the ETHERNET PHY.
5	Unused	Unused
6	Ready Flag	The Ethernet MAC Controller sets this bit after processing the Pending command.
7	Pending Flag	0: No command was received from the host. 1: A new command was received from the host, and processed by the Ethernet MAC.

Write Process:

It is a two stage process. The Host writes the command into registers 13/14 and the data into registers 11/12. The Command consists of Ethernet PHY-address/reg-address/opcde. When the Host sends a new command, it sets Bit-7 *(Pending),* and resets Bit-6 *(Ready)*.

After the command is processed, the Ethernet MAC Controller asserts Bit-6 *(Ready)*. The Host polls this register after a fixed time to check this bit, if found ready, it understands that the command was processed.

Read Process:

Same as for write, except that the data read from the Ethernet PHY is stored in the HIF_REG11/12, and the Host reads this data after it finds the *Ready* flag set.

Configuration Register (HIF_REG15):

This register's contents can be read by the Ethernet MAC, and it can be Read/Written by software via the Bridge.

Address	Field	HW	SW	Default	Description
0x0E	Configuration	R	R/W	0x00	Configuration Options

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Cfg Override	Speed 100	Full Duplex Enable	Reserved "0"	TX Enabled	Sleep Mode	Multi-cast Mode	Promiscuous

Bit	Description
0	0: Indicates it is not in promiscuous mode. 1: Indicates it is in promiscuous mode, which can accept all frames irrespective of the address.
1	0: Indicates it is not in multi-cast mode. 1: Indicates it is in multi-cast mode, and accepts all multi-cast frames irrespective of multi-cast address, and it does normal filtering for uni-cast frames.
2	0: Indicates the device is not in Sleep Mode. 1: Indicates the device is in Sleep Mode, except Ethernet MAC RX.
3	0: Indicates Ethernet MAC TX is disabled. 1: Indicates Ethernet MAC TX is enabled.
4	Reserved, always "0".
5	0: Indicates Ethernet MAC is working in Half-Duplex mode. 1: Indicates Ethernet MAC is working in Full-Duplex mode.
6	0: Indicates 10 Mbps Ethernet speed. 1: Indicates 100 Mbps Ethernet speed.
7	0: Speed/Duplex bits are set based on the current status of the LED pins for speed/duplex from Ethernet PHY. 1: Speed/Duplex bits used by Ethernet MAC / Bridge are from the HIF register bits HIF_REG15[6-5].

MAC Address Registers
HIF_REG16 to HIF_REG21:

The Ethernet MAC Address (Station Address) is 46 bits + 2 bits indicating multi-cast/uni-cast, and local/global. Six HIF Registers (HIF_REG16 to HIF_REG21) are used to store the Ethernet MAC Station Address.

Byte-1:
The two least significant bits indicate whether the address is a uni-cast or multi-cast address, and also whether it is a Local or Global address.

Bit-0:
0 = uni-cast address.
1 = multi-cast address.

Bit-1:
0 = global address.
1 = local address.

The most significant bits (bit-2 to bit-7) of Byte-1, and all bits of the other Bytes (total of 46 bits) comprise the station address.

Address	Register	Field	HW	SW	Default	Description
0x0F	HIF_REG16	MAC[7:2], [1:0]	R/W	R/W	0	MAC Address
0x10	HIF_REG17	MAC[15:8]	R/W	R/W	50	MAC Address
0x11	HIF_REG18	MAC[23:16]	R/W	R/W	C5	MAC Address
0x12	HIF_REG19	MAC[31:24]	R/W	R/W	00	MAC Address
0x13	HIF_REG20	MAC[39:32]	R/W	R/W	47	MAC Address
0x14	HIF_REG21	MAC[47:40]	R/W	R/W	B5	MAC Address

Frame Drop Counter Register (HIF_REG22):

This register is used to store the frames dropped by the bridge in the receive path. The default value present in this register is 0x00. When ever a frame is dropped by the bridge this register is incremented by one. The contents of this register goes up to 0xFF and stops. Software can read the count and when it reaches 0xFF, the counter must be cleared by the software by writing 0x00 to this register.

Pause Threshold Register (HIF_REG23):

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
	Unused	Determines second threshold value			Determines pause threshold		

Bit	Description
2:0	Threshold difference. 000: 0 001: 128 word 010: 256 word 011: 384 word 100: 512 word 101: 640 word 110: 700 word 111: 758 word
5:3	Pause threshold. 000: 1516 word 001: 758 word 010: 1000 word 011: 1600 word 100: 1650 word 101: 1700 word 110: 1800 word 111: 2000 word
6	Unused
7	Pause control. 0: Enable pause. 1: Disable pause.

Notes:
1. On reset, all HIF_REG23 bits are set to zero.
2. This register can be modified from the Windows registry. The value should be written immediately after the USB device detection.

EEPROM Status Register (HIF_REG24):

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	EEPROM Status
0	0	0	0	0	0	0	0	Read in progress.
0	0	0	0	0	0	0	1	Read successful.
0	0	0	0	0	0	1	0	Read unsuccessful.
0	0	0	0	0	1	x	x	Software EEPROM read.

Note:
Software need not write anything in HIF_REG24[1:0].

Electrical Characteristics

Absolute Maximum Ratings

Operating Temperature	0 °C to +70 °C
Storage Temperature	-40 °C to +150 °C
ESD HBM (MIL-STD 883E Method 3015-7 Class 2)	2000V
ESD MM (JEDEC EIA/JESD22 A115-A)	200V
CDM (JEDEC JESD22 C101-A)	500V
Latch up (JESD No. 78, March 1997)	200 mA, 1.5 x VCC
Junction Temperature (Tj)	115 °C
Thermal Resistance of Junction to Ambient (Still Air)	60 °C/W

DC Electrical Specification

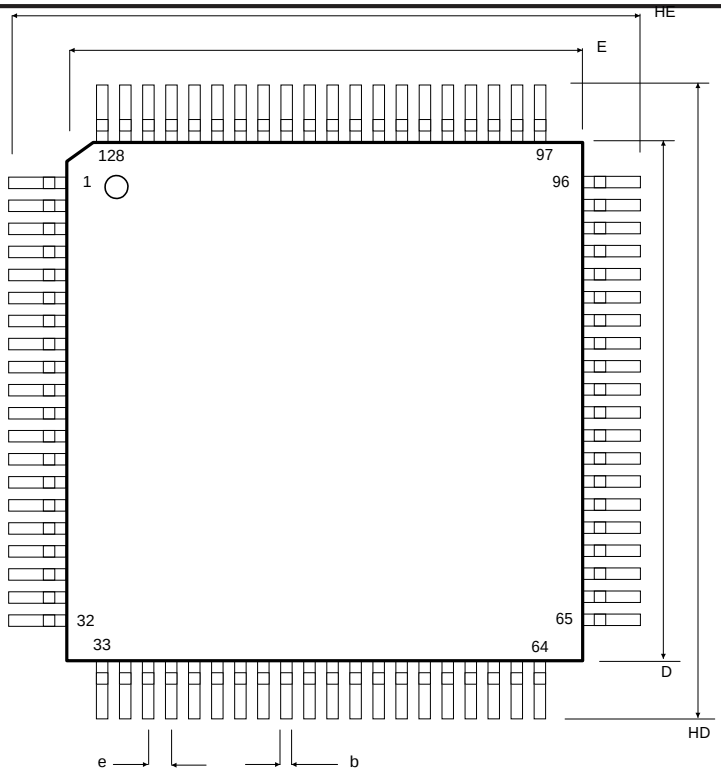
Temp = 0 °C to +70 °C, Vcc (3.3V) = 3.3V ±10%, Vcc (2.5 V) = 2.5V ±10% unless otherwise specified.

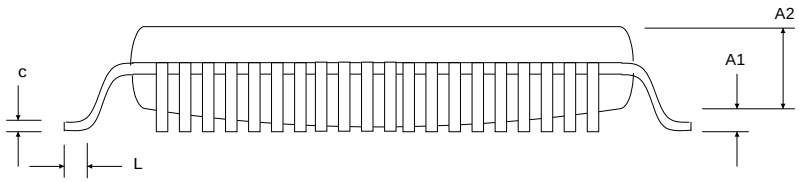
Symbol	Parameter	2.5V Min	2.5V Typ	2.5V Max		3.3V Min	3.3V Typ	3.3V Max	Unit	Condition
Vcc	Power Supply	2.25		2.75		3.0		3.6	V	
$Viclk_L$	Clock Input Voltage (low level)					-0.5		0.6	V	External
$Viclk_H$	Clock Input Voltage (high level)					2.4		Vcc	V	External
Vi_L	Input Voltage (low level)			0.82				1.08	V	CMOS
Vi_H	Input Voltage (high level)	1.6				2.1			V	CMOS
Vo_L	Output Voltage (low level)							0.4	V	Io_L = 4 mA
Vo_H	Output Voltage (high level)					1.85			V	Io_H = 4 mA
Ii_L	Input Leakage Current	-10		+10		-10		+10	µA	
Icc	Operating Current		100				40		mA	
Cp	Input pin Capacitance	3.1		5		3.1		5	pF	

AC Electrical Specification

Temp = 0 °C to +70 °C, Vcc (3.3V) = 3.3V ±10%, Vcc (2.5 V) = 2.5V ±10% unless otherwise specified.

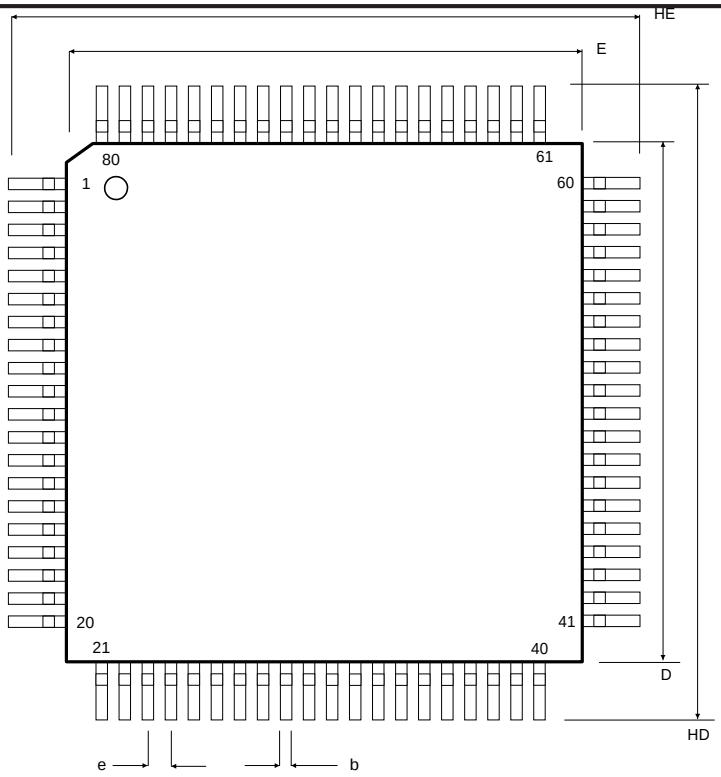
Symbol	Parameter	Typ	Unit	Condition
F_{CLKA}	USB Clock Frequency	12	MHz	±30 PPM
F_{CLKB}	10/100 PHY Clock Frequency	25	MHz	±30 PPM

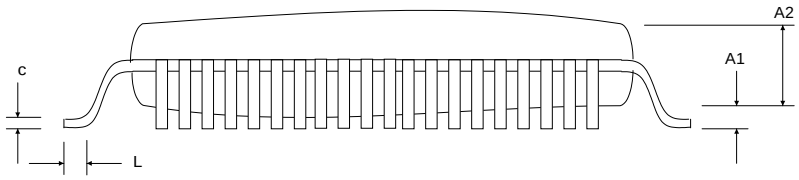




128-Pin "CQ" LQFP Package Dimensions

Symbol	Min	Millimeters Typ	Max
A1	0.05		-
A2	1.35		1.45
b	0.13		0.23
c	0.09		0.20
e		0.40	
L	0.45		0.75
HD	15.85	16	16.15
D	13.90	14	14.10
HE	15.85	16	16.15
E	13.90	14	14.10





80-Pin "CV" TQFP
Package Dimensions

Symbol	Millimeters		
	Min	Typ	Max
A1	0.05		0.15
A2	0.95		1.05
b	0.17		0.27
c	0.08		0.20
e		0.50	
L	0.45		0.75
HD		14	
D		12	
HE		14	
E		12	

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Revision History

Revision	Date	Comment
3.0	5-Nov-2006	Initial Release. Data Sheet version 3.0 was made for the new revision of MCS7830 silicon (i.e. MCS7830CQ-DA and MCS7830CV-DA). Revision 2.4 was for the previous silicon revision of the MCS7830 (i.e. MCS7830CQ and MCS7830CV)
3.1	31-Mar-2007	1. Marked all reserved pins as N.C. in the Pin-Out diagrams on pages 3 and 4. Added USB ground pins to Pin-Out diagrams on pages 3 and 4. 2. Added remote wakeup (RWKUP) and USB ground (UGND) pins to Pin-Out diagrams on pages 3 and 4 and Pin Descriptions table. 3. Added more information to the TXLED, RXLED, LINKLED, COLLED, and FDXLED pin descriptions. 4. Updated information in Maximum Ratings table. 5. Revised ICC operating current ratings in the DC electrical specifications table.
4.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram. 5. Modified some descriptions in the Feature page.

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