MCS9820
PCI to Single Serial Controller
Datasheet

Revision 2.00
Aug. 5th, 2011

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1. General Description

The MCS9820CV-BA is a PCI based single function I/O Adapter. It has one 16C450/16C550 compatible UART.

The MCS9820CV-BA has 32-Byte transmit and receive FIFO for UART channel. MCS9820CV-BA performs serial-to-parallel conversions on data received from a Serial device, and parallel-to-serial conversions on data received from its CPU.

The MCS9820CV-BA is ideally suited for PC applications, such as Add-On COM ports. It is available in 128-Pin QFP package & fabricated using an advanced submicron CMOS process to achieve low power drain and high-speed requirements.

MCS9820CV-BA is designed to be pin compatible with previous version of MCS9820CV. Existing designs of MCS9820CV can be migrated to MCS9820CV-BA without any modification to system design. Software compatibility is also maintained between MCS9820CV to MCS9820CV-BA.

2. Features

General

- 5V Operation
- Low Power
- Fully compliant with PCI Local Bus Specification 2.3
- Re-map function for Legacy Ports
- Microsoft WHQL Complaint Drivers
- 128 Pin QFP package, RoHS
- Commercial Grade, 0 to 70 deg C
- Advanced testability through scan addition

Serial Port

- One 16C 450 / 550 compatible UART
- Supports RS232, RS485 & RS422 modes
- Bi-directional Speeds from 50 bps to 115200 bps / Port
- Full Serial modem control
- Supports Hardware Flow Control
- 5, 6, 7, 8-bit Serial format support
- Even, Odd, None, Space & Mark parity supported
- On Chip deep 32 Byte FIFOs in Transmit, Receive path of Serial Port

Miscellaneous

- Four -Wire SPI Interface for EEPROM
- EEPROM read through PCI

3. Applications

- Generic Serial attached devices like Modem & Serial Mouse
- Serial Networking / Monitoring Equipment
- Data Acquisition System
- POS Terminal & Industrial PC
- Add-On I/O Cards
- Embedded systems – For I/O expansion
- Industrial Control

4. Ordering Information

- Part Number : MCS9820CV-BA
- 128 Pin QFP
- ROHS
- Commercial Grade, 0 to 70 deg C

5. Application Schematic

- PCI to 1S

6. Evaluation Board

- MCS98XXCV-BA EVB – Combo

7. Software Support

SW Driver Support

- Windows 95/98SE/ME
- Windows 32bit - 2000 /XP /NT /2003 Server
- Windows 64bit XP / 2003 Server
- Windows Vista / 2008 Server (32 & 64 bit)
- Windows 7 (32 & 64 bit)
- Linux Kernel 2.4.X / 2.6.X
- DOS-6.22

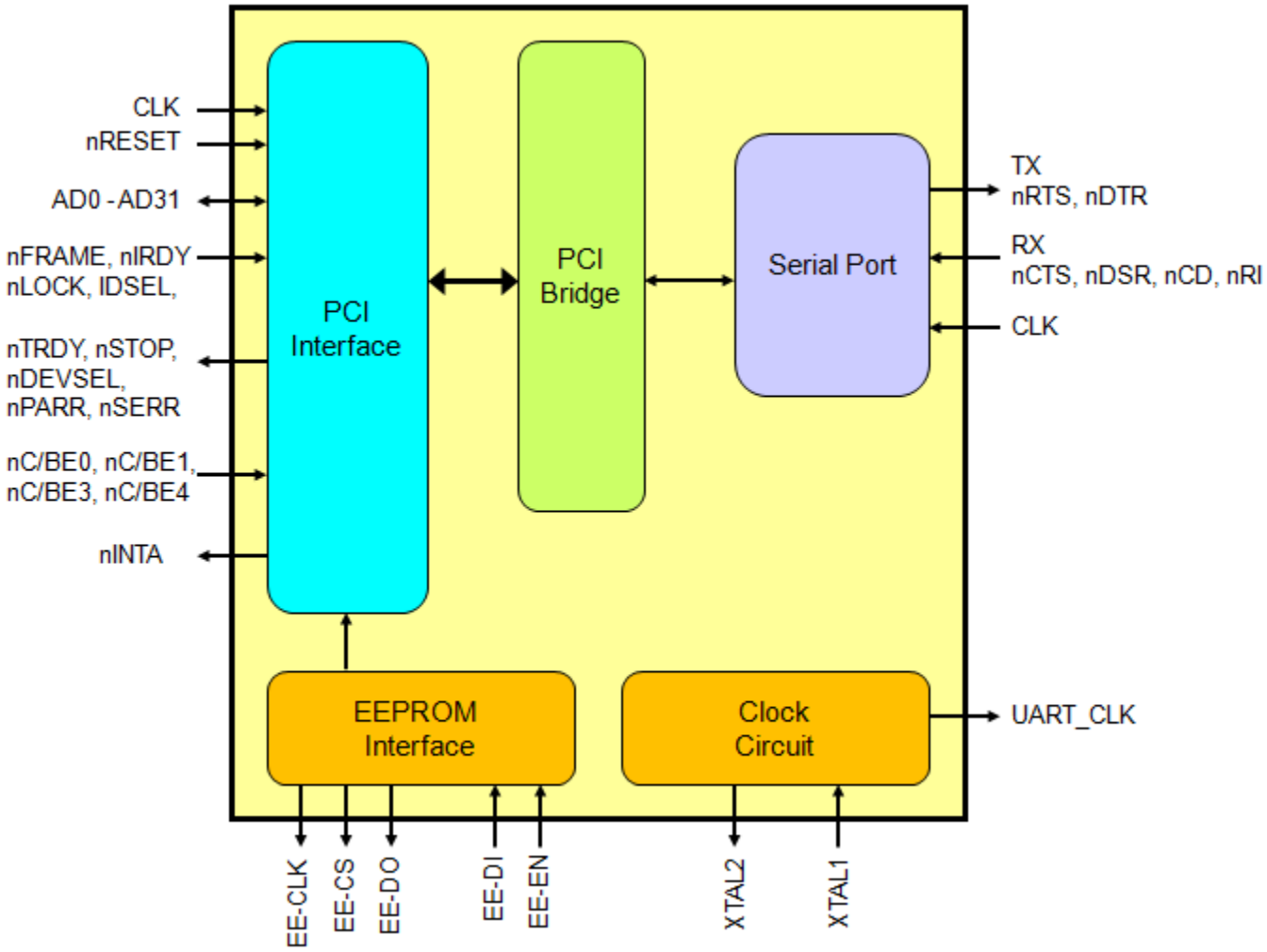
SW Utility Support

- Windows XP based Diagnostic Utility
- DOS based diagnostic Utility

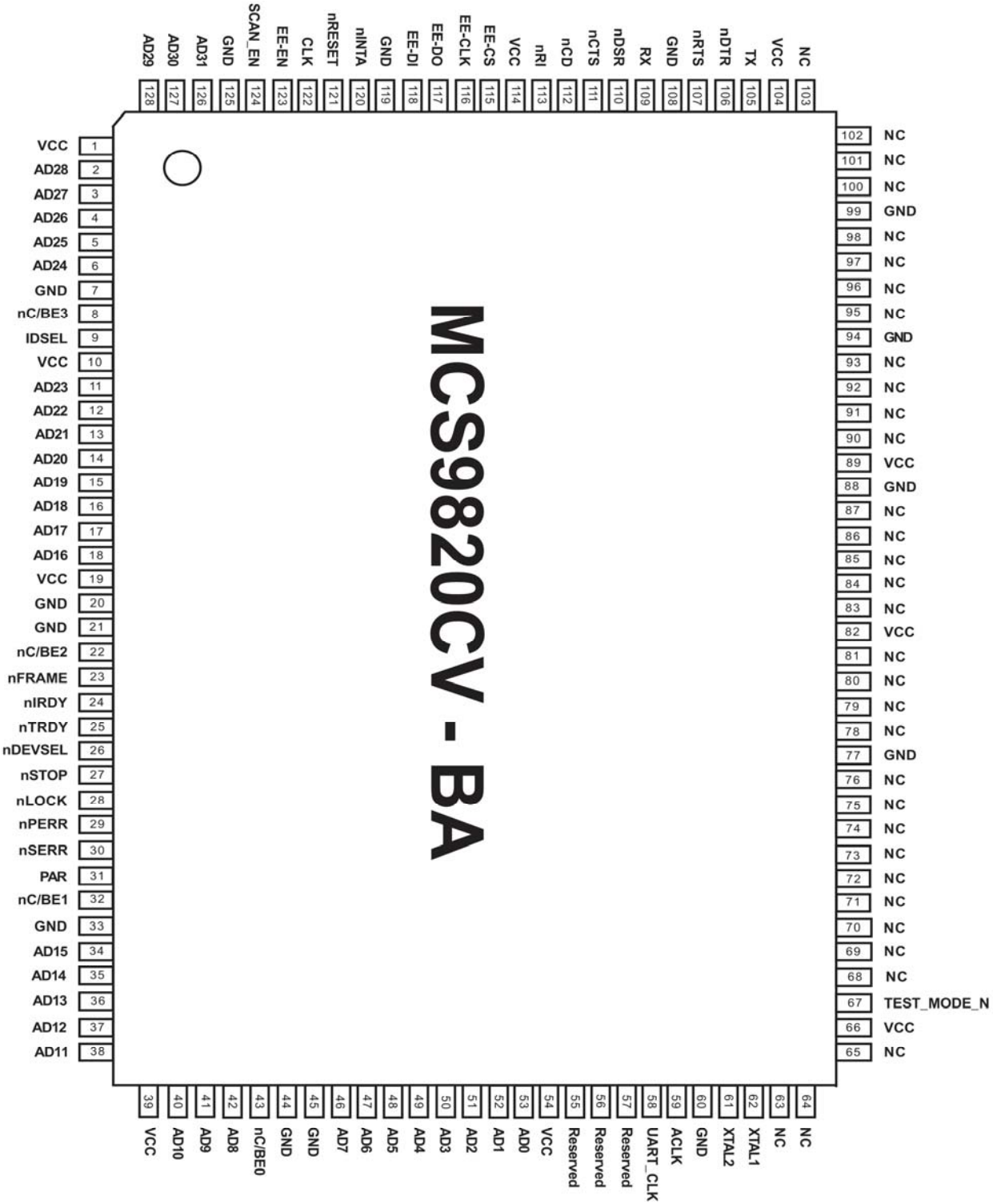
8. Certifications

- WHQL Certification of device drivers for Windows XP, Windows Vista & Windows 7 Operating Systems.

9. Block Diagram



10. Pin Diagram



11. Pin Descriptions

This section provides information on each Pin of MCS9820CV-BA

Name	Pin #	Direction	Drive Strength	Description
CLK	122	I		33 MHz PCI System Clock input.
nRESET	121	I(PU)		PCI system Reset (active low).Resets all internal registers, sequencers, and signals to a consistent state. During reset condition, AD[31-0] and nSERR are tri-stated.
AD[31-29]	126-128	I/O		Multiplexed PCI Address/Data bus. During the address phase, AD[31-0] contain a physical address. Data is stable and valid when nIRDY and nTRDY are asserted (active).
AD[28-24]	2-6	I/O		See AD[31-29] description.
AD[23-16]	11-18	I/O		See AD[31-29] description.
AD[15-11]	34-38	I/O		See AD[31-29] description.
AD[10-8]	40-42	I/O		See AD[31-29] description.
AD[7-0]	46-53	I/O		See AD[31-29] description.
nFRAME	23	I		nFRAME is asserted by the current Bus Master to indicate the beginning of an transfer. nFRAME remains active until the last Byte of the transfer is to be processed.
nIRDY	24	I		Initiator Ready. During a write, nIRDY asserted indicates that the initiator is driving valid data onto the data bus. During a read, nIRDY asserted indicates that the initiator is ready to accept data from the target device.
nTRDY	25	O		Target Ready (three-state). Asserted when target is ready to complete the current data phase.
nSTOP	27	O		Asserted to indicate that the target wishes the initiator to stop the transaction in progress on current data phase.

Name	Pin #	Direction	Drive Strength	Description
nLOCK	28	I		Indicates an atomic operation that may require multiple transactions to complete.
IDSEL	9	I		Initialization Device Select. Used as a chip select during configuration read and write transactions.
nDEVSEL	26	O		Device Select (three-state). Asserted when target has decoded one of its addresses.
nPERR	29	I/O		Parity Error (three-state). Used to report parity errors during all PCI transactions except a special cycle. The minimum duration of nPERR is one clock cycle.
nSERR	30	O		System Error (open drain). This pin goes low when address parity errors are detected.
PAR	31	I/O		Parity. Even Parity is applied across AD31-0 and C/BE3-0. PAR is stable and valid one clock after the address phase. For the data phase, PAR is stable and valid one clock after either nIRDY is asserted on a write transaction, or nTRDY is asserted on a read transaction.
nC/BE3	8	I		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte "3".
nC/BE2	22	I		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE2 applies to Byte "2".
nC/BE1	32	I		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE1 applies to Byte "1".
nC/BE0	43	I/O		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE0 applies to Byte "0".
nINTA	120	O		PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.

Name	Pin #	Direction	Drive Strength	Description
EE-CS	115	O	4mA	External EEPROM chip select (active high). After Power-On Reset, the EEPROM is read, and the read-only configuration registers are filled Sequentially from the first 64 Bytes in the EEPROM.
EE-CLK	116	O	4mA	External EEPROM clock.
EE-DI	118	I		External EEPROM data input.
EE-DO	117	O	4mA	External EEPROM data output.
EE-EN	123	I(PU)		Enable EEPROM (active high, internal pull-up). The external EEPROM can be disabled when this pin is tied to GND or pulled low. When the EEPROM is disabled, default values for PCI configuration registers will be used.
XTAL1	62	I		Crystal oscillator input or external clock input pin (22.1184 MHz). This signal input is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors connected from each side of the XTAL1 and XTAL2 to GND are required to form a crystal oscillator circuit.
XTAL2	61	O		Crystal oscillator output. See XTAL1 description.
UART_CLK	58	O	4mA	Master clock divided by 12 (1.8432 MHz). Standard UART clock for 115.2Kbps Baud rate.
Reserved	56	O		Reserved. No Connection, leave it as NC at system level.
Reserved	55	O		Reserved. No Connection, leave it as NC at system level.
ACLK	59	I(PU)		UART-A clock input. ACLK should be connected to UART_CLK output pin.
Reserved	57	I(PU)		Reserved
TX	105	O(PU)	12mA	UART serial Data Output.
nRTS	107	O(PU)	12mA	UART Request-To-Send signal. It is set high (inactive) after hardware Reset or during internal Loop-Back mode. When low, this indicates that UART is ready to transfer data. nRTS has no effect on the transmitter or receiver.

Name	Pin #	Direction	Drive Strength	Description
nDTR	106	O(PU)	12mA	UART Data-Terminal-Ready signal. It is set high (inactive) after a hardware Reset or during internal Loop-Back mode. When low, this output indicates to the modem or data set that UART-A is ready to establish a communication link. nDTR has no effect on the transmitter or receiver.
RX	109	I(PU)		UART, serial Data Input.
nCTS	111	I(PU)		UART Clear-To-Send signal. When low, this indicates that the modem or data set is ready to exchange data. nCTS has no effect on the transmitter.
nDSR	110	I(PU)		UART Data-Set-Ready signal. When low, this indicates the modem or data set is ready to establish a communication link.
nCD	112	I(PU)		UART Carrier-Detect signal. When low, this indicates the modem or data set has detected the data carrier. nCD has no effect on the transmitter.
nRI	113	I(PU)		UART Ring-detect signal.
Test_Mode_N	67	I(PU)		Reserved.
SCAN_EN	124	I(PD)		Reserved.
NC	63,64,65,68,69,70,71,72,73,74,75,76,78,79,80,81,83,84,85,86,87,90,91,92,93,95,96,97,98,100,101,102,103			No Connection

Name	Pin #	Direction	Drive Strength	Description
GND	7,20,21, 33, 44, 45,60,77, 88,94,99, 108,119, 125	Gnd		Power and Signal Ground.
Vcc	1,10,19, 39, 54, 66,82,89, 104,114	Pwr		Supply Voltage 5V

Note: -

I(PU) - Input – Internal Pull Up
I(PD) - Input – Internal Pull Down
O(PU) - Output – Internal Pull Up
OD_O (PU) - Open Drain Output – Internal Pull Up
I/O - - Bi-directional Signal
Pwr - Power
Gnd - Ground

12. Architectural overview

Architecture of MCS9820CV-BA is mainly divided in to four parts

- PCI core
- UART core.
- EEPROM

12.1 PCI Core

12.1.1 PCI Bus Operation

The execution of PCI Bus transactions take place in broadly five stages: address phase; transaction claiming; data phase(s); final data transfer; and transaction completion.

12.1.2 Address Phase

Every PCI transaction starts with an address phase, one PCI clock period in duration. During the address phase the initiator (also known as the current Bus Master) identifies the target device (via the address) and type of transaction (via the command). The initiator drives the 32-bit address onto the Address/Data Bus and a 4-bit command onto the Command/Byte-Enable Bus. The initiator also asserts the nFRAME signal during the same clock cycle to indicate the presence of valid address and transaction information on those buses. The initiator supplies the starting address and command type for one PCI clock cycle. The target generates the subsequent sequential addresses for burst transfers. The Address/Data Bus becomes the Data Bus, and the Command/Byte-Enable Bus becomes the Byte-Enable Bus for the remainder of the clock cycles in that transaction. The target latches the address and command type on the next rising edge of PCI clock, as do all other devices on that PCI bus. Each device then decodes the address and determines whether it is the intended target, and also decodes the command to determine the type of transaction.

12.1.3 Claiming the transaction

When a device determines that it is the target of a transaction, it claims the transaction by asserting nDEVSEL.

12.1.4 Data Phase(s)

The data phase of a transaction is the period during which a data object is transferred between the initiator and the target. The number of data Bytes to be transferred during a data phase is determined by the number of Command/Byte-Enable signals that are asserted by the initiator during the data phase. Each data phase is at least one PCI clock period in duration. Both initiator and target must indicate that they are ready to complete a data phase. If not, the data phase is extended by a wait state of one clock period in duration. The initiator and the target indicate this by asserting nIRDY and nTRDY respectively and the data transfer is completed at the rising edge of the next PCI clock.

12.1.5 Transaction Duration

The initiator, as stated earlier, gives only the starting address during the address phase. It does not tell the number of data transfers in a burst transfer transaction.

The target will automatically generate the addresses for subsequent Data Phase transfers. The initiator indicates the completion of a transaction by asserting nIRDY and de-asserting nFRAME during the last data transfer phase. The transaction does not actually complete until the target has also asserted the nTRDY signal and the last data transfer takes place. At this point the nTRDY and nDEVSEL are de-asserted by the target.

12.1.6 Transaction Completion

When all of nIRDY, nTRDY, nDEVSEL, and nFRAME are in the inactive state (high state), the bus is in idle state. The bus is then ready to be claimed by another Bus Master.

12.1.7 PCI Resource Allocation

PCI devices do not have "Hard-Wired" assignments for memory or I/O Ports like ISA devices do. PCI devices use "Plug & Play" to obtain the required resources each time the system boots up. Each PCI device can request up to six resource allocations. These can be blocks of memory (RAM) or blocks of I/O Registers. The size of each resource block requested can also be specified, allowing great flexibility. Each of these resource blocks is accessed by means of a Base-Address-Register (BAR). As the name suggests, this is a pointer to the start of the resource. Individual registers are then addressed using relative offsets from the Base-Address-Register contents. The important thing to note is: plugging the same PCI card into different machines will not necessarily result in the same addresses being assigned to it. For this reason, software (drivers, etc.) must always obtain the specific addresses for the device from the PCI System.

Each PCI device is assigned an entry in the PCI System's shared "Configuration Space". Every device is allocated 256 Bytes in the Configuration Space. The first 64 Bytes must follow the conventions of a standard PCI Configuration "Header". There are several pieces of information the device must present in specific fields within the header to allow the PCI System to properly identify it. These include the Vendor-ID, Device-ID and Class-Code. These three fields should provide enough information to allow the PCI System to associate the correct software driver with the hardware device. Other fields can be used to provide additional information to further refine the needs and capabilities of the device.

As part of the Enumeration process (discovery of which devices are present in the system) the Base-Address-Registers are configured for each device. The device tells the system how many registers (etc.) it requires, and the system maps that number into the system's resource space, reserving them for exclusive use by that particular device. No guarantees are made that any two requests for resources will have any predictable relationship to each other. Each PCI System is free to use its own allocation strategy when managing resources.

12.1.8 Multi-Function Devices

ASIX uses the Subsystem-ID field to indicate how many Serial Ports and Parallel Ports are provided by the current implementation. By changing the data in the Subsystem-ID field, and stuffing only the appropriate number of external components, the same board could be used for products with either one or two Ports. The least significant Hexadecimal digit of the Subsystem-ID field indicates the number of Serial Ports that are currently being provided by the device.

The next higher digit indicates the number of Parallel Ports being provided. The table below shows several different combinations and the types of Ports that would be enabled. Some ASIX devices provide Serial Ports, some provide Parallel Ports, and some provide both types of Ports. This field is used as an aid to the software Drivers, allowing them to easily determine how many of each Port type to configure.

Subsystem-ID	Parallel Ports	Serial Ports
0001	0	1
0010	1	0
0012	1	2

This use of the term "Multi-Function Device" should not be confused with the more generic use of that term by the PCI System. Each "Function" within a "Unit" (physical device) gets its own Configuration Space Header. ASIX's devices do not need this extra layer of complexity, the six Base Address Registers provided by one PCI "Function" are more than adequate to allocate all of the desired resources.

12.1.9 PCI Configuration Space Header

Default values for several key fields are shown in the table below.

AD 31-24	AD 23-16	AD 15-8	AD 7-0	Offset(Hex)
Device ID (9820)		Vendor ID (9710)		00
Status		Command		04
Class Code (078000)			Revision ID (01)	08
BIST	Header Type	Latency Timer	Cache Size (08)	0C
Base Address Register (BAR) 0 – "UART-A" (U1)				10
Reserved				14
Reserved				18
Reserved				1C
Reserved				20
Reserved				24
Reserved				28
Subsystem ID (0001)		Subsystem Vendor ID (1000)		2C
Reserved				30
Reserved				34
Reserved				38
Max Latency (00)	Min Grant (00)	Interrupt Pin (01)	Interrupt Line	3C
Reserved		Loading Timers		40
EEPROM Register				44
raidreg2	raidreg1	4'h0	Test Bus Sel	16'h9710	48

Internal Address Select Configuration

The MCS9820 uses single Base Address Registers.
These essentially act as internal “Chip Select” logic.
Registers are addressed by using one of the Base Addresses plus an offset.

PCI to Single UART (MCS9820CV-BA)

BAR Number	Core Module
BAR0	UART 1
BAR1	Reserved
BAR2	Reserved
BAR3	Reserved
BAR4	Reserved
BAR5	Reserved

12.2 UART Core

12.2.1 Overview

MCS9820 is a single serial which is 16C450/16C550 specification. Operation and functionality of this UART described below.

Main features of Serial Port :

- Supports RS232, RS485 & RS422 modes
- Bi-directional Speeds from 50 bps to 115200 bps / port
- Full Serial modem control
- Supports hardware flow control
- 5, 6, 7 and 8 bit serial format support
- Even, Odd, None, Space & Mark parity supported

12.2.2 Operational Modes

The UART is compatible with the 16C450, 16C550 mode of operation.. The operation of the port depends upon the mode settings, which are described below. The modes, conditions & corresponding FIFO depth are tabulated below.

UART mode	FIFO Size (Bytes)	FCR [0]
450	1	0
550	32	1

12.2.3 450 Mode

After the hardware reset, bit 0 of the FIFO Control Register (FCR) is cleared, hence the UART is compatible with the 16C450 mode of operation. The transmitter & receiver FIFOs (referred to as the "transmitting Holding register" & "receiver holding register" respectively) have a depth of one byte. This mode of operation is known "Byte Mode".

12.2.4 550 Mode

After the hardware reset, writing a 1 to FCR [0] will increase the FIFO size to 32, providing compatibility to 16C550 devices. In 16C550 mode of operation, the device has the following features.

- RTS/CTS hardware flow control
- Deeper FIFOs

Programmable Baud-Rate Generator

A programmable Baud Rate Generator is provided that typically takes a clock input of 1.8432 MHz and divides it by a divisor in the range between 1 and (2_{16}- 1). The output frequency of the Baud Rate generator is 16 times the desired Baud Rate. Two 8-bit registers, called Divisor Latches, store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during the device's initialization in order to ensure correct operation of the Baud Rate Generator. When either of the Divisor Latches is altered, an internal 16-bit Baud Counter is also updated to prevent long counts on the initial load.

Baud Rate generator programming table for the default 1.8432 MHz clock (UART_CLK).

Baud Rate (Bits per Second)	**Input Clock(MHz)**	**Baud Clock** Logic Out(Hz)	DLM	DLL
50	1.8432	798.6	9	0
150	1.8432	2.395K	3	0
300	1.8432	4.791K	1	128
600	1.8432	9.583K	0	192
1200	1.8432	19.160K	0	96
2400	1.8432	38.33K	0	48
4800	1.8432	76.666K	0	24
9600	1.8432	153.33K	0	12
19200	1.8432	460.8K	0	4
38400	1.8432	613.33K	0	3
57600	1.8432	920 K	0	2
115200	1.8432	1.84 M	0	1

ASIX devices with Serial Ports provide the UART_CLK output signal that can be used as the input clock for the UART. This is the standard 1.8432 MHz clock. Using this signal as the clock input generates the expected Baud Rates as shown in the table above.

12.3. External EEPROM

Data is read from the EEPROM immediately after a Hardware Reset, and the values obtained are used to update the Configuration before the PCI System first sees the device on the Bus. This allows a OEM Customers to customize the vendor and product ID's in place of ASIX ID's. EEPROM can be used to arrive at different product combination by setting appropriate sub-system ID's. For this EE-EN (Pin#123) to be left as No Connect at system level.

If external EEPROM is disabled by connecting the EE-EN (Pin#123) to ground, after hardware reset default values of configuration are loaded by the ASIC.

Following are main features of Serial EEPROM Interface :

- Supports Serial EEPROM of 1K Bit Size with 16bit communication capability
- Configuration Space contents can be modified through EEPROM
- Changing configuration values, different modes can be selected
- Inter Character Gap in multiples of 1bit duration can be set for UART.

Following EEPROM types confirmed at ASIX with MCS9820 **:**

- Atmel AT93LC46B, AT93C46B
- MICROCHIP 93LC46B, 93AA46B, 93AA46C
- ST Micro Electronics M93C46-WMN

13. Extended Modes through EEPROM

Mode supported by MCS9820 configuration without using external EEPROM.

- PCI to 1Serial

Vendor ID and Product ID customizations can be implemented in MCS9820, through external EEPROM. Any change of Vendor ID, Product ID information requires customized device driver.

Note : EEPROM need to be programmed in external EEPROM burner for customizations.

14. EEPROM Contents

Contents of the EEPROM (16-bit), values shown below are for 2S1P Mode

EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents	EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents
0x00	9820	Device ID(changes according to mode)	0x20	0000	
0x01	0000		0x21	0000	
0x02	9710	Vendor ID	0x22	0000	
0x03	0000		0x23	0000	
0x04	0000	{Intr_mask_reg[15:8], icg_reg1[7:0]}	0x24	0000	
0x05	0000		0x25	0000	
0x06	0000		0x26	0000	
0x07	0000		0x27	0000	
0x08	0780	Class code(23-8)	0x28	0000	
0x09	0000		0x29	0000	
0x0A	0001	{class code (7-0), Revision ID }	0x2A	0000	
0x0B	0000		0x2B	0000	
0x0C	0000	Header	0x2C	0001	Subsystem ID (Changes according to mode)
0x0D	0000		0x2D	0000	
0x0E	0000		0x2E	1000	Subsystem Vendor ID
0x0F	0000		0x2F	0000	
0x10	0000	ICG_reg2[7:0]	0x30	0000	
0x11	0000		0x31	0000	
0x12	0000		0x32	0000	
0x13	0000		0x33	0000	
0x14	0000		0x34	0000	
0x15	0000		0x35	0000	

EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents	EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents
0x16	0000		0x36	0000	
0x17	0000		0x37	0000	
0x18	0000		0x38	0000	
0x19	0000		0x39	0000	
0x1A	0000		0x3A	0000	
0x1B	0000		0x3B	0000	
0x1C	0000		0x3C	0000	{Max_lat[7:0], Min_gnt [7:0]}
0x1D	0000		0x3D	0000	
0x1E	0000		0x3E	0100	Interrupt Pin
0x1F	0000		0x3F	0000	

EEPROM Data Configuration Values

Description	EEPROM Address Location	Word/Byte Data
Device ID	0x00	9820
Vendor ID	0x02	9710
Class code	0x08	0780
Class code Interface	0x0A (Most Significant Byte)	00
Revision ID	0x0A (Least Significant Byte)	01
Header	0x0C (Least Significant Byte)	00
Subsystem ID	0x2C	0001
Subsystem Vendor ID	0x2E	1000
Interrupt pin	0x3E (Most Significant Byte)	01
Icg_reg1[7:0] Inter Character Gap setting register for UART-A	0x04(Least Significant Byte)	00 (This value is used to put the delay between each character).
Icg_reg2[7:0] Inter Character Gap setting register for UART-B	0x10(Least Significant Byte)	00 (This value is used to put the delay between each character).
Intr_mask_reg[15:8]	0x04(Most Significant Byte)	00

Icg_reg1 & 2 : Inter Character Gap register is used to set Inter Character Gap in multiples of 1bit duration for UART-A & B Ports

Intr_mask_reg[15:0] : Interrupt Mask Register can be used to mask the interrupt from unused Serial or Parallel ports.

Register(bit)	Value(Default for 2S+ 1P)	Description
Intr_mask_reg[8]	0	UART-A Interrupt Mask register. By setting this bit to "1" interrupts can be disabled from this Port.
Intr_mask_reg[9]	0	UART-B Interrupt Mask register. By setting this bit to "1" interrupts can be disabled from this Port.
Intr_mask_reg[11]	0	Parallel Port Interrupt Mask register. By setting this bit to "1" interrupts can be disabled from this Port.

The EEPROM controller reads the least significant byte and then the most significant byte in the 16-bit format. Therefore, when writing to each address in the EEPROM, the least significant byte must be written first, followed by the most significant byte. For example, to write 9820 into address 0x00, the value would be written as 20 98, where 20 is the least significant byte and is written first.

15. Electrical Specifications

Absolute Maximum Ratings

Supply Voltage	6 Volts
Voltage at any pin	GND - 0.3 V to VCC + 0.3 V
Operating Temperature	0 °C to +70 °C
Storage Temperature	-40 °C to +150 °C
ESD HBM (MIL-STD 883E Method 3015-7 Class 2)	2000V
ESD MM (JEDEC EIA/JEDS22 A115-A)	200V
CDM (JEDEC JEDS22 C101-A)	500V
Latch up (JESD No. 78, March 1997)	200 mA, 1.5 x Vcc

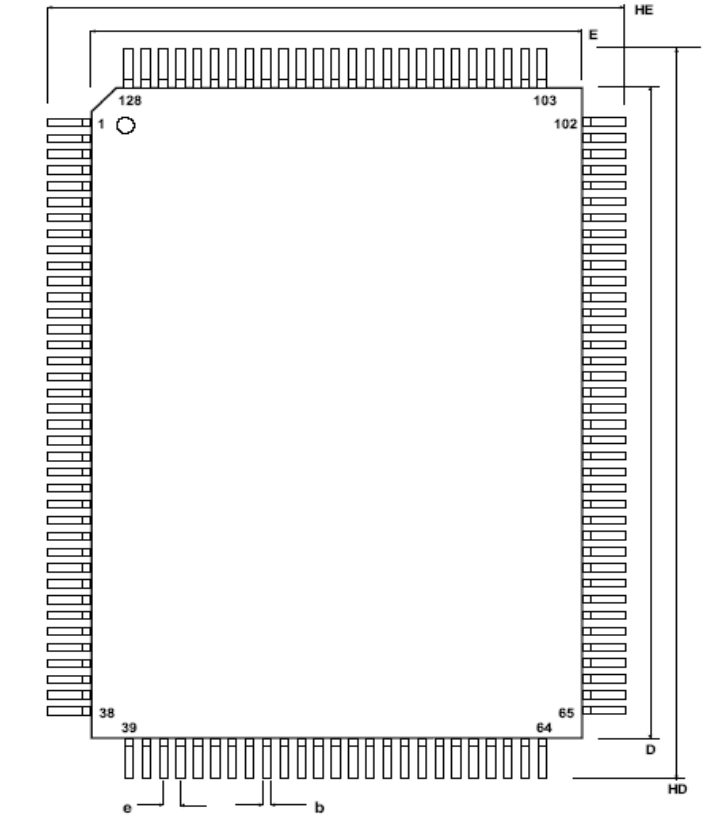
Recommended Operating Conditions

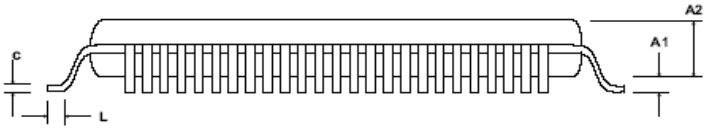
Symbol	Parameter	Min	Typ	Max	Unit	Condition
Vcc	Supply Voltage	4.75	5	5.25	V	
Vin	Input Voltage	0		Vcc		
Icc	Operating Current		70		mA	No Serial Load

DC Electrical Characteristics : Ta = 0 to +70 °C, VCC = 4.75 to 5.25 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Condition
ViL	Input Voltage (Low)			0.3 *Vcc	V	CMOS
ViH	Input Voltage (High)	0.7 *Vcc			V	CMOS
ViL	Input Voltage (Low)			0.8	V	TTL
ViH	Input Voltage (High)	2.0			V	TTL
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.84		V	CMOS
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		3.22		V	CMOS
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.10		V	TTL
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		1.87		V	TTL
VoL	Output Voltage (Low)			0.4	V	IoL = 2 to 24 mA
VoH	Output Voltage (High)	3.5			V	IoH = 2 to 24mA
Ri	Input Pull-Up/Pull-Down Resistance		50		KΩ	ViL = 0V or ViH = Vcc

16. Mechanical Specifications – QFP





128-Pin QFP
Package Dimensions

Symbol	Millimeters		
	Min	Typ	Max
A1	0.10		0.30
A2	2.73		2.97
b	0.17		0.27
c	0.09		0.20
e		0.50	
L	0.70		1.03
HD	23.00		23.40
D	19.90		20.10
HE	17.00		17.40
E	13.90		14.10

Revision History

Revision	Date	Comment
0.1	09th May 2008	Initial release
1.0	1st May 2008	"Tentative Data Sheet" text removed in all pages & document version changed to 1.0
1.1	9th March 2010	SW Support updated for Windows 7 and WHQL drivers availability
2.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram in Section 9.

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