MCS9904
PCIe to Quad Serial Controller
Datasheet

Revision 2.00
Aug. 5th, 2011

IMPORTANT NOTICE

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TRADEMARKS

Table of Contents

1   Introduction

MCS9904 is a single lane multifunction PCI express to I/O controller. MCS9904 supports four serial ports and eight GPIO's. MCS9904 also provides an option for peripheral expansion through ASIX proprietary Cascade interface. The generic cascade interface allows interconnecting with other ASIC's like MCS9900 to expand the peripheral ports.

The serial ports are compatible with RS232, RS422 & RS485 standards and supports throughput from 50bps to 16Mbps. All the GPIO pins are programmable and can be used as Input or Output. An I^{2}C interface is provided to configure MCS9904 device options through an external EEPROM.

1.1 Block Diagram
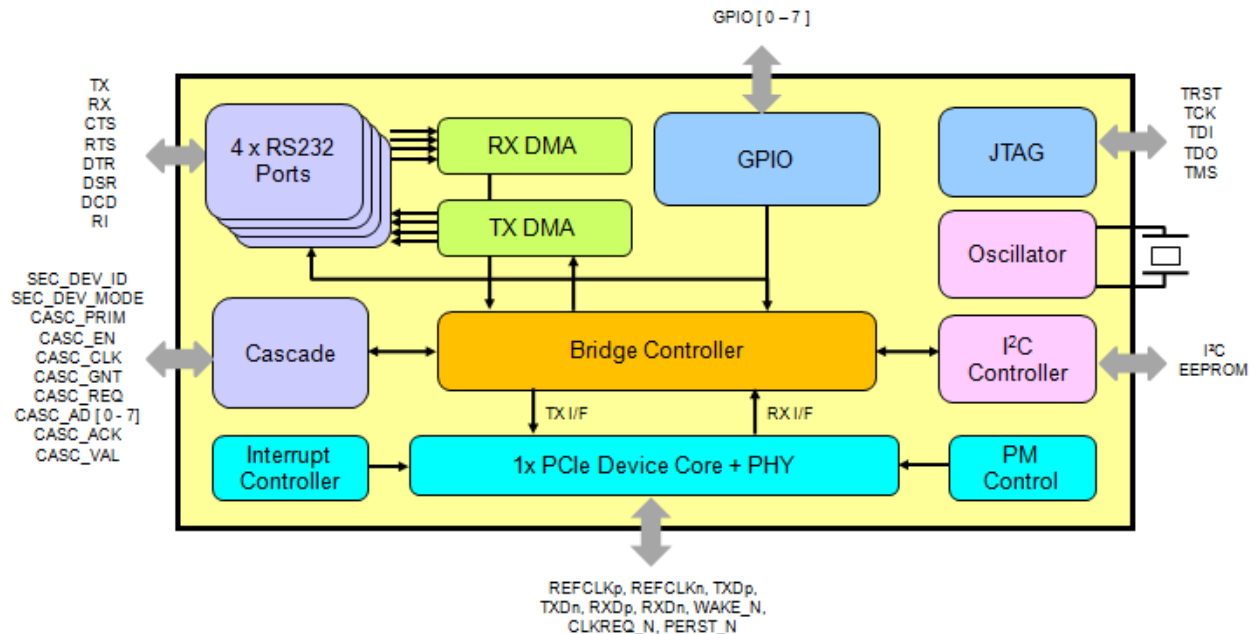
1.2 Features

PCI express

- Single-lane (X1) PCI Express End-point Controller with integrated PHY
- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express card specifications
- Supports four PCI Express functions
- Supports auto completion of configuration requests
- Supports built in flow control
- Supports Message TLP (Error) generation
- Supports integrated time out handling of Non-posted request
- Supports both legacy and MSI Interrupt
- Supports PCIe Power Management

Serial Port

- Four 16C450 / 550 / Extended 550 / 650 / ASIX Enhanced Mode compatible UARTs
- Supports RS232, RS422 & RS485 modes
- Bi-directional speeds from 50 bps to 16 Mbps per port
- Full Serial Modem Control
- Supports Hardware, Software Flow Control
- Supports 5, 6, 7, 8 bit Serial format
- Supports Even, Odd, None, Space and Mark parity
- Supports Custom baud rate by programming internal PLL or external clock
- Supports On Chip 256 Byte depth FIFOs in Transmit, Receive path of each Serial Port
- Supports remote wakeup and power management features
- Serial Port transceiver shutdown support
- Supports Slow IrDA mode (up to 115200bps) on all Serial Ports

Cascade

MCS9904 supports a 13-Pin proprietary interface to connect to other ASIX devices for IO expansion. Through this interface, MCS9904 can be used as Cascade Secondary device and can be connected to Cascade Primary capable ASIX Devices like MCS9900.

Eg. MCS9904 can be connected to MCS9900, for following product configurations.

- PCIe to 8 Serial Ports
- PCIe to 6 Serial Ports and one Parallel port

General Device Features

- I^{2}C interface for EEPROM
- EEPROM read / write through PCIe Interface
- 8 bi-directional multi-function GPIO lines
- On chip oscillator
- Power supply : 1.2V, 3.3V

1.3 Applications

- Serial Attached Devices
- Serial Networking / Monitoring Equipment
- Data Acquisition System
- POS Terminal & Industrial PC
- Add-On I/O Cards – Serial
- Embedded systems – For I/O expansion

1.4 Ordering information

- Ordering Part Number   : MCS9904CV-AA
- Operating Temperature   : 0 to 85° C
- Package   : 128 LQFP, RoHS

1.5 Support

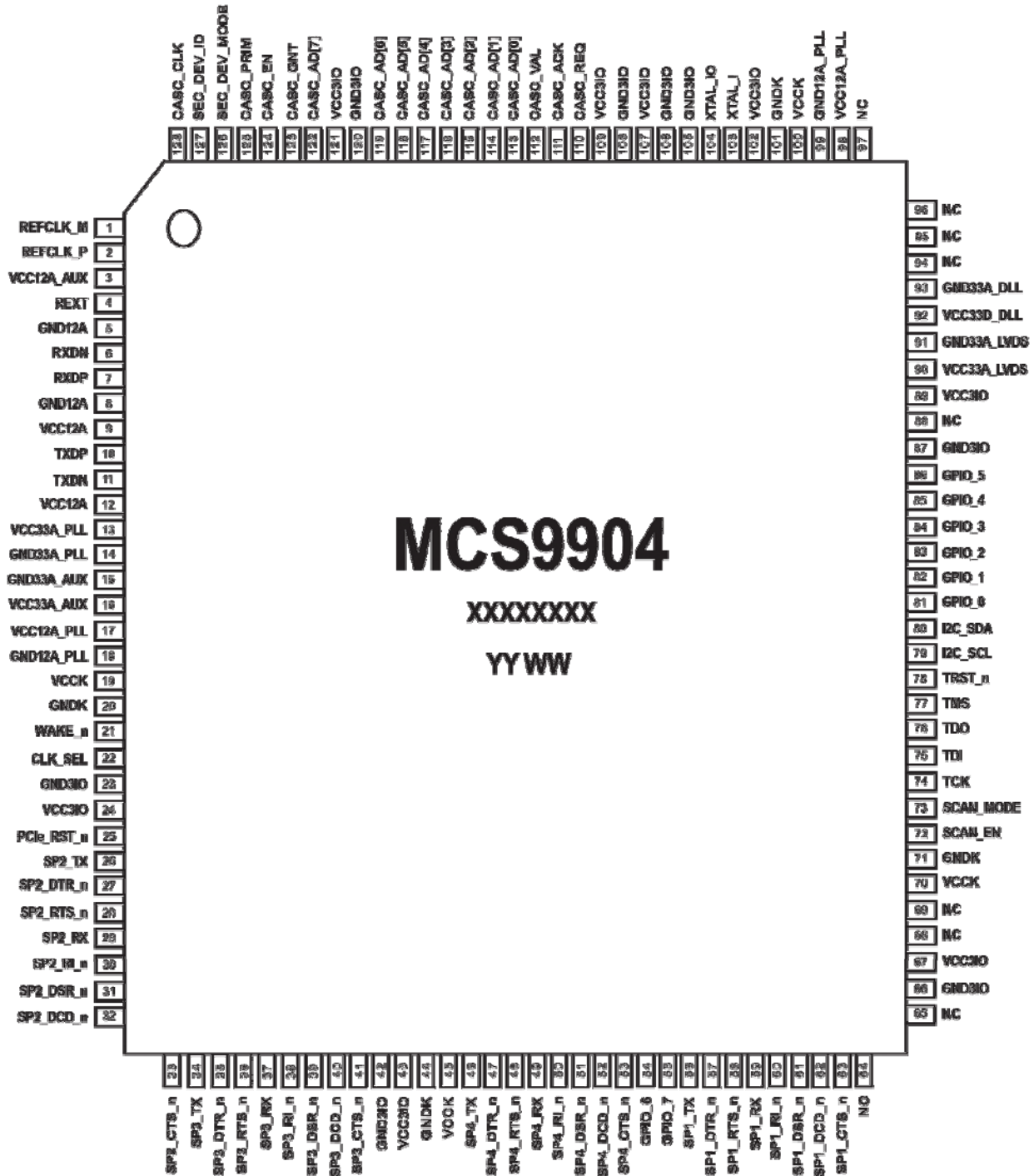- Reference Schematics   : Available ***
- Evaluation Board   : Available ***
- Software Support   : Available ***
- System Design Data & Other Technical Collateral   : Available ***

*** Please contact ASIX Support Team for above items, write to support@asix.com.tw

2 Pin Diagram

2.1 MCS9904CV-AA Pin diagram

3   Description

Pin Naming Convention

The Pin names use the following conventions:

"n" suffix is an active low signal, "I" – Input, "O" – Output, "P" – Passive, "DS" – Drive Strength in milli Amperes(mA), "PU" – Pull Up, "PD" – Pull Down, "N/A" – Not Applicable and "PROG" – Programmable

3.1   Pin configurations

Following table describes the pin configurations of MCS9904CV-AA device.

Pin	MCS9904	Pin	MCS9904	Pin	MCS9904	Pin	MCS9904
1	REFCLK_M	37	SP3_RX	73	SCAN_MODE	109	VCC3IO
2	REFCLK_P	38	SP3_RI_n	74	TCK	110	CASC_REQ
3	VCC12A_AUX	39	SP3_DSR_n	75	TDI	111	CASC_ACK
4	REXT	40	SP3_DCD_n	76	TDO	112	CASC_VAL
5	GND12A	41	SP3_CTS_n	77	TMS	113	CASC_AD[0]
6	RXDN	42	GND3IO	78	TRST_n	114	CASC_AD[1]
7	RXDP	43	VCC3IO	79	I2C_SCL	115	CASC_AD[2]
8	GND12A	44	GNDK	80	I2C_SDA	116	CASC_AD[3]
9	VCC12A	45	VCCK	81	GPIO_0	117	CASC_AD[4]
10	TXDP	46	SP4_TX	82	GPIO_1	118	CASC_AD[5]
11	TXDN	47	SP4_DTR_n	83	GPIO_2	119	CASC_AD[6]
12	VCC12A	48	SP4_RTS_n	84	GPIO_3	120	GND3IO
13	VCC33A_PLL	49	SP4_RX	85	GPIO_4	121	VCC3IO
14	GND33A_PLL	50	SP4_RI_n	86	GPIO_5	122	CASC_AD[7]
15	GND33A_AUX	51	SP4_DSR_n	87	GND3IO	123	CASC_GNT
16	VCC33A_AUX	52	SP4_DCD_n	88	NC	124	CASC_EN
17	VCC12A_PLL	53	SP4_CTS_n	89	VCC3IO	125	CASC_PRIM
18	GND12A_PLL	54	GPIO_6	90	VCC33A_LVDS	126	SEC_DEV_MODE
19	VCCK	55	GPIO_7	91	GND33A_LVDS	127	SEC_DEV_ID
20	GNDK	56	SP1_TX	92	VCC33D_DLL	128	CASC_CLK
21	WAKE_n	57	SP1_DTR_n	93	GND33A_DLL		
22	CLK_SEL	58	SP1_RTS_n	94	NC		
23	GND3IO	59	SP1_RX	95	NC		
24	VCC3IO	60	SP1_RI_n	96	NC		
25	PCIe_RST_n	61	SP1_DSR_n	97	NC		
26	SP2_TX	62	SP1_DCD_n	98	VCC12A_PLL		
27	SP2_DTR_n	63	SP1_CTS_n	99	GND12A_PLL		
28	SP2_RTS_n	64	NC	100	VCCK		
29	SP2_RX	65	NC	101	GNDK		
30	SP2_RI_n	66	GND3IO	102	VCC3IO		
31	SP2_DSR_n	67	VCC3IO	103	XTAL_I		
32	SP2_DCD_n	68	NC	104	XTAL_IO		
33	SP2_CTS_n	69	NC	105	GND3IO		
34	SP3_TX	70	VCCK	106	GND3IO		
35	SP3_DTR_n	71	GNDK	107	VCC3IO		

8

Pin	MCS9904	Pin	MCS9904	Pin	MCS9904	Pin	MCS9904
36	SP3_RTS_n	72	SCAN_EN	108	GND3IO		

3.2 PCI Express Interface Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
1	REFCLK_M	I	LVDS	–	–	PCIe PHY differential PLL reference clock. Cascade Mode: Pull down using 10K Resistor.
2	REFCLK_P	I	LVDS	–	–	PCIe PHY differential PLL reference clock. Cascade Mode: Pull down using 10K Resistor.
4	REXT	O	Analog	–	–	Bandgap External Resistor (Connect this pin to ground through an external resistor of 6.2KΩ, ±1%)
6	RXDN	I	LVDS	–	–	PCIe PHY differential negative serial data input. Cascade Mode: Pull down using 10K Resistor.
7	RXDP	I	LVDS	–	–	PCIe PHY differential positive serial data input. Cascade Mode: Pull down using 10K Resistor.
10	TXDP	O	LVDS	–	–	PCIe PHY differential positive serial data output. Cascade Mode: Leave this pin as "No Connection".
11	TXDN	O	LVDS	–	–	PCIe PHY differential negative serial data output. Cascade Mode: Leave this pin as "No Connection".
21	WAKE_n	O	LVTTL	4	PU	This is an active low signal used to reactivate the PCI Express slot's main power and reference clocks. Cascade Mode: Leave this pin as "No Connection".
22	CLK_SEL	O	LVTTL	4	PU	Used to enable/disable clock of PCI Express card.

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
25	PCIe_RST_n	I	LVTTL	4	PU	Active low asynchronous reset from PCIe RC

3.3 Serial Port Interface Signals

Serial Port 1

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
56	SP1_TX	O	LVTTL	4	–	Transmit data out to transceiver or IrDA data out to IR LED
57	SP1_DTR_n	O	LVTTL	4	–	Data terminal ready (Active Low) Also used for setting cascade clock Pull up : Sets cascade clock to run at 62.5 MHz Pull down : Sets cascade clock to run at 96 MHz
58	SP1_RTS_n	O	LVTTL	4	–	Request to send (Active Low)
59	SP1_RX	I	LVTTL	4	PU	Serial receives data in from transceiver or IrDA data in from IrDA detector.
60	SP1_RI_n	I	LVTTL	4	PU	Ring Indicator (Active Low)
61	SP1_DSR_n	I	LVTTL	4	PU	Data Set Ready (Active Low)
62	SP1_DCD_n	I	LVTTL	4	PU	Data Carrier Detect (Active Low)
63	SP1_CTS_n	I	LVTTL	4	PU	Clear to send (Active Low)

Serial Port 2

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
26	SP2_TX	O	LVTTL	4	–	Transmit data out to transceiver or IrDA data out to IR LED
27	SP2_DTR_n	O	LVTTL	4	–	Data terminal ready (Active Low)
28	SP2_RTS_n	O	LVTTL	4	–	Request to send (Active Low)
29	SP2_RX	I	LVTTL	4	PU	Serial receives data in from transceiver or IrDA data in from IrDA detector.

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
30	SP2_RI_n	I	LVTTL	4	PU	Ring Indicator (Active Low)
31	SP2_DSR_n	I	LVTTL	4	PU	Data Set Ready (Active Low)
32	SP2_DCD_n	I	LVTTL	4	PU	Data Carrier Detect (Active Low)
33	SP2_CTS_n	I	LVTTL	4	PU	Clear to send (Active Low)

Serial Port 3

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
34	SP3_TX	O	LVTTL	12	–	Transmit data out to transceiver or IrDA data out to IR LED
35	SP3_DTR_n	O	LVTTL	12	–	Data terminal ready (Active Low)
36	SP3_RTS_n	O	LVTTL	12	–	Request to send (Active Low)
37	SP3_RX	I	LVTTL	12	PU	Serial receives data in from transceiver or IrDA data in from IrDA detector.
38	SP3_RI_n	I	LVTTL	4	PU	Ring Indicator (Active Low)
39	SP3_DSR_n	I	LVTTL	4	PU	Data Set Ready (Active Low)
40	SP3_DCD_n	I	LVTTL	4	PU	Data Carrier Detect (Active Low)
41	SP3_CTS_n	I	LVTTL	4	PU	Clear to send (Active Low)

Serial Port 4

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
46	SP4_TX	O	LVTTL	4	–	Transmit data out to transceiver or IrDA data out to IR LED
47	SP4_DTR_n	O	LVTTL	4	–	Data terminal ready (Active Low)
48	SP4_RTS_n	O	LVTTL	12	–	Request to send (Active Low)
49	SP4_RX	I	LVTTL	12	PU	Serial receives data in from transceiver or IrDA data in from IrDA detector.
50	SP4_RI_n	I	LVTTL	12	PU	Ring Indicator (Active Low)
51	SP4_DSR_n	I	LVTTL	12	PU	Data Set Ready (Active Low)
52	SP4_DCD_n	I	LVTTL	12	PU	Data Carrier Detect (Active Low)
53	SP4_CTS_n	I	LVTTL	12	PU	Clear to send (Active Low)

3.4 Cascade Interface Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
110	CASC_REQ	I/O	LVTTL	8	–	To request the arbiter to grant access to CASC_AD bus.
111	CASC_ACK	I/O	LVTTL	8	–	Asserted by slave, in response to CASC_VAL, when it is ready to accept transfer
112	CASC_VAL	I/O	LVTTL	8	–	1: address/data/command on CASC_AD[7:0] is valid, 0: CASC_AD is not valid
113	CASC_AD[0]	I/O	LVTTL	8	–	To transfer Address / Data and control words
114	CASC_AD[1]	I/O	LVTTL	8	–	To transfer Address / Data and control words
115	CASC_AD[2]	I/O	LVTTL	8	–	To transfer Address / Data and control words
116	CASC_AD[3]	I/O	LVTTL	8	–	To transfer Address / Data and control words
117	CASC_AD[4]	I/O	LVTTL	8	–	To transfer Address / Data and control words
118	CASC_AD[5]	I/O	LVTTL	8	–	To transfer Address / Data and control words
119	CASC_AD[6]	I/O	LVTTL	8	–	To transfer Address / Data and control words
122	CASC_AD[7]	I/O	LVTTL	8	–	To transfer Address / Data and control words
123	CASC_GNT	I/O	LVTTL	8	–	Grant to access of CASC_AD bus
124	CASC_EN	I	LVTTL	4	PD	1 : cascade mode enabled 0 : cascade mode disabled
125	CASC_PRIM	I	LVTTL	4	PD	Chip is Cascade Secondary. Leave this Pin as "No Connection".

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
126	SEC_DEV_MODE	O	LVTTL	8	PD	For Non-Cascade applications, leave this pin as No Connect. When MCS9904CV-AA is used as Cascade Secondary Device, connect this pin to corresponding pin of the Cascade Primary Device.
127	SEC_DEV_ID	I	LVTTL	4	PD	Leave this pin as "No Connection"
128	CASC_CLK	O	LVTTL	8		Pull down externally using 1K resistor.

3.5 I^{2}C Interface Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
79	I2C_SCL	I/O	LVTTL	4	PU	2-Wire EEPROM Clock
80	I2C_SDA	I/O	LVTTL	4	PU	2-Wire EEPROM Data in/out.

3.6 GPIO Interface Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
81	GPIO_0	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
82	GPIO_1	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
83	GPIO_2	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
84	GPIO_3	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
85	GPIO_4	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
86	GPIO_5	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
54	GPIO_6	I/O	LVTTL	8	PU/PD	General Purpose I/O signal
55	GPIO_7	I/O	LVTTL	8	PU/PD	General Purpose I/O signal

3.7 Clock/Crystal Oscillator Interface Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
103	XTAL_I	I	Analog	–	–	Crystal input for PLL, 24 ~ 42MHz
104	XTAL_IO	I/O	Analog	–	–	Feedback signal for the oscillator pad

3.8 Test Mode Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
72	SCAN_EN	I	LVTTL	4	PD	Scan enable signal

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
73	SCAN_MODE	I	LVTTL	4	–	This signal is used as clock input in cascade mode. Cascade mode: Cascade Clock driven by 'primary' through 'CASC_CLK' should be interfaced to this pin. Non-Cascade Mode: Pull Down using 1K resistor.

3.9 JTAG Interface Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
74	TCK	I	LVTTL	4	–	JTAG chain clock
75	TDI	I	LVTTL	4	PD	JTAG chain input
76	TDO	O	LVTTL	4	–	JTAG chain output
77	TMS	I	LVTTL	4	PD	JTAG chain Test mode select
78	TRST_n	I	LVTTL	4	PU	JTAG Reset (pull-up is recommended on JTAG Reset)

3.10 Power Supply Signals

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
3	VCC12A_AUX	P	PWR	–	–	1.2V Analog Power Supply
9	VCC12A	P	PWR	–	–	1.2V Analog Power Supply
12	VCC12A	P	PWR	–	–	1.2V Analog Power Supply
13	VCC33A_PLL	P	PWR	–	–	3.3V Analog Power Supply
16	VCC33A_AUX	P	PWR	–	–	3.3V Analog Power Supply
17	VCC12A_PLL	P	PWR	–	–	1.2V Analog Power Supply
19	VCCK	P	PWR	–	–	1.2V Digital Power Supply
24	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
43	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
45	VCCK	P	PWR	–	–	1.2V Digital Power Supply
67	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
70	VCCK	P	PWR	–	–	1.2V Digital Power Supply
89	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
90	VCC33A_LVDS	P	PWR	–	–	3.3V Analog Power Supply
92	VCC33D_DLL	P	PWR	–	–	3.3V Digital Power Supply
98	VCC12A_PLL	P	PWR	–	–	1.2V Analog Power Supply
100	VCCK	P	PWR	–	–	1.2V Digital Power Supply
102	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
107	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
109	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
121	VCC3IO	P	PWR	–	–	3.3V Digital Power Supply
5	GND12A	P	PWR	–	–	Analog Ground
8	GND12A	P	PWR	–	–	Analog Ground
14	GND33A_PLL	P	PWR	–	–	Analog Ground
15	GND33A_AUX	P	PWR	–	–	Analog Ground
18	GND12A_PLL	P	PWR	–	–	Analog Ground
20	GNDK	P	PWR	–	–	Digital Ground
23	GND3IO	P	PWR	–	–	Digital Ground
42	GND3IO	P	PWR	–	–	Digital Ground
44	GNDK	P	PWR	–	–	Digital Ground
66	GND3IO	P	PWR	–	–	Digital Ground
71	GNDK	P	PWR	–	–	Digital Ground
87	GND3IO	P	PWR	–	–	Digital Ground
91	GND33A_LVDS	P	PWR	–	–	Analog Ground
93	GND33A_DLL	P	PWR	–	–	Analog Ground
99	GND12A_PLL	P	PWR	–	–	Analog Ground
101	GNDK	P	PWR	–	–	Digital Ground
105	GND3IO	P	PWR	–	–	Digital Ground
106	GND3IO	P	PWR	–	–	Digital Ground
108	GND3IO	P	PWR	–	–	Digital Ground

Pin#	Pin name	I/O/P	Type	DS	PU/PD	Description
120	GND3IO	P	PWR	–	–	Digital Ground

Note: Pin Numbers 64, 65, 68, 69, 88, 94, 95, 96 & 97 are "No Connect" Pins for MCS9904.

4   Function Mapping

Function Mapping

Function	Non – Cascade Mode	Cascade Mode	
	4 Serial	8 Serial	6 Serial + 1 Parallel
Function 0	Serial Port 1	Serial Port 1 Serial Port 5	Serial Port 1 Serial Port 5
Function 1	Serial Port 2	Serial Port 2 Serial Port 6	Serial Port 2 Serial Port 6
Function 2	Serial Port 3	Serial Port 3 Serial Port 7	Serial Port 3 Parallel Port
Function 3	Serial Port 4	Serial Port 4 Serial port 8	Serial Port 4

5   Functional Description

MCS9904CV-AA is a single lane PCI Express based multifunction peripheral controller which supports 4-Port UART Controller, Cascade Controller, GPIO Controller, an I^{2}C Controller and a bridge to control the transfers between the interfaces and PCIe.

The Serial port controllers are compatible with 16C450/550/Extended 550. It supports RS232, RS422 and RS485 standards with bi-directional speeds from 50bps to 16Mbps/port. MCS9904 also supports Custom BAUD rates with external clock or by programming internal PLL. Each Serial port controller uses an on-chip 256 byte deep FIFO in Transmit and receive paths.

The Cascade interface is a 13-pin ASIX proprietary interface which supports to add another cascade supported chip to expand the peripheral functions.

An I^{2}C master interface is included to be able to connect to EPROM that could store PCIe device configuration. The 8-GPIO pins are programmable as an Input or Output.

5.1   PCIe Operation

PCIe is divided into three major blocks as Physical layer, Data link layer and Transaction layer. Physical link layer and Transaction layer together comprises PCIe core. Their functionality is explained below.

PCIe PHY

The Physical Layer isolates the Transaction and Data Link Layers from the signaling technology used for Link data interchange. The Physical Layer is divided into the logical and electrical functional sub-blocks.

The logical sub-block has two main sections: A transmit section that prepares outgoing information passed from the Data Link Layer for transmission by the electrical sub-block, and a receiver section that identifies and prepares received information before passing it to the Data Link Layer. The logical sub-block and electrical sub-block coordinate the state of each transceiver through a status and control register interface or functional equivalent. The logical sub-block directs control and management functions of the Physical Layer.

The electrical sub-block contains a Transmitter and a Receiver. The Transmitter is supplied by the logical sub-block with Symbols which it serializes and transmits onto a Lane. The Receiver is supplied with serialized Symbols from the Lane. It transforms the electrical signals into a bit stream which is de-serialized and supplied to the logical sub-block along with a Link clock recovered from the incoming serial stream.

The Physical Layer is responsible for the following:
- Power management
- Width and lane negotiation
- Reset/hot-plug control
- 8-bit/10-bit encoding/decoding
- Scrambling/de-scrambling
- Embedded clock tuning and alignment
- Transmission and reception circuit
- Elastic buffer
- Data Link Layer

The Data Link Layer
The Data Link Layer acts as an intermediate stage between the Transaction Layer and the Physical Layer. The Data Link Layer is responsible for reliably conveying Transaction Layer Packets (TLPs) supplied by the Transaction Layer across a PCI Express Link to the other component's Transaction Layer

The Data Link Layer is responsible for the following:
- Link management including TLP acknowledgment
- Retry mechanism in case of a non-acknowledged packet
- Flow control across the Link (transmission and reception)
- Power management
- CRC generation and CRC checking
- Error reporting

Transaction Layer/User Interface Layer
Transaction layer and User interface layer together perform all transaction layer functionalities. User interface layer defines a plug-and-play type interface mechanism to accept TLPs from user space for transmission, and to pass received TLPs on reception.

The Transaction Layer is primarily responsible for the following:
- Assembly and disassembly of Transaction Layer packets (TLPs)
- Storage of configuration information
- Converts received Completion packets into data payloads,
- Updates status information
- Responsible for flow control services
- Ordering rules
- Power management services
- PCIe Bridge
- Master Slave Bridge is divided into PCIe packet formatter, PCIe target interface block, Mater arbiter, Slave de-mux and VCI interface block.

19

5.2 PCIe Configuration Space

The following table describes PCIe configuration space register value details for Non-Cascade and Cascade modes supported by MCS9904

Non cascade mode

Function	Register	MCS9904CV-AA
Function0	Device ID	16'h9904
	Vendor ID	16'h9710
	Revision ID	'h0
	Class code	'h7
	Sub Class Code	'h0
	Program interface	'h2
	Sub Vendor ID	'hA000
	Sub Device ID	'h1000
	Power Management Cap	16'h060F
	extended Capabilities	'h1
	Device Capabilities	16'h8302
	Link Capabilities	'h7
	MSI & Clock Power Mgmt Enable	8'h19
	Interrupt Pin	'h1
Function1	Device ID	16'h9904
	Vendor ID	16'h9710
	Revision ID	'h0
	Class code	'h7
	Sub Class Code	'h0
	Program interface	'h2
	Sub Vendor ID	'hA000
	Sub Device ID	'h1000
	Power Management Cap	16'h060F
	extended Capabilities	'h1
	Device Capabilities	16'h8302
	Link Capabilities	'h7
	MSI & Clock Power Mgmt Enable	8'h19

20

Function	Register	MCS9904CV-AA
	Interrupt Pin	'h2
Function2	Device ID	16'h9904
	Vendor ID	'h9710
	Revision ID	'h0
	Class code	'h7
	Sub Class Code	'h0
	Program interface	'h2
	Sub Vendor ID	'hA000
	Sub Device ID	'h1000
	Power Management Cap	16'h060F
	extended Capabilities	'h1
	Device Capabilities	16'h8302
	Link Capabilities	'h7
	MSI & Clock Power Mgmt Enable	'h19
	Interrupt Pin	'h3
Function3	Device ID	'h9904
	Vendor ID	'h9710
	Revision ID	'h0
	Class code	'h7
	Sub Class Code	'h0
	Program interface	'h2
	Sub Vendor ID	'hA000
	Sub Device ID	'h1000
	Power Management Cap	16'h060F
	extended Capabilities	'h1
	Device Capabilities	16'h8302
	Link Capabilities	'h7
	MSI & Clock Power Mgmt Enable	'h19
	Interrupt Pin	'h4

Cascade mode

Function	Register	4S+4S	2S1P+4S
Function0	Device ID	16'h9900	16'h9900
	Vendor ID	'h9710	'h9710
	Revision ID	'h0	'h0
	Class code	'h7	'h7
	Sub Class Code	'h80	'h80
	Program interface	'h0	'h0
	Sub Vendor ID	'hA000	'hA000
	Sub Device ID	'h3002	'h3002
	Power Management Cap	16'h060F	16'h060F
	extended Capabilities	'h1	'h1
	Device Capabilities	16'h8302	16'h8302
	Link Capabilities	'h7	'h7
	MSI & Clock Power Mgmt Enable	8'h29	8'h29
	Interrupt Pin	'h1	'h1
Function1	Device ID	16'h9900	16'h9900
	Vendor ID	'h9710	'h9710
	Revision ID	'h0	'h0
	Class code	'h7	'h7
	Sub Class Code	'h80	'h80
	Program interface	'h0	'h0
	Sub Vendor ID	'hA000	'hA000
	Sub Device ID	'h3002	'h3002
	Power Management Cap	16'h060F	16'h060F
	extended Capabilities	'h1	'h1
	Device Capabilities	16'h8302	16'h8302
	Link Capabilities	'h7	'h7
	MSI & Clock Power Mgmt Enable	8'h29	8'h29
	Interrupt Pin	'h2	'h2
Function2	Device ID	16'h9900	16'h9900
	Vendor ID	'h9710	'h9710
	Revision ID	'h0	'h0
	Class code	'h7	'h7
	Sub Class Code	'h80	'h80
	Program interface	'h0	'h0
	Sub Vendor ID	'hA000	'hA000
	Sub Device ID	'h3002	'h3012

22

Function	Register	4S+4S	2S1P+4S
	Power Management Cap	16'h060F	16'h060F
	extended Capabilities	'h1	'h1
	Device Capabilities	16'h8302	16'h8302
	Link Capabilities	'h7	'h7
	MSI & Clock Power Mgmt Enable	8'h29	8'h29
	Interrupt Pin	'h3	'h3
Function3	Device ID	16'h9900	16'h9900
	Vendor ID	'h9710	'h9710
	Revision ID	'h0	'h0
	Class code	'h7	'h7
	Sub Class Code	'h80	'h80
	Program interface	'h0	'h0
	Sub Vendor ID	'hA000	'hA000
	Sub Device ID	'h3002	'h1000
	Power Management Cap	16'h060F	16'h060F
	extended Capabilities	'h1	'h1
	Device Capabilities	16'h8302	16'h8302
	Link Capabilities	'h7	'h7
	MSI & Clock Power Mgmt Enable	8'h29	8'h29
	Interrupt Pin	'h4	'h4

5.3 Serial Port

Serial port is a full-duplex device which uses separate lines for transmitting and receiving data to send and receive data at the same time. When a character is about to be transmitted, a start bit is sent. A start bit has a value of 0 (also called a space state). Thus, when the line switches from a value of 1 to a value of 0, the receiver is alerted that a data character is about to be sent. Once the start bit has been sent, the transmitter sends the actual data bits. There may either be 5, 6, 7 or 8 data bits, depending on the number you have selected. Both receiver and the transmitter must agree on the number of data bits, as well as the baud rate.

Notice, when only 7 data bits are employed, and cannot send ASCII values greater than 127. Likewise, using 5 bits limits the highest possible value to 31. After the data has been transmitted, a stop bit is sent. A stop bit has a value of 1 or a mark state and it can be detected correctly even if the previous data bit also had a value of 1. This is accomplished by the stop bit's duration. Stop bits can be 1, 1.5 or 2 bit periods in length.

Besides the synchronization provided by the use of start and stop bits, an additional bit called a parity bit may optionally be transmitted along with the data. A parity bit affords a small amount of error checking, to help detect data corruption that might occur during transmission. You can choose even parity, odd parity, mark parity, space parity or none at all. When even or odd parity is being used, the number of marks (logical 1 bit) in each data byte is counted, and a single bit is transmitted following the data bits to indicate whether the number of 1 bit just sent is even or odd.

The Serial port implements the Enhanced mode and all of its features and it is backward compatible to the other modes. Each serial port controller has register logic controlling baud rates (50 bps – 16 Mbps), stop bits, parity bit settings. In addition, this block has serial port specific registers for interrupts, line status, line control features which can be accessed by software. The serial port controllers can interface to external RS232/RS422/RS485 transceivers. All the modes have some extra features to enhance the performance.

The different modes of serial port are:

- UART 16C450(Default Mode)
- UART 16C550
- UART 16C550 Ex
- UART 16C650 Mode
- ASIX Enhanced Mode

UART 16C450 Mode

This mode of operation is also known as Byte mode of operation. After the power on reset, the default UART operating mode is set to 16C450.

UART 16C550 Mode

After the hardware reset, writing a 1 to FCR [0] register increases the FIFO size to 16, providing the compatibility with 16C550 type of devices. This mode of operation also does not have any enhanced features. Support all the features of 450 mode.

UART 16C550 Extended Mode

After the hardware reset, writing a 1 to FCR [0] and enabling the FIFOSEL signal the UART goes in to the 16C550 extended mode. In this mode the FIFO size increases to 128 from 16. This mode of operation also does not have any enhanced features. Support all the features of 16C550 mode.

UART 16C650 Mode

UART is compatible with 16C650 mode when the EFR [4] is set, i.e. the device is in the enhanced mode. In 16C650 mode, software drivers usually put the device in the enhanced mode. Running 16C650 drivers on the UART channel will result in 16C650 compatibility mode with 128 deep FIFOs, as long as the FCR [0] register is set. Support all the features of 16C550 Ex mode.

ASIX Enhanced Mode

The additional features offered in ASIX Enhanced mode generally apply when the UART is in enhanced mode. Flow control and High baud rate support can be achieved in this mode of operation. In enhanced mode, the FIFO size is 128 bytes. ASIX Enhanced mode specific features are enabled using the additional control register ACR.

5.4 I^{2}C

All I^{2}C devices are connected through two wires: serial data (SDA) and serial clock (SCL). I^{2}C has a master/slave protocol. The master initiates the communication. Since there are only two wires, this protocol includes the extra overhead of the addressing and acknowledgment mechanisms.

Serial Data: The serial data SDA is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal; therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz). For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

Serial Clock: The serial clock SCL is a bi-directional pin used to synchronize the data transfer from and to the device.

Address inputs: The address inputs A0, A1, A2 are used by the slave for multiple device operations. The logic levels on these inputs are compared with the corresponding bits in the slave address.

EEPROM Access
I^{2}C operation is performed at address: GPIO_I2C_BAR5+0xC8.

The 32-bit information sent at this address is specified in tsif_cfg_data_in register. The details of this register are as follows:

Bits	Type	Reset	Name	Description
[31]	RW	0	tsif_cfg_data_in	If '1' specifies write to EPROM. If '0' specifies read from EEPROM.
[30:25]	RW	0	tsif_cfg_data_in	specifies I^{2}C device address
[24]	RW	0	tsif_cfg_data_in	specifies I^{2}C address is 8-bit/16-bit
[23:8]	RW	0	tsif_cfg_data_in	specifies I^{2}C address
[7:0]	RW	0	tsif_cfg_data_in	specifies 8-bit data

5.5 PM Control

This block implements power management. The chip works in three PCIe based power states (1) D0, (2) D3 Hot and (3) D3 Cold.

There is NO power plane separation between Vaux and VCC. In D3 Cold, the chip VCC should be powered from Vaux to support remote wake up.

Further power save is achieved through disabling the blocks which are not selected. A set of register bits, Port_dis_reg[7:0], are provided to disable each block independently. Port_dis_reg is mapped to BAR4 + 0x69 and can access through all functions and its bit map is given below

| Register Bit	Control	Description
port_dis_reg[0]	pp_disable	1: Disables Parallel Port
port_dis_reg[1]	Serial Port transceiver shut down polarity	1: Active Low 0: Active High
port_dis_reg[2]	Serial Port transceiver shut down enable	1: Enables transceiver shut down when in power save mode 0: disables transceiver shut down
port_dis_reg[3]	sp1_disable	1 : Disables Serial Port 1
port_dis_reg[4]	sp2_disable	1 : Disables Serial Port 2
port_dis_reg[5]	sp3_disable	1 : Disables Serial Port 3
port_dis_reg[6]	sp4_disable	1 : Disables Serial Port 4
port_dis_reg[7]	disp_disable	1 : Reserved

5.6 Cascade Interface

Cascade Interface is a generic IO expansion bus that is based on ASIX proprietary interface protocol. The cascade interface allows interconnecting any ASIX device supporting the cascade interface protocol.

A standalone MCS9904 device supports up to 4 serial ports over PCIe. When a MCS9904 device is interconnected through MCS9900 device using cascade interface, the number of peripheral ports can be doubled. The combined MCS9900 and MCS9904 devices are serviced through a single PCIe on the primary MCS9900, and the ports can be expanded using one of the following configurations.

- 8 serial ports
- 6 serial ports + 1 parallel port

In cascaded configuration, MCS9900 chips works as primary and MCS9904 as secondary. The primary chip implements 4-function PCIe endpoint. The PCIe core of secondary chip is disabled. Only cascade and serial port logic is active in secondary MCS9904 chip

The cascade interface also allows connecting any other chip that's designed as per this interface. When a non MCS9904 chip is connected, functions 0, 1 and 2 are used by primary and functions 3 and 4 are available to be used by secondary chip.
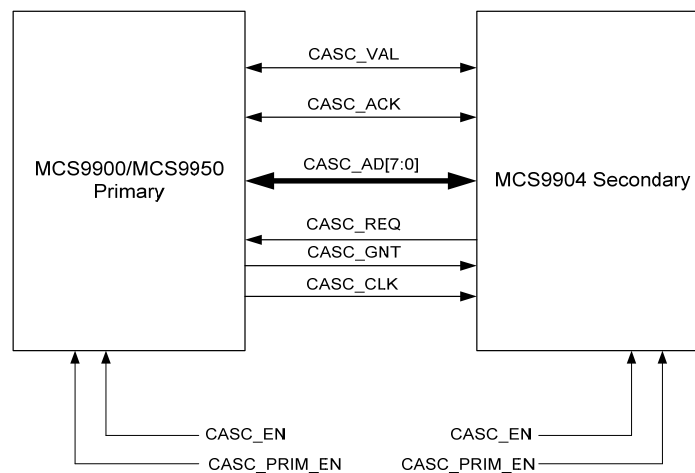
Cascade Interface between Primary and Secondary Devices

In cascade mode, the PCIe endpoint interface is available through the primary MCS9900 device only. The PCIe is disabled on the MCS9904 cascaded secondary device and its access is limited through the cascade interface only. The primary MCS9900 implements a 4-function PCIe end point such that each of these 4 functions serve two serial port, one from primary chip and the other from secondary chip. The following tables list the functions and the corresponding BAR mapping.

BAR Mapping for 8 Serial mode PCIe functions

BAR	Function 0	Function 1	Function 2	Function 3
BAR0	SP1 I/O	SP2 I/O	SP3 I/O	SP4 I/O
BAR1	SP1 Mem	SP2 Mem	SP3 Mem	SP4 Mem
BAR2	-	-	-	-
BAR3	SP5 I/O	SP6 I/O	SP7 I/O	SP8 I/O
BAR4	SP5 Mem	SP6 Mem	SP7 Mem	SP8 Mem
BAR5	GPIO/I2C	GPIO/I2C	GPIO/I2C	GPIO/I2C

BAR Mapping for 6-Serial mode PCIe functions

BAR	Function 0	Function 1	Function 2	Function 3
BAR0	SP1 I/O	SP2 I/O	SP3 I/O	SP4 I/O
BAR1	SP1 Mem	SP2 Mem	SP3 Mem	SP4 Mem
BAR2	-	-	-	-
BAR3	SP5 I/O	SP6 I/O	-	-
BAR4	SP5 Mem	SP6 Mem	-	-
BAR5	GPIO/I2C	GPIO/I2C	-	GPIO/I2C

BAR Mapping for 4-Serial mode PCIe functions

BAR	Function 0	Function 1	Function 2
BAR0	SP1 I/O	SP2 I/O	-
BAR1	SP1 Mem	SP2 Mem	-
BAR2	-	-	-
BAR3	SP3 I/O	SP4 I/O	-
BAR4	SP3 Mem	SP4 Mem	-
BAR5	GPIO/I2C	GPIO/I2C	-

**BAR Mapping for 2 Serial & Other Secondary device mode PCIe functions**

BAR	Function 0	Function 1	Function 2	Function 3
BAR0	SP1 I/O	SP2 I/O	Secondary chip	Secondary chip
BAR1	SP1 Mem	SP2 Mem	Secondary chip	Secondary chip
BAR2	-	-	Secondary chip	Secondary chip
BAR3	-	-	Secondary chip	Secondary chip
BAR4	-	-	Secondary chip	Secondary chip
BAR5	GPIO/I2C	GPIO/I2C	-	GPIO/I2C

1 Serial & Other Secondary device mode PCIe functions

BAR	Function 0	Function 1	Function 2	Function 3
BAR0	SP1 I/O	-	Secondary chip	Secondary chip
BAR1	SP1 Mem	-	Secondary chip	Secondary chip
BAR2	-	-	Secondary chip	Secondary chip
BAR3	-	-	Secondary chip	Secondary chip
BAR4	-	-	Secondary chip	Secondary chip
BAR5	GPIO/I2C	GPIO/I2C	-	GPIO/I2C

Cascade clock connection

In order to meet timing on cascade interface, it is required to send cascade clock out from primary (through CASC_CLK pin) and bring it back using SCAN_MODE pins to both primary and secondary chips through an external onboard connection. Figure below shows the required connections.
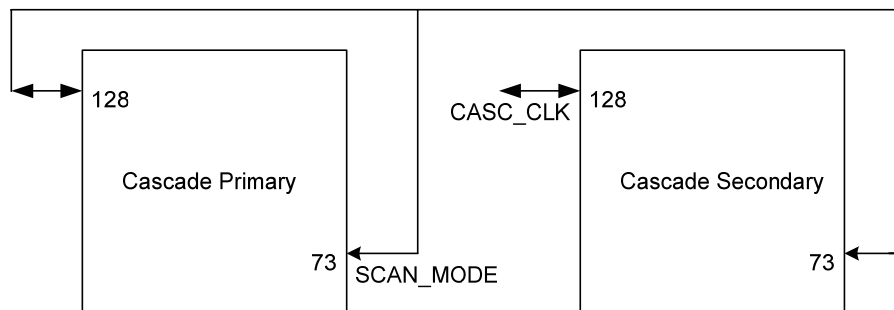
5.7 Clocks and Resets

MCS9904 requires two input clocks. One input clock is sourced from the PCIe connector and the second input clock is sourced from the external crystal. PCIe PHY uses the 100 MHz differential clock from the PCIe connector to generate the internal 125MHz clock. Clock from crystal is used to generate clocks for serial ports.

Crystal Requirement

MCS9904 requires one crystal. This crystal is used to generate serial port clocks. Preferable input frequency is 30 MHz because it allows generating the serial port clock frequency of 96 MHz.

Crystal	Frequency
For Serial Ports	30 MHz

Internal PLLs

MCS9904 uses two PLLs to generate the necessary internal clocks for the device operation. The usage of the PLLs is listed in the following Table.

PLL	Input Frequency	Output Frequency	Used By
PLL1	30 MHz	96 MHz	Serial Port

POR Cell

A POR Cell is used to isolate reset of EEPROM from PCIe reset. It is observed that some PCIe hosts issue multiple PCIe resets. EEPROM read starts automatically on power up. If PCIe reset is used for EEPROM state machines, it causes abrupt resets to EEPROM state machine and may cause it to hang. To avoid this, EEPROM logic is being reset on power-on only. PCIe resets do not affect EEPROM logic.

Side effect of this is that EEPROM logic and the register set that's loaded from EEPROM holds the values till power cycle. If there is a change in EEPROM or EEPROM data, it is required to power cycle in order to get the new values.

5.8 GPIO

There are 8 General Purpose Input/Output pins. All the GPIO pins are interrupt capable. Each GPIO can be configured independent of all other GPIO. The GPIOs allow data input and IRQ generation.
The GPIO Interface register layout can be configured so that the direction of each I/O can be configured using single register for all I/Os.

6   EEPROM Contents Layout

MCS9904 requires an I^2C EEPROM (in 16 bit organization mode) for configuring various sub configurations and device parameters.

EEPROM Address	Parameter	MCS9904 (4S)
0	Signature ID_F0[7:0]	10
1	Signature ID_F0[15:8]	97
2	Vendor ID_F0[7:0]	10
3	Vendor ID_F0[15:8]	97
4	Device ID_F0[7:0]	04
5	Device ID_F0[15:8]	99
6	Revision ID	00
7	Programmable IF_F0	00
8	Sub Class Code_F0	01
9	Class Code_F0	03
10	Sub System Vendor ID_F0[7:0]	00
11	Sub System Vendor ID_F0[15:8]	A0
12	Sub System Device ID_F0[7:0]	00
13	Sub System Device ID_F0[15:8]	40
14	PM_Cap_F0[7:0]	0F
15	PM_Cap_F0[15:8]	06
16	Extended capabilities F0[7:0]	01
17	Extended capabilities F015:8]	00
18	Device Capabilities F0[7:0]	02
19	Device Capabilities F0[15:8]	83
20	Link_Capabilities F0[7:0]	07
21	msi_and_clk_pwr_mgmt_en F0[7:0]	01
22	Interrupt pin F0	01
23	Vendor ID_F1[7:0]	10
24	Vendor ID_F1[15:8]	97
25	Device ID_F1[7:0]	04
26	Device ID_F1[15:8]	99
27	Programmable IF_F1	02
28	Sub Class Code_F1	00
29	Class Code_F1	07
30	Sub System Vendor ID_F1[7:0]	00
31	Sub System Vendor ID_F1[15:8]	A0
32	Sub System Device ID_F1[7:0]	00
33	Sub System Device ID_F1[15:8]	10
34	PM_Cap_F1[7:0]	0F
35	PM_Cap_F1[15:8]	06
36	Extended capabilities F1[7:0]	01
37	Extended capabilities F115:8]	00
38	Device Capabilities F1[7:0]	02
39	Device Capabilities F1[15:8]	83

EEPROM Address	Parameter	MCS9904 (4S)
40	Link_Capabilities F17:0]	07
41	msi_and_clk_pwr_mgmt_en F1[7:0]	19
42	Interrupt pin F1	02
43	Vendor ID_F2[7:0]	10
44	Vendor ID_F2[15:8]	97
45	Device ID_F2[7:0]	04
46	Device ID_F2[15:8]	99
47	Programmable IF_F2	02
48	Sub Class Code_F2	00
49	Class Code_F2	07
50	Sub System Vendor ID_F2[7:0]	00
51	Sub System Vendor ID_F2[15:8]	A0
52	Sub System Device ID_F2[7:0]	00
53	Sub System Device ID_F2[15:8]	10
54	PM_Cap_F2[7:0]	0F
55	PM_Cap_F2[15:8]	06
56	Extended capabilities F2[7:0]	01
57	Extended capabilities F215:8]	00
58	Device Capabilities F2[7:0]	02
59	Device Capabilities F2[15:8]	83
60	Link_Capabilities F2[7:0]	07
61	msi_and_clk_pwr_mgmt_en F2[7:0]	19
62	Interrupt pin F2	03
63	Vendor ID_F3[7:0]	10
64	Vendor ID_F3[15:8]	97
65	Device ID_F3[7:0]	04
66	Device ID_F3[15:8]	99
67	Programmable IF_F3	02
68	Sub Class Code_F3	00
69	Class Code_F3	07
70	Sub System Vendor ID_F3[7:0]	00
71	Sub System Vendor ID_F3[15:8]	A0
72	Sub System Device ID_F3[7:0]	00
73	Sub System Device ID_F3[15:8]	10
74	PM_Cap_F3[7:0]	0F
75	PM_Cap_F3[15:8]	06
76	Extended capabilities F3[7:0]	01
77	Extended capabilities F3[15:8]	00
78	Device Capabilities F3[7:0]	02
79	Device Capabilities F3[15:8]	83
80	Link_Capabilities F3[7:0]	07
81	msi_and_clk_pwr_mgmt_en F3[7:0]	19
82	Interrupt pin F3	04
83	Vendor ID_F4[7:0]	10
84	Vendor ID_F4[15:8]	97

33

EEPROM Address	Parameter	MCS9904 (4S)
85	Device ID_F4[7:0]	04
86	Device ID_F4[15:8]	99
87	Programmable IF_F3	02
88	Sub Class Code_F3	00
89	Class Code_F3	07
90	Sub System Vendor ID_F4[7:0]	00
91	Sub System Vendor ID_F4[15:8]	A0
92	Sub System Device ID_F4[7:0]	00
93	Sub System Device ID_F4[15:8]	10
94	PM_Cap_F4[7:0]	0F
95	PM_Cap_F4[15:8]	06
96	Extended capabilities F4[7:0]	01
97	Extended capabilities F4[15:8]	00
98	Device Capabilities F4[7:0]	02
99	Device Capabilities F4[15:8]	83
100	Link_Capabilities F4[7:0]	07
101	msi_and_clk_pwr_mgmt_en F4[7:0]	19
102	Interrupt pin F4	04
103	INTA Mask register	01
104	INTB Mask Register	02
105	INTC Mask Register	04
106	INTD Mask Register	18
107	Port Disable Register	02
108	Reserved	74
109	Serial port1 Function number	01
110	Serial port2 Function number	02
111	Serial port3 Function number	03
112	Serial port4 Function number	04
113	Reserved	00
114 to 170	bar3,bar4 incase of 3rd party modes	--

Extended Modes through EEPROM

Different product configurations can be selected for MCS9904. By using external EEPROM, more functional configurations can be derived with MCS9904 as listed below.

MCS9904 Possible Product Configuration	EEPROM Required?	Mode Selection at System Level?
1 Serial Port	Yes	No
2 Serial Ports	Yes	No
3 Serial Ports	Yes	No
4 Serial Ports	No	No

# 7   Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Rating	unit
VCCK	1.2V Digital Power Supply	-0.3 to 1.44	V
VCC12A	1.2V Analog Power Supply	-0.3 to 1.44	V
VCC33IO	3.3V Digital Power Supply	-0.3 to 4.0	V
VCC33A	3.3V Analog Power Supply	-0.3 to 4.0	V
T_{stg}	Storage temperature	-40 to 150	^{o}C
To	Operating temperature	0 to 85	^{o}C
Tj	Junction temperature	0 to 125	^{o}C
ESD HBM	(MIL-STD 883E Method 3015-7 Class 2)	2000	V
ESD MM	(JEDEC EIA/JESD22 A115-A)	200	V
CDM	(JEDEC JESD22 C101-A)	500	V
θ_{JA}	Thermal Resistance of Junction to Ambient	52.7	C/W
θ_{JC}	Thermal Resistance of Junction to Case	17.8	C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter	0.54	C/W

C/W – ^{o}C per Watt , For Still Air Condition

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	units
VCCK	1.2V Digital Power Supply	1.08	1.2	1.32	V
VCC12A	1.2V Analog Power Supply	1.08	1.2	1.32	V
VCC33IO	3.3V Digital Power Supply	2.97	3.3	3.63	V
VCC33A	3.3V Analog Power Supply	2.97	3.3	3.63	V
$I_{1.2VD}$	Current in 1.2V Digital Power Supply		65		mA
$I_{1.2VA}$	Current in 1.2V Analog Power Supply		40		mA
$I_{3.3VD}$	Current of 3.3V Digital Power Supply		20		mA
$I_{3.3VA}$	Current in 3.3V Analog Power Supply		75		mA

8   Mechanical Dimensions
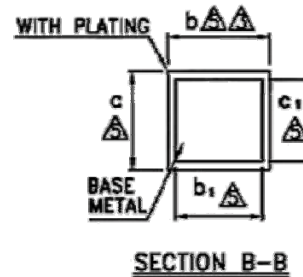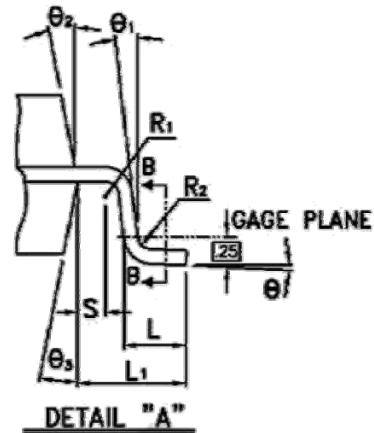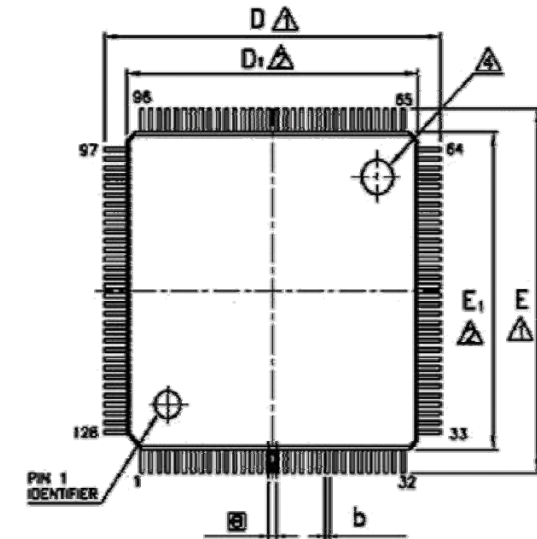
Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	—
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	—	0.20
c1	0.09	—	0.16
D	15.85	16.00	16.15
D1	13.90	14.00	14.10
E	15.85	16.00	16.15
E1	13.90	14.00	14.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	12°TYP		
θ3	12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.

37

Revision History

Revision	Date	Comment
1.0	July 20, 2010	Initial release
2.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram in Section 1.1.

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