MCS9990
PCIe to 4-Port USB 2.0 Host Controller
Datasheet

Revision 3.00
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Notation

The following conventions are used in this document

- A word is 16 bits wide
- A double word or Dword is 32 bits wide
- [x] Denotes the bit position in the register. [0] bit is the least significant position
- Base 16 numbers are denoted with a lowercase 'h' following a number or with a '0x' preceding a number
- Base 10 numbers are denoted with the absence of the above notation
- PU is pull-up on I/O pad
- PD is pull-down on I/O pad
- DS is Drive Strength in milli Amperes (mA)
- N/A is Not Applicable
- PROG is Programmable
- I is Input
- O is Output
- P is Passive
- "_N" means the Signal is active low signal
- RSVD – Reserved

The registers follow the following notation for the read and write access

Name	Description
RO	Read Only
RW	Read Write
RWC	Read/Write 1 to clear
RW1	Read or Write 1 to set
WO	Write Only
RC	Read on clear

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1. Introduction

1.1 General description

MCS9990 is a single lane multi function PCI Express to 4 dedicated USB2.0 host controllers, dedicated bandwidth per port, allowing 4 dedicated USB2.0 host controllers share 2.5Gbps wide PCI Express bus bandwidth. It supports two modes of operation – USB Host mode and OTG mode, selectable through device mode select pins. The USB Host mode supports four USB2.0 Host ports with four dedicated USB host controllers. The OTG mode supports two USB2.0 Host ports, one USB OTG port and provision to select GPIO or ISA interface. The four USB2.0 host ports are integrated with on-chip transceivers and support four dedicated Enhanced Host Controller Interface (EHCI) and four dedicated Open Host Controller Interface (OHCI). The USB OTG port is integrated with OTG PHY and supports host and device operations. The provisional ISA interface supports up to four serial ports and/or up to two parallel ports. The provisional 24 GPIO pins are programmable as an input or output.

1.2 Features

PCI Express

- Single-lane (x1) PCI Express endpoint controller with integrated PHY
- Compliant with PCI Express base specification revision 1.1
- Compliant with PCI Express Card specifications
- Supports multiple DMA transactions
- Supports eight PCI Express functions
- Supports Message TLP (error) generation
- Supports both legacy and MSI Interrupt mechanism

USB

- Four USB 2.0 Host Ports with on-chip transceivers, can handle High-speed (480Mbps), Full-speed (12Mbps) and low-speed (1.5Mbps) transactions
- One of the USB 2.0 Host Port can support OTG Feature
- Four dedicated Enhanced Host Controller Interface (EHCI) controllers
- Four dedicated Companion Open Host Controller Interface (OHCI) controllers
- Compatible with Bulk, Interrupt and Isochronous type USB devices
- Simultaneous operation of multiple high-performance USB devices
- Supports USB Power Management
- As a peripheral, OTG supports High Speed (HS)/ Full Speed (FS) Operation
- As a peripheral, OTG supports the following endpoints
    - One control endpoint
    - One interrupt IN endpoint
    - Two Bulk IN endpoints
    - Two Bulk OUT endpoints

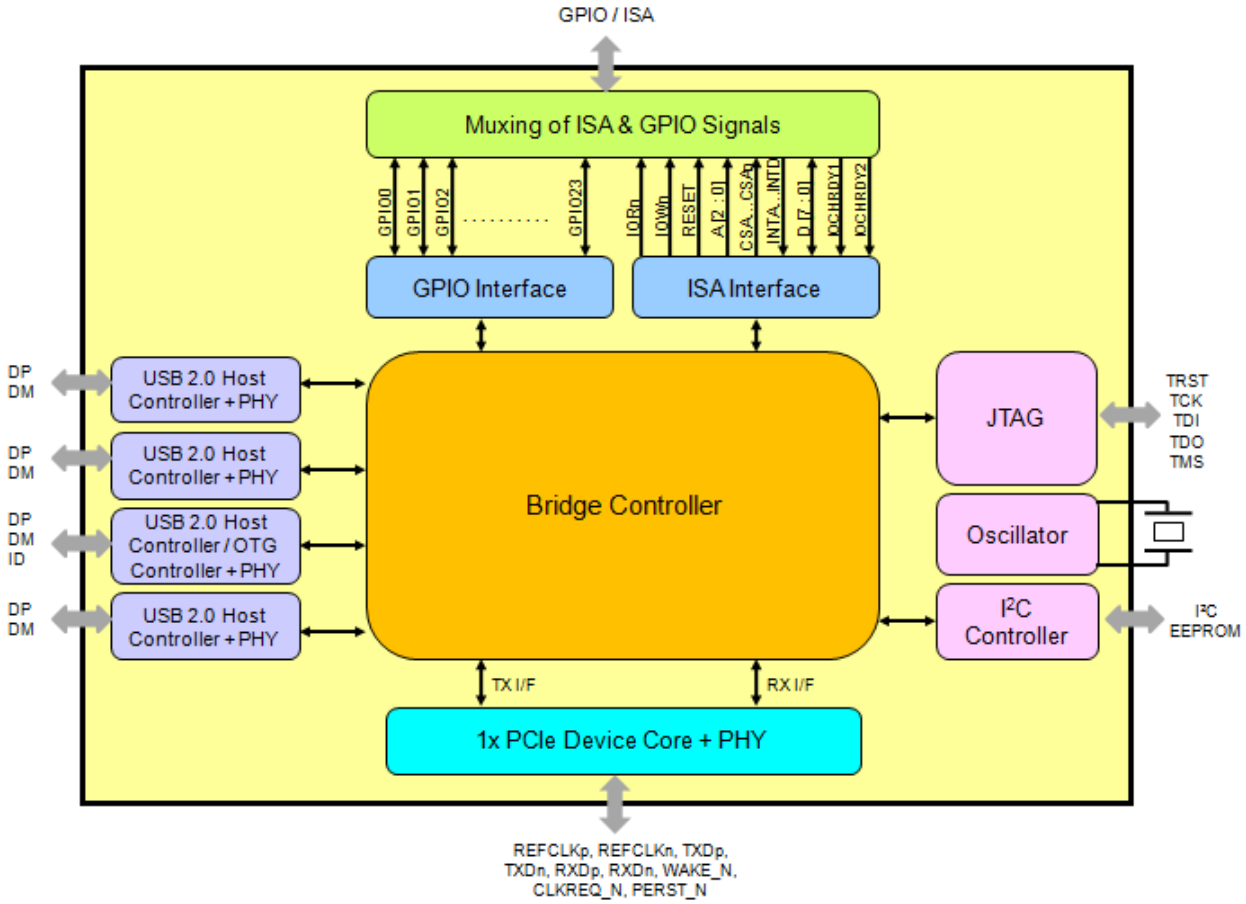
General Device Features

- Device parameters configurable through EEPROM
- 24 GPIO lines
- Optionally GPIO lines are configurable to support ISA Interface
- JTAG Port for board level diagnostics
- Power Supply requirement : 1.2V for Core & 3.3V for IO's
- On-chip Voltage regulator for 3.3V to 1.2V

1.3 Applications

- Extend the USB host/OTG ports on a PC or embedded systems
- Embedded applications for providing multiple USB ports
- Add-on I/O cards for serial port and parallel port through ISA interface
- PC/Server motherboard applications
- Digital Audio/Video applications
- NAS, Printer servers
- Video security monitoring applications

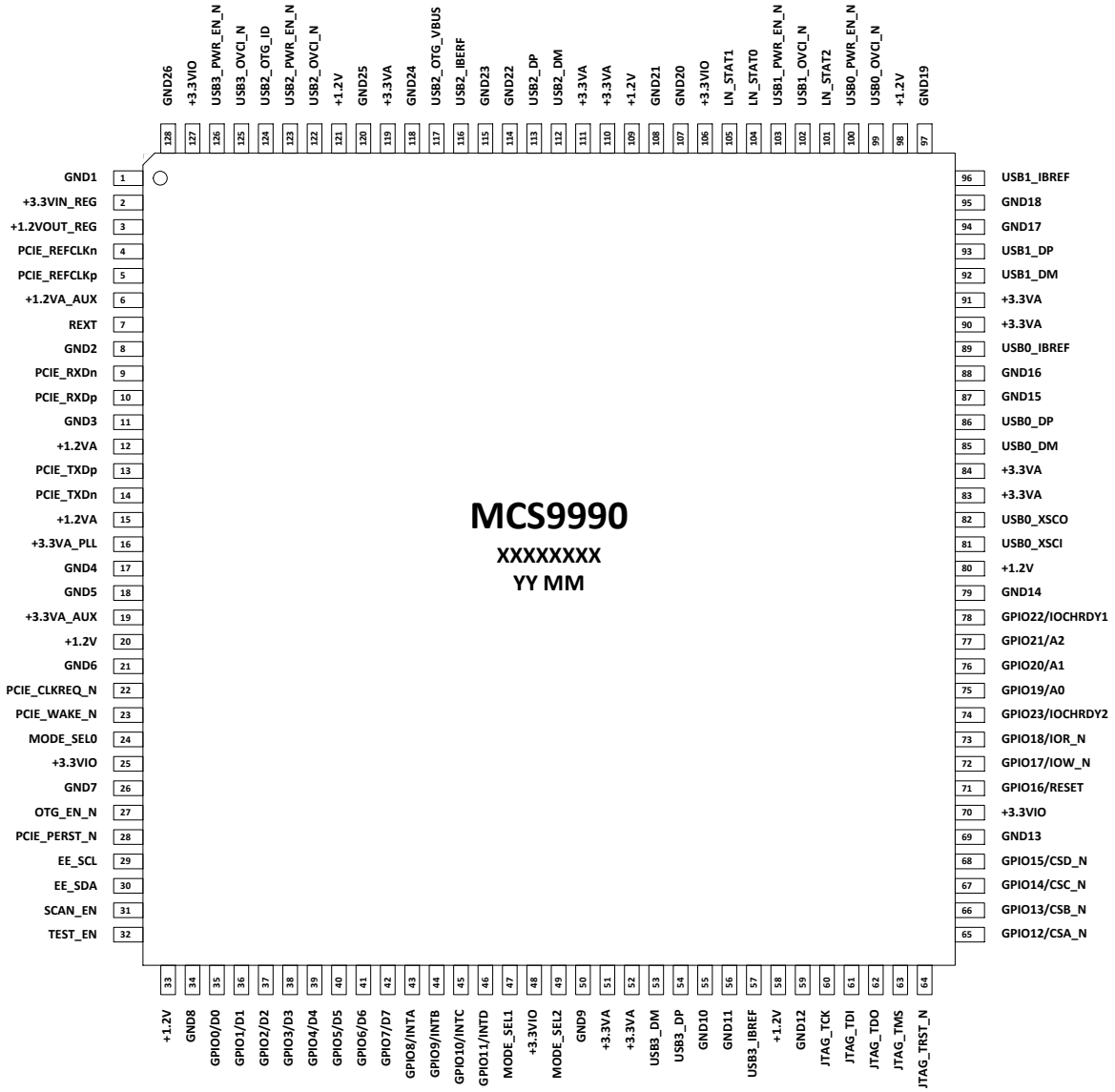
1.4 Block Diagram



1.5 Pin Configuration

- 128-Pin LQFP (14x14)

Top View



Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	GND1	33	+1.2V	65	GPIO12/CSA_N	97	GND19
2	+3.3VIN_REG	34	GND8	66	GPIO13/CSB_N	98	+1.2V
3	+1.2VOUT_REG	35	GPIO0/D0	67	GPIO14/CSC_N	99	USB0_OVCI_N
4	PCIE_REFCLKn	36	GPIO1/D1	68	GPIO15/CSD_N	100	USB0_PWR_EN_N
5	PCIE_REFCLKp	37	GPIO2/D2	69	GND13	101	LN_STAT2
6	+1.2VA_AUX	38	GPIO3/D3	70	+3.3VIO	102	USB1_OVCI_N
7	REXT	39	GPIO4/D4	71	GPIO16/RESET	103	USB1_PWR_EN_N
8	GND2	40	GPIO5/D5	72	GPIO17/IOW_N	104	LN_STAT0
9	PCIE_RXDn	41	GPIO6/D6	73	GPIO18/IOR_N	105	LN_STAT1
10	PCIE_RXDp	42	GPIO7/D7	74	GPIO23/IOCHRDY2	106	+3.3VIO
11	GND3	43	GPIO8/INTA	75	GPIO19/A0	107	GND20
12	+1.2VA	44	GPIO9/INTB	76	GPIO20/A1	108	GND21
13	PCIE_TXDp	45	GPIO10/INTC	77	GPIO21/A2	109	+1.2V
14	PCIE_TXDn	46	GPIO11/INTD	78	GPIO22/IOCHRDY1	110	+3.3VA
15	+1.2VA	47	MODE_SEL1	79	GND14	111	+3.3VA
16	+3.3VA_PLL	48	+3.3VIO	80	+1.2V	112	USB2_DM
17	GND4	49	MODE_SEL2	81	USB0_XSCI	113	USB2_DP
18	GND5	50	GND9	82	USB0_XSCO	114	GND22
19	+3.3VA_AUX	51	+3.3VA	83	+3.3VA	115	GND23
20	+1.2V	52	+3.3VA	84	+3.3VA	116	USB2_IBERF
21	GND6	53	USB3_DM	85	USB0_DM	117	USB2_OTG_VBUS
22	PCIE_CLKREQ_N	54	USB3_DP	86	USB0_DP	118	GND24
23	PCIE_WAKE_N	55	GND10	87	GND15	119	+3.3VA
24	MODE_SEL0	56	GND11	88	GND16	120	GND25
25	+3.3VIO	57	USB3_IBREF	89	USB0_IBREF	121	+1.2V
26	GND7	58	+1.2V	90	+3.3VA	122	USB2_OVCI_N
27	OTG_EN_N	59	GND12	91	+3.3VA	123	USB2_PWR_EN_N
28	PCIE_PERST_N	60	JTAG_TCK	92	USB1_DM	124	USB2_OTG_ID
29	EE_SCL	61	JTAG_TDI	93	USB1_DP	125	USB3_OVCI_N
30	EE_SDA	62	JTAG_TDO	94	GND17	126	USB3_PWR_EN_N
31	SCAN_EN	63	JTAG_TMS	95	GND18	127	+3.3VIO
32	TEST_EN	64	JTAG_TRST_N	96	USB1_IBREF	128	GND26

1.6 Support

Reference Schematics	: Available***
Evaluation Board	: Available***
Software Support	: Available***
System Design Data and Other Technical Collateral	: Available***
Certification	: Already certified for PCIe Compliance through FPGA System

*** Please contact ASIX Support Team for above items, write to support@asix.com.tw

1.7 Ordering Information

Part Number	: MCS9990CV-AA
Operating Temperature	: 0 to 70°C
Package	: 128 LQFP, RoHS

Part Number	: MCS9990IV-AA
Operating Temperature	: -40 to 85°C
Package	: 128 LQFP, RoHS

2. Architectural Overview

MCS9990 is integrated host controller with USB 2.0 transceivers and PCIe interface in to a single chip. It consists of 4 OHCI, 4 EHCI, OTG, ISA, GPIO and I2C cores. MCS9990 compiles with USB specification revision 2.0 and OHCI Interface specification 1.0a for full-/low-speed signaling and Intel's EHCI specification 1.0 for high-speed signaling. MCS9990 contains PCIe PHY compliant with 1.1 PCIe end point controller, 4-port USB and OTG controller and a bridge that controls the transfers between the USB controller and the PCIe interface. In addition, MCS9990 supports an optional ISA interface, I2C, JTAG interface for board testability.

PCIe PHY

This block is a Single-lane transceivers complaint with the PCIe base specification 1.1 and contains the high speed 2.5Gbps differential transmit and receive lines. This block performs the 8b/10b encoding and decoding, etc.

PCIe Endpoint Controller

A PCIe endpoint controller is a device, which is similar to PCI/PCI-X based Host Bus Adapters. A root port needs to establish the linkup, initiate credits and then enumerate the endpoint before the endpoint starts any memory write/read cycles. This PCIe endpoint is fully compliant with PCIe base specification 1.1

PCIe architecture is specified in layers. It is classified into three layers namely transaction layer, data link layer, and physical layer. PCIe configuration uses standard mechanisms as defined in the PCI plug-and-play specification. The software layers will generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based, split-transaction protocol. The link layer adds sequence numbers and CRC to these packets to create a highly reliable data transfer mechanism. The basic physical layer consists of a dual-simplex channel that is implemented as a transmit pair and a receive pair. The link speed of 2.5Gbps/direction provides a 200MBps communication channel that is close to twice the classic PCI data rate.

Bridge Controller

The bridge implements application master and application slave functional modules which take care of transmit and receive PCIe TLPs (Transaction Layer Packets).

Application master interacts with the transmit channels of the PCIe core and the USB host controller core. The data received on the USB interface are packetized by the application master interface as PCIe TLPs and supplied to the PCIe core for transmitting the data onto PCIe lines. The application slave interacts with receive as well as transmit channels of the PCIe core. It takes care of the TLPs received from the PCIe core and redirecting them to appropriate USB port. Also takes care of the completion packets onto PCIe lines using the transmit channel for the PCIe core.

USB 2.0 Host Controllers

MCS9990 supports up to 4 USB 2.0 host ports with dedicated EHCI and OHCI host controllers each port. Each USB host port can be operated at full USB 2.0 bandwidth. This feature significantly improves USB 2.0 performance when multiple USB 2.0 devices are used at the same time and allows multiple USB 2.0 devices to be operated at their maximum capabilities without any performance limitations.

Under the USB Host mode, all 4 USB host controller ports (Port 0 ~ 3) are available. In the USB OTG mode, 1 USB OTG port (Port 2) and 2 USB host controller ports (Port 0/Port 1) are available.

USB OTG Controller

The OTG controller is compliant with USB Specification Rev 2.0 and OTG supplement Rev 1.0a. The host controller supports high (480 Mbps), full (12 Mbps) and low (1.5 Mbps) speed modes of operation. The device controller has two BULK IN and two BULK OUT endpoints, one Control and one Interrupt IN endpoint. The OTG controller supports both host negotiation protocol (HNP) and session request protocol (SRP). HNP is used to transfer control of a connection from the default Host (A-device) to the default peripheral (B-device). The OTG supplement defines two methods that are used by the B-device to request that the A-device to begin a session. They are called "Data-Line Pulsing" and "VBUS pulsing". These two methods comprise the Session Request Protocol (SRP).

ISA Bridge

The ISA interface allows expanding the peripheral IOs, such as UARTs, parallel ports through external ISA interface components. ISA interface can be configured to support both 16 (Intel) mode and 68 (Motorola) Mode Data Bus Interface.

- Configured to support up to 4 UARTs
- Configured to supports parallel port interface
- ISA Interface can support following IO Configurations
  - 1 to 4 UARTs **or** 1 to 2 UARTs + 1 Parallel Port

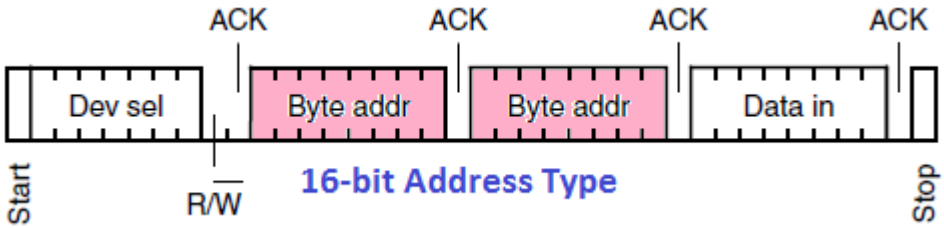
When ISA Mode is selected, MCS9990 assumes the presence of an external "ISA to 4 Serial" peripheral configuration on the ISA interface, for default mode.

GPIO Interface

The MCS9990 supports up to 24 General Purpose I/O (GPIO) pins to be used for system control and connection to various devices. Each GPIO pin can be programmed as an input or output and can also be used as interrupt request lines when programmed to input mode. The GPIO's can be configured as open drain signals in O/P mode. Has programmable internal pull-up capability.

I2C Interface

The MCS9990 supports a 2-wire I2C interface for accessing an external EEPROM that supports both read and write operations. On power-up reset the EEPROM controller checks for the EEPROM presence. If EEPROM is present, controller loads the configuration data from the EEPROM and replaces the corresponding default values. The MCS9990 I2C interface supports two 3.3V I/O signals – Serial Data (SDA) and Serial Clock (SCL) to support 16-bit addressing (as below sample Byte Write instruction figure) 24C32 or higher size I2C EEPROM with frequency rate up to 400 KHz. The I2C EEPROM is required for MCS9990 applications.
Note that the I2C EEPROM is ONLY auto-loaded during MCS9990 power-up reset stage.



3. Pin Description

3.1 PCI Express Interface Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
4	PCIE_REFCLKn	I	LVDS	--	--	PCIe differential clock Negative
5	PCIE_REFCLKp	I	LVDS	--	--	PCIe differential clock Positive
7	REXT	O	Analog	--	--	Band gap external resistor, connect resistor to Ground
9	PCIE_RXDn	I	LVDS	--	--	PCIe differential data Receive Negative with integrated 50-Ω termination resistor to ground
10	PCIE_RXDp	I	LVDS	--	--	PCIe differential data Receive Positive with integrated 50-Ω termination resistor to ground
13	PCIE_TXDp	O	LVDS	--	--	PCIe differential data Transmit Positive
14	PCIE_TXDn	O	LVDS	--	--	PCIe differential data Transmit Negative
22	PCIE_CLKREQ_N	O	LVTTL	4	PU	Active low signal to enable/disable the reference clock of PCIe card. When High, Reference clock is disabled.
23	PCIE_WAKE_N	O	LVTTL	4	PU	Wakeup, Active low signal to request the host platform to return from a sleep/suspended state to service a PCI express function initiated wake event.
28	PCIE_PERST_N	I	LVTTL	--	PU	Fundamental reset from the PCIe connector. Active Low

3.2 USB Interface Signals

3.2.1 Port 0

USB Host Mode – Port will be USB 2.0 Host Port
OTG Mode – Port will be USB 2.0 Host Port

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
81	USB0_XSCI	I	Analog	--	--	Crystal Oscillator Input – 12MHz
82	USB0_XSCO	O	Analog	--	--	Crystal Oscillator Output
85	USB0_DM	I/O	Analog	--	--	USB2.0 differential data negative
86	USB0_DP	I/O	Analog	--	--	USB2.0 differential data positive
89	USB0_IBREF	I	Analog	--	--	External reference resistor (12.1 KΩ, 1%) connect resistor to Ground
99	USB0_OVCI_N	I	LVTTL	--	PU	USB Over Current Indication
100	USB0_PWR_EN_N	O	LVTTL	4	--	USB power enable signal

All the four USB Ports will be sharing the USB0_XSCI and USB0_XSCO.

3.2.2 Port 1

USB Host Mode – Port will be USB 2.0 Host Port
OTG Mode – Port will be USB 2.0 Host Port

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
92	USB1_DM	I/O	Analog	--	--	USB2.0 differential data negative
93	USB1_DP	I/O	Analog	--	--	USB2.0 differential data positive
96	USB1_IBREF	I	Analog	--	--	External reference resistor (12.1KΩ, 1%) connect resistor to Ground
102	USB1_OVCI_N	I	LVTTL	--	PU	USB Over Current Indication
103	USB1_PWR_EN_N	O	LVTTL	4	--	USB power enable signal

3.2.3 Port 2

USB Host Mode – Port will be USB 2.0 Host Port

OTG Mode – Port will be USB OTG Port

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
112	USB2_DM	I/O	Analog	--	--	USB2.0 differential data negative
113	USB2_DP	I/O	Analog	--	--	USB2.0 differential data positive
116	USB2_IBREF	I	Analog	--	--	External reference resistor (12.1KΩ, 1%) connect resistor to Ground
122	USB2_OVCI_N	I	LVTTL	--	PU	USB Over Current Indication
123	USB2_PWR_EN_N	O	LVTTL	4	--	USB power enable signal
124	USB2_OTG_ID	I	LVTTL	--	PROG	Identification pin for OTG ports which differentiates A-Device or B-Device
117	USB2_OTG_VBUS	I	LVTTL	--	--	Voltage detection circuit input

3.2.4 Port 3

USB Host Mode – Port will be USB 2.0 Host Port

OTG Mode – Port will not be available

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
53	USB3_DM	I/O	Analog	--	--	USB2.0 differential data negative
54	USB3_DP	I/O	Analog	--	--	USB2.0 differential data positive
57	USB3_IBREF	I	Analog	--	--	External reference resistor (12.1KΩ, 1%) connect resistor to Ground
125	USB3_OVCI_N	I	LVTTL	--	PU	USB Over Current Indication
126	USB3_PWR_EN_N	O	LVTTL	4	--	USB Power Enable Signal

3.3 ISA/GPIO Interface Signals Description

GPIO and ISA pins are multiplexed. These can be used with combination of OTG and 2 USB Host ports. ISA pins are available in **2USB+OTG+ISA** Mode and GPIO pins in **2USB+OTG+GPIO** Mode.

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
35	D0	I/O	LVTTL	4	PD	Data bus signal at ISA interface
36	D1	I/O	LVTTL	4	PD	Data bus signal at ISA interface
37	D2	I/O	LVTTL	4	PD	Data bus signal at ISA interface
38	D3	I/O	LVTTL	4	PD	Data bus signal at ISA interface
39	D4	I/O	LVTTL	4	PD	Data bus signal at ISA interface
40	D5	I/O	LVTTL	4	PD	Data bus signal at ISA interface
41	D6	I/O	LVTTL	4	PD	Data bus signal at ISA interface
42	D7	I/O	LVTTL	4	PD	Data bus signal at ISA interface
43	INTA	I	LVTTL	4	PU/PD	Interrupt signal coming from Port-A of external peripheral
44	INTB	I	LVTTL	4	PU/PD	Interrupt signal coming from Port-B of external peripheral
45	INTC	I	LVTTL	4	PU/PD	Interrupt signal coming from Port-C of external peripheral
46	INTD	I	LVTTL	4	PU/PD	Interrupt signal coming from Port-D of external peripheral
65	CSA_N	O	LVTTL	4	--	Chip Select line for Port-A of external peripheral
66	CSB_N	O	LVTTL	4	--	Chip Select line for Port-B of external peripheral
67	CSC_N	O	LVTTL	4	--	Chip Select line for Port-C of external peripheral
68	CSD_N	O	LVTTL	4	--	Chip Select line for Port-D of external peripheral
71	RESET	O	LVTTL	4	--	Reset signal for external peripheral at ISA interface
72	IOW_N	O	LVTTL	4	--	Write pulse for external peripheral at ISA interface
73	IOR_N	O	LVTTL	4	--	Read pulse for external peripheral at ISA interface
75	A0	O	LVTTL	4	--	External peripheral Address line
76	A1	O	LVTTL	4	--	External peripheral Address line
77	A2	O	LVTTL	4	--	External peripheral Address line
78	IOCHRDY1	I	LVTTL	4	PU	IOCHRDY coming from Port-A of external peripheral
74	IOCHRDY2	I	LVTTL	4	PU	IOCHRDY coming from Port-C of external peripheral

Note : In Intel mode (default Mode) pads are PD and in Motorola mode pads are PU.

GPIO Interface Signals

Available in **2USB+OTG+GPIO** Mode Only

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
35	GPIO0	I/O	LVTTL	4	PROG	General Purpose I/O Pins
36	GPIO1	I/O	LVTTL	4	PROG	General Purpose I/O Pins
37	GPIO2	I/O	LVTTL	4	PROG	General Purpose I/O Pins
38	GPIO3	I/O	LVTTL	4	PROG	General Purpose I/O Pins
39	GPIO4	I/O	LVTTL	4	PROG	General Purpose I/O Pins
40	GPIO5	I/O	LVTTL	4	PROG	General Purpose I/O Pins
41	GPIO6	I/O	LVTTL	4	PROG	General Purpose I/O Pins
42	GPIO7	I/O	LVTTL	4	PROG	General Purpose I/O Pins
43	GPIO8	I/O	LVTTL	4	PROG	General Purpose I/O Pins
44	GPIO9	I/O	LVTTL	4	PROG	General Purpose I/O Pins
45	GPIO10	I/O	LVTTL	4	PROG	General Purpose I/O Pins
46	GPIO11	I/O	LVTTL	4	PROG	General Purpose I/O Pins
65	GPIO12	I/O	LVTTL	4	PROG	General Purpose I/O Pins
66	GPIO13	I/O	LVTTL	4	PROG	General Purpose I/O Pins
67	GPIO14	I/O	LVTTL	4	PROG	General Purpose I/O Pins
68	GPIO15	I/O	LVTTL	4	PROG	General Purpose I/O Pins
71	GPIO16	I/O	LVTTL	4	PROG	General Purpose I/O Pins
72	GPIO17	I/O	LVTTL	4	PROG	General Purpose I/O Pins
73	GPIO18	I/O	LVTTL	4	PROG	General Purpose I/O Pins
75	GPIO19	I/O	LVTTL	4	PROG	General Purpose I/O Pins
76	GPIO20	I/O	LVTTL	4	PROG	General Purpose I/O Pins
77	GPIO21	I/O	LVTTL	4	PROG	General Purpose I/O Pins
78	GPIO22	I/O	LVTTL	4	PROG	General Purpose I/O Pins
74	GPIO23	I/O	LVTTL	4	PROG	General Purpose I/O Pins

Note: 1. All the GPIO pins can be either PU or open and the PU's are Programmable.
2. All the GPIO/ISA pins should be made as NC's in the other device modes.

3.4 I2C Interface Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
29	EE_SCL	I/O	LVTTL	4	PU	2-Wire EEPROM Clock
30	EE_SDA	I/O	LVTTL	4	PU	2-Wire EEPROM Data In/Out

3.5 Misc Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
27	OTG_EN_N	I	LVTTL	--	PU	Device Mode Select 1 → 4 USB Host Controllers mode 0 → 2 USB Host Controllers, 1 OTG and ISA/GPIO mode
24	MODE_SEL0	I	LVTTL	--	PD	Mode select line
47	MODE_SEL1	I	LVTTL	--	PD	Mode select line
49	MODE_SEL2	I	LVTTL	--	PD	Mode select line
31	SCAN_EN	I	LVTTL	--	PD	Scan Enable signal
32	TEST_EN	I	LVTTL	--	PD	Test Enable signal
104	LN_STAT0	I/O	LVTTL	4	PD	Active high status signal provides information on link up of PCIe interface. Also a Bootstrap Pin
105	LN_STAT1	I/O	LVTTL	4	PD	Active high status signal provides information on configuration of PCIe functions on loading the default / EEPROM contents. Also a bootstrap Pin
101	LN_STAT2	I/O	LVTTL	4	PD	Bootstrap pin. (Please refer to "Bootstrap Options" section)

3.6 JTAG Signals

JTAG interface can be used for board testability

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
60	JTAG_TCK	I	LVTTL	--	--	JTAG chain clock
61	JTAG_TDI	I	LVTTL	--	PU	JTAG chain input
62	JTAG_TDO	O	LVTTL	4	--	JTAG chain output
63	JTAG_TMS	I	LVTTL	--	PU	JTAG chain Test mode select
64	JTAG_TRST_N	I	LVTTL	--	PU	Debug reset signal

3.7 Internal Regulator Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
2	+3.3VIN_REG	I	Power	--	--	Power supply voltage for Voltage Regulator PHY
3	+1.2VOUT_REG	O	Power	--	--	1.2V output voltage

3.8 Power Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
6	+1.2VA_AUX	P	Power	--	--	1.2V Analog auxiliary power for PCIe PHY
19	+3.3VA_AUX	P	Power	--	--	3.3V Analog auxiliary power for PCIe PHY
16	+3.3VA_PLL	P	Power	--	--	3.3V Analog Power Supply for internal PLL used in PCIe PHY
20	+1.2V	P	Power	--	--	1.2V core power supply
33	+1.2V	P	Power	--	--	1.2V core power supply
58	+1.2V	P	Power	--	--	1.2V core power supply
80	+1.2V	P	Power	--	--	1.2V core power supply
98	+1.2V	P	Power	--	--	1.2V core power supply
109	+1.2V	P	Power	--	--	1.2V core power supply
121	+1.2V	P	Power	--	--	1.2V core power supply
12	+1.2VA	P	Power	--	--	1.2V Analog/IO power supply
15	+1.2VA	P	Power	--	--	1.2V Analog/IO power supply
25	+3.3VIO	P	Power	--	--	3.3V Digital IO Power Supply
48	+3.3VIO	P	Power	--	--	3.3V Digital IO Power Supply
70	+3.3VIO	P	Power	--	--	3.3V Digital IO Power Supply
106	+3.3VIO	P	Power	--	--	3.3V Digital IO Power Supply

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
127	+3.3VIO	P	Power	--	--	3.3V Digital IO Power Supply
51	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB3 PHY
52	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB3 PHY
83	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB0 PHY
84	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB0 PHY
90	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB1 PHY
91	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB1 PHY
110	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB2 PHY
111	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB2 PHY
119	+3.3VA	P	Power	--	--	3.3V Analog supply voltage for USB OTG PHY

3.9 Ground Signals

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
1	GND1	P	Ground	--	--	Ground
8	GND2	P	Ground	--	--	Ground
11	GND3	P	Ground	--	--	Ground
17	GND4	P	Ground	--	--	Ground
18	GND5	P	Ground	--	--	Ground
21	GND6	P	Ground	--	--	Ground
26	GND7	P	Ground	--	--	Ground
34	GND8	P	Ground	--	--	Ground
50	GND9	P	Ground	--	--	Ground

Pin#	Pin Name	I/O/P	Type	DS	PU/PD	Description
55	GND10	P	Ground	--	--	Ground
56	GND11	P	Ground	--	--	Ground
59	GND12	P	Ground	--	--	Ground
69	GND13	P	Ground	--	--	Ground
79	GND14	P	Ground	--	--	Ground
87	GND15	P	Ground	--	--	Ground
88	GND16	P	Ground	--	--	Ground
94	GND17	P	Ground	--	--	Ground
95	GND18	P	Ground	--	--	Ground
97	GND19	P	Ground	--	--	Ground
107	GND20	P	Ground	--	--	Ground
108	GND21	P	Ground	--	--	Ground
114	GND22	P	Ground	--	--	Ground
115	GND23	P	Ground	--	--	Ground
118	GND24	P	Ground	--	--	Ground
120	GND25	P	Ground	--	--	Ground
128	GND26	P	Ground	--	--	Ground

Note : All ground signal can be shorted at system level, refer to reference schematics for additional details.

4. Mode Selection and Function Mapping

Mode Selection

MCS9990 supports following four functional modes, selectable through device mode select pins at board level. The I2C EEPROM is also required to be used in these modes.

Mode Selection	TEST_EN	MODE_SEL2	MODE_SEL1	MODE_SEL0	OTG_EN_N
4 USB Host	0	0	0	0	1
2 USB Host + OTG	0	0	0	1	0
2 USB Host + OTG + ISA	0	0	1	0	0
2 USB Host + OTG + GPIO	0	0	1	1	0

Function Mapping

MCS9990 supports four functional modes. All these functional modes have different peripheral mapping with respect to the functions configured by PCIe. In all there are eight functions in all the four modes. Following table shows different function mapping in different functional modes.

Function	4 Host USB	2 USB + OTG	2 USB + OTG + ISA	2 USB + OTG + GPIO
Function 0	OHCI for CH0	OHCI for CH0	OHCI for CH0	OHCI for CH0
Function 1	EHCI for CH0	EHCI for CH0	EHCI for CH0	EHCI for CH0
Function 2	OHCI for CH1	OHCI for CH1	OHCI for CH1	OHCI for CH1
Function 3	EHCI for CH1	EHCI for CH1	EHCI for CH1	EHCI for CH1
Function 4	OHCI for CH2	OHCI for CH2	OHCI for CH2	OHCI for CH2
Function 5	EHCI for CH2	EHCI for CH2	EHCI for CH2	EHCI for CH2
Function 6	OHCI for CH3	OTG for CH2	OTG for CH2	OTG for CH2
Function 7	EHCI for CH3	NA	ISA	GPIO

5. Bootstrap Options

In MCS9990, six bootstrap options are present.

Pin Name	Bootstrap	Internal PU/PD	Default External PU/PD	Description
LN_STAT0	PCIEXP_ERR_MSK	PD	PU	To mask PCIe error bits. By default logic 'Low' is present to mask error reporting
LN_STAT1	MAXRD_128BYTES	PD	Open	To set maximum read request size from EP to be 128 bytes by passing high logic on the line. By default logic 'Low' is present
LN_STAT2	AUX_POWER	PD	PU	For auxiliary power detection, connected to 'Vaux' detect circuit at board level. By default logic 'Low' is present
GPIO19	ASPM_CNTRL	PU	PD	To Provide ASPM support controllability. By default logic 'High' is present to enable ASPM
GPIO20	ADV_ERROR_REPORT	PU	Open	To provide Advance Error Report support controllability. By default logic 'High' is present to enable the feature.
GPIO21	WAKE_HIB_EN	PU	Open	To provide wake from D3 Cold (Hibernate) state through device connected under USB host. By default logic 'High' is present to disable this feature. To enable the feature provide weak pull down at board level.

6. Register Information

6.1 PCIe Configuration Space

6.1.1 PCIe Configuration Space for OHCI Controller 1 - (Function 0)

31 24	23 16	15 8	7 0	
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code	Subclass	Programming Interface	Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
BAR_OHCI Register				10h
Base Address Register 1				14h
Base Address Register 2				18h
Base Address Register 3				1Ch
Base Address Register 4				20h
Base Address Register 5				24h
Card Bus CIS				28h
Subsystem Device ID		Subsystem Vendor ID		2Ch
Expansion ROM				30h
Reserved		Reserved	Capabilities Pointer	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved				40h 4Ch
MSI Control		Next Item Pointer	MSI Capability ID	50h
Message Address				54h
Message Upper Address				58h
Reserved		MSI Data		5Ch
MSI Mask Bits (Optional)				60h
MSI Pending Bits (Optional)				64h
Reserved				68h.. 74h
PMC		Next Item Pointer	PMI Capability ID	78h
Data	PMCSR_BSE	PM Control/Status Register (PMCSR)		7Ch
PCI Express Capabilities Register		Next Item Pointer	PCIe Capability ID	80h
Device Capabilities				84h
Device Status		Device Control		88h
Link Capabilities				8Ch
Link Status		Link Control		90h
Reserved				94h.. FCh
Next Capability Offset/Version		Virtual Channel Capability ID		100h
Port VC Capability Register 1				104h
Port VC Capability Register 2				108h
Port VC Status Register		Port VC Control Register		10Ch
VC Resource Capability Register				110h
VC Resource Control Register				114h
VC Resource Status Register		RsvdP		118h
Reserved				11Ch.. 7FCh
Next Capability Offset/Version		Advanced Error Reporting Capability ID		800h
Uncorrectable Error Status Register				804h
Uncorrectable Error Mask Register				808h
Uncorrectable Error Severity Register				80Ch
Correctable Error Status Register				810h
Correctable Error Mask Register				814h
Advanced Error Capabilities and Control Register				818h
Header Log Register 1				81Ch
Header Log Register 2				820h
Header Log Register 3				824h
Header Log Register 4				828h

6.1.2 PCIe Configuration Space for OHCI Controller 2, 3, and 4 - (Function 2, 4 and 6)

31 24	23 16	15 8	7 0	
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code	Subclass	Programming Interface	Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
BAR_OHCI Register				10h
Base Address Register 1				14h
Base Address Register 2				18h
Base Address Register 3				1Ch
Base Address Register 4				20h
Base Address Register 5				24h
Card Bus CIS				28h
Subsystem Device ID		Subsystem Vendor ID		2Ch
Expansion ROM				30h
Reserved		Reserved	Capabilities Pointer	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved				40h 4Ch
MSI Control		Next Item Pointer	MSI Capability ID	50h
Message Address				54h
Message Upper Address				58h
Reserved		MSI Data		5Ch
MSI Mask Bits (Optional)				60h
MSI Pending Bits (Optional)				64h
Reserved				68h.. 74h
PMC		Next Item Pointer	PMI Capability ID	78h
Data	PMCSR_BSE	PM Control/Status Register (PMCSR)		7Ch
PCI Express Capabilities Register		Next Item Pointer	PCIe Capability ID	80h
Device Capabilities				84h
Device Status		Device Control		88h
Link Capabilities				8Ch
Link Status		Link Control		90h
Reserved				94h.. FCh 7FCh
Next Capability Offset/Version		Advanced Error Reporting Capability ID		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register 1				11Ch
Header Log Register 2				120h
Header Log Register 3				124h
Header Log Register 4				128h

6.1.3 PCI Configuration Space for EHCI Controller 1, 2, 3 and 4 - (Function 1, 3, 5 and 7)

31 24	23 16	15 8	7 0	
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code	Subclass	Programming Interface	Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
USBBASE				10h
Base Address Register 1				14h
Base Address Register 2				18h
Base Address Register 3				1Ch
Base Address Register 4				20h
Base Address Register 5				24h
Card Bus CIS				28h
Subsystem Device ID		Subsystem Vendor ID		2Ch
Expansion ROM				30h
Reserved		Reserved	Capabilities Pointer	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved				40h 4Ch
MSI Control		Next Item Pointer	MSI Capability ID	50h
Message Address				54h
Message Upper Address				58h
Reserved		MSI Data		5Ch
PORTWAKECAP		FLADJ	SBRN	60h
Reserved				64h.. 74h
PMC		Next Item Pointer	PMI Capability ID	78h
Data	PMCSR_BSE	PM Control/Status Register (PMCSR)		7Ch
PCI Express Capabilities Register		Next Item Pointer	PCIe Capability ID	80h
Device Capabilities				84h
Device Status		Device Control		88h
Link Capabilities				8Ch
Link Status		Link Control		90h
Reserved				94h.. FCh
Next Capability Offset/Version		Advanced Error Reporting Capability ID		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register 1				11Ch
Header Log Register 2				120h
Header Log Register 3				124h
Header Log Register 4				128h

6.2 Configuration Register Set

Following are the configuration register values that are loaded into configuration space to setup the hardware resources, device characteristics, etc.

Function	Offset	Register Name	Access
Function 0	00h	F0_DevIDVenID	R
	09h	F0_Classcode	R
	10h	F0_BAR0	RW
	2Ch	F0_SubsysDIDVID	R
	3Dh	F0_IntPinMap	R
	78h	F0_DevCapPwrMgtCap	R
Function 1	00h	F1_DevIDVenID	R
	09h	F1_Classcode	R
	10h	F1_BAR0	RW
	2Ch	F1_SubsysDIDVID	R
	3Dh	F1_IntPinMap	R
	78h	F1_DevCapPwrMgtCap	R
Function 2	00h	F2_DevIDVenID	R
	09h	F2_Classcode	R
	10h	F2_BAR0	RW
	2Ch	F2_SubsysDIDVID	R
	3Dh	F2_IntPinMap	R
	78h	F2_DevCapPwrMgtCap	R
Function 3	00h	F3_DevIDVenID	R
	09h	F3_Classcode	R
	10h	F3_BAR0	RW
	2Ch	F3_SubsysDIDVID	R
	3Dh	F3_IntPinMap	R
	78h	F3_DevCapPwrMgtCap	R
Function 4	00h	F4_DevIDVenID	R

Function	Offset	Register Name	Access
	09h	F4_Classcode	R
	10h	F4_BAR0	RW
	2Ch	F4_SubsysDIDVID	R
	3Dh	F4_IntPinMap	R
	78h	F4_DevCapPwrMgtCap	R
Function 5	00h	F5_DevIDVenID	R
	09h	F5_Classcode	R
	10h	F5_BAR0	RW
	2Ch	F5_SubsysDIDVID	R
	3Dh	F5_IntPinMap	R
	78h	F5_DevCapPwrMgtCap	R
Function 6	00h	F6_DevIDVenID	R
	09h	F6_Classcode	R
	10h	F6_BAR0	RW
	2Ch	F6_SubsysDIDVID	R
	3Dh	F6_IntPinMap	R
	78h	F6_DevCapPwrMgtCap	R
Function 7	00h	F7_DevIDVenID	R
	09h	F7_Classcode	R
	10h	F7_BAR0	RW
	14h	F7_BAR1	RW
	18h	F7_BAR2	RW
	1Ch	F7_BAR3	RW
	20h	F7_BAR4	RW
	2Ch	F7_SubsysDIDVID	R
	3Dh	F7_IntPinMap	R
	78h	F7_DevCapPwrMgtCap	R

6.2.1 Description of Configuration Registers

F0_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-0
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-0
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F0_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-0
		4USB	8'h0C	
		2USB+OTG	8'h0C	
		2USB+OTG+ISA	8'h0C	
		2USB+OTG+GPIO	8'h0C	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-0
		4USB	8'h03	
		2USB+OTG	8'h03	
		2USB+OTG+ISA	8'h03	
		2USB+OTG+GPIO	8'h03	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-0
		4USB	8'h10	
		2USB+OTG	8'h10	
		2USB+OTG+ISA	8'h10	
		2USB+OTG+GPIO	8'h10	
7:0	Rsvd	8'h00		Reserved

F0_BAR0

Bit	Name	Default		Description
31:0	BAR0	**Opmode**	**Value**	Base Address Register-0 field for Function-0
		4USB	32'hFFFF_F000	
		2USB+OTG	32'hFFFF_F000	
		2USB+OTG+ISA	32'hFFFF_F000	
		2USB+OTG+GPIO	32'hFFFF_F000	

F0_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	**Opmode**	**Value**	Sub System Device ID field for Function-0
		4USB	16'h4000	
		2USB+OTG	16'h4000	
		2USB+OTG+ISA	16'h4000	
		2USB+OTG+GPIO	16'h4000	
15:0	SubsysVID	**Opmode**	**Value**	Sub System Vendor ID field for Function-0
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F0_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b001	Interrupt pin [2:0] field for Function-0

F0_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-0
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-0
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-0
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-0
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-0
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-0
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-0
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-0
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-0
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-0
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-0
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-0
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-0
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-0
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-0
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-0

F1_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-1
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-1
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F1_Classcode

Bit	Name	Default		Description
31:24	Classcode	**Opmode**	**Value**	Class code field for Function-1
		4USB	8'h0C	
		2USB+OTG	8'h0C	
		2USB+OTG+ISA	8'h0C	
		2USB+OTG+GPIO	8'h0C	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-1
		4USB	8'h03	
		2USB+OTG	8'h03	
		2USB+OTG+ISA	8'h03	
		2USB+OTG+GPIO	8'h03	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-1
		4USB	8'h20	
		2USB+OTG	8'h20	
		2USB+OTG+ISA	8'h20	
		2USB+OTG+GPIO	8'h20	
7:0	Rsvd	8'h00		Reserved

F1_BAR0

Bit	Name	Default		Description
31:0	BAR0	Opmode	Value	Base Address Register-0 field for Function-1
		4USB	32'hFFFF_FF00	
		2USB+OTG	32'hFFFF_FF00	
		2USB+OTG+ISA	32'hFFFF_FF00	
		2USB+OTG+GPIO	32'hFFFF_FF00	

F1_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	Opmode	Value	Sub System Device ID field for Function-1
		4USB	16'h4000	
		2USB+OTG	16'h4000	
		2USB+OTG+ISA	16'h4000	
		2USB+OTG+GPIO	16'h4000	
15:0	SubsysVID	Opmode	Value	Sub System Vendor ID field for Function-1
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F1_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b001	Interrupt pin [2:0] field for Function-1

F1_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-1
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-1
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-1
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-1
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-1
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-1
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-1
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-1
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-1
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-1
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-1
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-1
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-1
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-1
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-1
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-1

F2_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-2
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-2
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F2_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-2
		4USB	8'h0C	
		2USB+OTG	8'h0C	
		2USB+OTG+ISA	8'h0C	
		2USB+OTG+GPIO	8'h0C	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-2
		4USB	8'h03	
		2USB+OTG	8'h03	
		2USB+OTG+ISA	8'h03	
		2USB+OTG+GPIO	8'h03	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-2
		4USB	8'h10	
		2USB+OTG	8'h10	
		2USB+OTG+ISA	8'h10	
		2USB+OTG+GPIO	8'h10	
7:0	Rsvd	8'h00		Reserved

F2_BAR0

Bit	Name	Default		Description
31:0	BAR0	**Opmode**	**Value**	Base Address Register-0 field for Function-2
		4USB	32'hFFFF_F000	
		2USB+OTG	32'hFFFF_F000	
		2USB+OTG+ISA	32'hFFFF_F000	
		2USB+OTG+GPIO	32'hFFFF_F000	

F2_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	**Opmode**	**Value**	Sub System Device ID field for Function-2
		4USB	16'h4000	
		2USB+OTG	16'h4000	
		2USB+OTG+ISA	16'h4000	
		2USB+OTG+GPIO	16'h4000	
15:0	SubsysVID	**Opmode**	**Value**	Sub System Vendor ID field for Function-2
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F2_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b010	Interrupt pin [2:0] field for Function-2

F2_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-2
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-2
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-2
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-2
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-2
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-2
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-2
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-2
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-2
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-2
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-2
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-2
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-2
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-2
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-2
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-2

F3_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-3
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-3
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F3_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-3
		4USB	8'h0C	
		2USB+OTG	8'h0C	
		2USB+OTG+ISA	8'h0C	
		2USB+OTG+GPIO	8'h0C	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-3
		4USB	8'h03	
		2USB+OTG	8'h03	
		2USB+OTG+ISA	8'h03	
		2USB+OTG+GPIO	8'h03	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-3
		4USB	8'h20	
		2USB+OTG	8'h20	
		2USB+OTG+ISA	8'h20	
		2USB+OTG+GPIO	8'h20	
7:0	Rsvd	8'h00		Reserved

F3_BAR0

Bit	Name	Default		Description
31:0	BAR0	Opmode	Value	Base Address Register-0 field for Function-3
		4USB	32'hFFFF_FF00	
		2USB+OTG	32'hFFFF_FF00	
		2USB+OTG+ISA	32'hFFFF_FF00	
		2USB+OTG+GPIO	32'hFFFF_FF00	

F3_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	Opmode	Value	Sub System Device ID field for Function-3
		4USB	16'h4000	
		2USB+OTG	16'h4000	
		2USB+OTG+ISA	16'h4000	
		2USB+OTG+GPIO	16'h4000	
15:0	SubsysVID	Opmode	Value	Sub System Vendor ID field for Function-3
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F3_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b010	Interrupt pin [2:0] field for Function-3

F3_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-3
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-3
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-3
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-3
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-3
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-3
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-3
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-3
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-3
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-3
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-3
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-3
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-3
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-3
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-3
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-3

F4_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-4
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-4
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F4_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-4
		4USB	8'h0C	
		2USB+OTG	8'h0C	
		2USB+OTG+ISA	8'h0C	
		2USB+OTG+GPIO	8'h0C	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-4
		4USB	8'h03	
		2USB+OTG	8'h03	
		2USB+OTG+ISA	8'h03	
		2USB+OTG+GPIO	8'h03	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-4
		4USB	8'h10	
		2USB+OTG	8'h10	
		2USB+OTG+ISA	8'h10	
		2USB+OTG+GPIO	8'h10	
7:0	Rsvd	8'h00		Reserved

F4_BAR0

Bit	Name	Default		Description
31:0	BAR0	Opmode	Value	Base Address Register-0 field for Function-4
		4USB	32'hFFFF_F000	
		2USB+OTG	32'hFFFF_F000	
		2USB+OTG+ISA	32'hFFFF_F000	
		2USB+OTG+GPIO	32'hFFFF_F000	

F4_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	Opmode	Value	Sub System Device ID field for Function-4
		4USB	16'h4000	
		2USB+OTG	16'h4000	
		2USB+OTG+ISA	16'h4000	
		2USB+OTG+GPIO	16'h4000	
15:0	SubsysVID	Opmode	Value	Sub System Vendor ID field for Function-4
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F4_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b011	Interrupt pin [2:0] field for Function-4

F4_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-4
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-4
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-4
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-4
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-4
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-4
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-4
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-4
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-4
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-4
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-4
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-4
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-4
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-4
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-4
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-4

F5_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-5
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-5
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F5_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-5
		4USB	8'h0C	
		2USB+OTG	8'h0C	
		2USB+OTG+ISA	8'h0C	
		2USB+OTG+GPIO	8'h0C	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-5
		4USB	8'h03	
		2USB+OTG	8'h03	
		2USB+OTG+ISA	8'h03	
		2USB+OTG+GPIO	8'h03	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-5
		4USB	8'h20	
		2USB+OTG	8'h20	
		2USB+OTG+ISA	8'h20	
		2USB+OTG+GPIO	8'h20	
7:0	Rsvd	8'h00		Reserved

F5_BAR0

Bit	Name	Default		Description
31:0	BAR0	Opmode	Value	Base Address Register-0 field for Function-5
		4USB	32'hFFFF_FF00	
		2USB+OTG	32'hFFFF_FF00	
		2USB+OTG+ISA	32'hFFFF_FF00	
		2USB+OTG+GPIO	32'hFFFF_FF00	

F5_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	Opmode	Value	Sub System Device ID field for Function-5
		4USB	16'h4000	
		2USB+OTG	16'h4000	
		2USB+OTG+ISA	16'h4000	
		2USB+OTG+GPIO	16'h4000	
15:0	SubsysVID	Opmode	Value	Sub System Vendor ID field for Function-5
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F5_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b011	Interrupt pin [2:0] field for Function-5

F5_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-5
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-5
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-5
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-5
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-5
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-5
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-5
15:11	Rsvd	5'd0	
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-5
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-5
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-5
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-5
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-5
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-5
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-5
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-5
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-5

F6_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-6
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-6
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F6_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-6
		4USB	8'h0C	
		2USB+OTG	8'hFF	
		2USB+OTG+ISA	8'hFF	
		2USB+OTG+GPIO	8'hFF	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-6
		4USB	8'h03	
		2USB+OTG	8'h00	
		2USB+OTG+ISA	8'h00	
		2USB+OTG+GPIO	8'h00	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-6
		4USB	8'h10	
		2USB+OTG	8'h00	
		2USB+OTG+ISA	8'h00	
		2USB+OTG+GPIO	8'h00	
7:0	Rsvd	8'h00		Reserved

F6_BAR0

Bit	Name	Default		Description
31:0	BAR0	Opmode	Value	Base Address Register-0 field for Function-6
		4USB	32'hFFFF_F000	
		2USB+OTG	32'hFFFF_F000	
		2USB+OTG+ISA	32'hFFFF_F000	
		2USB+OTG+GPIO	32'hFFFF_F000	

F6_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	Opmode	Value	Sub System Device ID field for Function-6
		4USB	16'h4000	
		2USB+OTG	16'h5000	
		2USB+OTG+ISA	16'h5000	
		2USB+OTG+GPIO	16'h5000	
15:0	SubsysVID	Opmode	Value	Sub System Vendor ID field for Function-6
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F6_IntPinMap

Bit	Name	Default		Description
31:3	Rsvd			Reserved
2:0	IntPinMap	Opmode	Value	Interrupt pin [2:0] field for Function-6
		4USB	3'b100	
		2USB+OTG	3'b011	
		2USB+OTG+ISA	3'b011	
		2USB+OTG+GPIO	3'b011	

F6_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-6
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-6
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-6
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-6
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-6
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-6
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-6
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-6
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-6
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-6
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-6
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-6
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-6
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-6
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-6
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-6

F7_DevIDVenID

Bit	Name	Default		Description
31:16	DevID	**Opmode**	**Value**	Device ID field for Function-7
		4USB	16'h9990	
		2USB+OTG	16'h9990	
		2USB+OTG+ISA	16'h9990	
		2USB+OTG+GPIO	16'h9990	
15:0	VenID	**Opmode**	**Value**	Vendor ID field for Function-7
		4USB	16'h9710	
		2USB+OTG	16'h9710	
		2USB+OTG+ISA	16'h9710	
		2USB+OTG+GPIO	16'h9710	

F7_Classcode

Bit	Name	Default		Description
31:24	ClassCode	**Opmode**	**Value**	Class code field for Function-7
		4USB	8'h0C	
		2USB+OTG	8'h00	
		2USB+OTG+ISA	8'h07	
		2USB+OTG+GPIO	8'hFF	
23:16	SubClassCode	**Opmode**	**Value**	Sub Class Code field for Function-7
		4USB	8'h03	
		2USB+OTG	8'h00	
		2USB+OTG+ISA	8'h80	
		2USB+OTG+GPIO	8'h00	
15:8	ProgIntfInfo	**Opmode**	**Value**	Programming Interface Information field for Function-7
		4USB	8'h20	
		2USB+OTG	8'h00	
		2USB+OTG+ISA	8'h00	
		2USB+OTG+GPIO	8'h01	
7:0	Rsvd	8'h00		Reserved

F7_BAR0

Bit	Name	Default		Description
		Opmode	Value	
31:0	BAR0	4USB	32'hFFFF_FF00	Base Address Register-0 field for Function-7
		2USB+OTG	32'h0000_0000	
		2USB+OTG+ISA	32'hFFFF_FFF9	
		2USB+OTG+GPIO	32'hFFFF_FF00	

F7_BAR1

Bit	Name	Default		Description
		Opmode	Value	
31:0	BAR1	4USB	32'h0000_0000	Base Address Register-1 field for Function-7
		2USB+OTG	32'h0000_0000	
		2USB+OTG+ISA	32'hFFFF_FFF9	
		2USB+OTG+GPIO	32'h0000_0000	

F7_BAR2

Bit	Name	Default		Description
		Opmode	Value	
31:0	BAR2	4USB	32'h0000_0000	Base Address Register-2 field for Function-7
		2USB+OTG	32'h0000_0000	
		2USB+OTG+ISA	32'hFFFF_FFF9	
		2USB+OTG+GPIO	32'h0000_0000	

F7_BAR3

Bit	Name	Default		Description
		Opmode	Value	
31:0	BAR3	4USB	32'h0000_0000	Base Address Register-3 field for Function-7
		2USB+OTG	32'h0000_0000	
		2USB+OTG+ISA	32'hFFFF_FFF9	
		2USB+OTG+GPIO	32'h0000_0000	

F7_BAR4

Bit	Name	Default		Description
31:0	BAR4	Opmode	Value	Base Address Register-4 field for Function-7
		4USB	32'h0000_0000	
		2USB+OTG	32'h0000_0000	
		2USB+OTG+ISA	32'hFFFF_F000	
		2USB+OTG+GPIO	32'h0000_0000	

F7_SubsysDIDVID

Bit	Name	Default		Description
31:16	SubsysDID	Opmode	Value	Sub System Device ID field for Function-7
		4USB	16'h4000	
		2USB+OTG	16'h0000	
		2USB+OTG+ISA	16'h3004	
		2USB+OTG+GPIO	16'h6000	
15:0	SubsysVID	Opmode	Value	Sub System Vendor ID field for Function-7
		4USB	16'hA000	
		2USB+OTG	16'hA000	
		2USB+OTG+ISA	16'hA000	
		2USB+OTG+GPIO	16'hA000	

F7_IntPinMap

Bit	Name	Default	Description
31:3	Rsvd	29'd0	Reserved
2:0	IntPinMap	3'b100	Interrupt pin [2:0] field for Function-7

F7_DevCapPwrMgtCap

Bit	Name	Default	Description
31	DevCap	1'b0	Reserved
30:28		3'b000	[14:12] bit field of Device Capability Register for Function-7
27:25		3'b111	Endpoint L1 Acceptable Latency = [11:9] bit field of Device Capability Register for Function-7
24:22		3'b111	Endpoint L0s Acceptable Latency = [8:6] bit field of Device Capability Register for Function-7
21		1'b0	Extended Tag field supported = [5] bit field of Device Capability Register for Function-7
20		1'b0	DLL Link active reporting Capable = [20] field of Link Capability Register for Function-7
19		1'b0	Surprise down error reporting Capable = [19] field of Link Capability Register for Function-7
18:16		3'b001	Max Payload Size Supported = [2:0] bit field of Device Capability Register for Function-7
15:11	Rsvd	5'd0	Reserved
10	PwrMgtCap	1'b0	D3 cold Support = [31] bit field of Power Management Capability Register for Function-7
9		1'b0	D3 hot PME Support = [30] bit field of Power Management Capability Register for Function-7
8		1'b0	D2 PME Support = [29] bit field of Power Management Capability Register for Function-7
7		1'b0	D1 PME Support = [28] bit field of Power Management Capability Register for Function-7
6		1'b0	D0 PME Support = [27] bit field of Power Management Capability Register for Function-7
5		1'b0	D2 Support = [26] bit field of Power Management Capability Register for Function-7
4		1'b0	D1 Support = [25] bit field of Power Management Capability Register for Function-7
3:1		3'b111	AUX current = [24:22] bit field of Power Management Capability Register for Function-7
0		1'b1	No Soft Reset = [3] bit field of Power Management Status/Control Register for Function-7

6.3 OHCI Register Set

The Host Controller (HC) contains a set of operational registers which are mapped into system memory space. According to the function of these registers, they are divided into four partitions, specifically Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as DWORD's (DW). Address to access these registers is calculated by adding **BAR0** base address of OHCI function to the offset mentioned below.

BAR0 (of OHCI function) + <Offset>

Control and Status Register

Offset	Register Name	Default Value	Access
00-03h	HcRevision	32'h0000_0010	RO
04-07h	HcControl	32'h0000_0000	RW
08-0Bh	HcCommandStatus	32'h0000_0000	RW
0C-0Fh	HcInterruptStatus	32'h0000_0000	RW
10-13h	HcInterruptEnable	32'h0000_0000	RW
14-17h	HcInterruptDisable	32'h0000_0000	RW

Memory Pointer Register

Offset	Register Name	Default Value	Access
18-1Bh	HcHCCA	32'h0000_0000	RO
1C-1Fh	HcPeriodCurrentED	32'h0000_0000	RW
20-23h	HcControlHeadED	32'h0000_0000	RW
24-27h	HcControlCurrentED	32'h0000_0000	RW
28-2Bh	HcBulkHeadED	32'h0000_0000	RW
2C-2Fh	HcBulkCurrentED	32'h0000_0000	RW
30-33h	HcDoneHead	32'h0000_0000	RW

Frame Counter Register

Offset	Register Name	Default Value	Access
34-37h	HcFmInterval	32'h0000_2EDF	RW
38-3Bh	HcFmRemaining	32'h0000_0000	RW
3C-3Fh	HcFmNumber	32'h0000_0000	RW
40-43h	HcPeriodicStart	32'h0000_0000	RW
44-47h	HcLSThreshold	32'h0000_0628	RW

Root Hub Register

Offset	Register Name	Default Value	Access
48-4Bh	HcRhDescriptorA	Implementation Specific	RW
4C-4Fh	HcRhDescriptorB	Implementation Specific	RW
50-53h	HcRhStatus	32'h0000_0000	RW
54-57h	HcRhPortStatus1	32'h0000_0000	RW

6.3.1 Description of OHCI Operational Registers

HcRevision

Key	Bit	Reset	HCD /HC	Description
REV	7:0	10h	R / R	Revision: This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this OHC. For example, a value of 11h corresponds to version 1.1.
Rsvd	31:8			Reserved

HcControl

The HcControl register defines the operating modes for the Host Controller. Most of the fields in this register are modified only by the Host Controller Driver, except Host Controller Functional State and Remote Wakeup Connected.

Key	Bit	Reset	HCD/HC	Description
CBSR	1:0	00b	RW / R	Control Bulk Service Ratio This specifies the service ratio between Control and Bulk EDs. Before processing any of the non periodic lists, OHC compares the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs .The internal count will be retained when crossing the frame boundary. CBSR | no. of Control EDs Over BulkEDs served 0 1 : 1 1 2 : 1 2 3 : 1 3 4 : 1
PLE	2	0b	RW / R	Periodic List Enable This bit is set to enable the processing of the periodic list in the next Frame. OHC must check this bit before it starts processing the list.

Key	Bit	Reset	HCD/HC	Description
IE	3	0b	RW/R	Isochronous Enable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, OHC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), OHC continues processing the EDs. If cleared (disabled), OHC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.
CLE	4	0b	RW/R	Control List Enable This bit is set to enable the processing g of the Control list in the next Frame. OHC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list.
BLE	5	0b	RW/R	Bulk List Enable This bit is set to enable the processing of the Bulk list in the next Frame. OHC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list.
HCFS	7:6	00b	RW/RW	Host Controller Functional State for USB 00b: USBRESET 01b: USBRESUME 10b: USBOPERATIONAL 11b: USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1ms later. HCD may determine whether OHC has begun sending SOFs by reading the Start of Frame field of HcInterruptStatus. This field may be changed by OHC only when in the USBSUSPEND state. OHC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. OHC enters USBSUSPEND after software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.

Key	Bit	Reset	HCD/HC	Description
IR	8	0b	RW/R	Interrupt Routing This bit determines the routing of interrupts generated by event registered in HcInterruptStatus. If clear, all interrupts are routed to the normal host bus interrupt mechanism i.e. INT pin. If set, interrupts are routed to the System Management Interrupt.
RWC	9	0b	RW/ RW	Remote Wakeup Connected This bit indicates whether OHC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during POST. OHC clears the bit upon a hardware reset but does not alter it upon a software reset.
RWE	10	0b	RW/R	Remote Wakeup Enable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the Resume Detected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
Rsvd	31:11			Reserved

HcCommandStatus

The HcCommandStatus register is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the Host Controller. The Scheduling Overrun Count field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host Controller increments the counter and sets the Scheduling Overrun field in the HcInterruptStatus register.

Key	Bit	Reset	HCD/HC	Description
HCR	0	0b	RW/ RW	HostControllerReset This bit is set by HCD to initiate a software reset of OHC. Regardless of the functional state of OHC, it moves to the USBSUSPEND state in which most of the operational registers are reset except those stated otherwise;

Key	Bit	Reset	HCD/HC	Description
CLF	1	0b	RW/ RW	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When OHC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, OHC will not start processing the Control list. If CF is 1, OHC will start processing the Control list and will set ControlListFilled to 0. If the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when OHC completes processing the Control list and Control list processing will stop.
BLF	2	0b	RW/ RW	BulkListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When OHC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BLF to 0. If HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
OCR	3	0b	RW/ RW	Ownership Change Request This bit is set by an HCD to request a change of control of the OHC. When set OHC will set the Ownership Change field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from HCD.
Rsvd	15:4			Reserved
SOC	17:16	00b	R/ RW	Scheduling Overrun Count These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if Scheduling Overrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problems.
Rsvd	31:18			Reserved

HcInterruptstatus

This register provides status on various events that cause hardware interrupts. When an event occurs, Host Controller sets the corresponding bit in this register. When a bit becomes set, a hardware interrupt is generated if the interrupt is enabled in the HcInterruptEnable register and the MasterInterruptEnable bit is set. The Host Controller Driver may clear specific bits in this register by writing '1' to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The Host Controller will never clear the bit.

Key	Bit	Reset	HCD/HC	Description
SO	0	0b	RW/ RW	Scheduling Overrun This bit is set when the USB schedule for the current Frame overruns .A scheduling overrun will also cause the Scheduling Overrun Count of HcCommandStatus to be incremented.
WDH	1	0b	RW/RW	WritebackDoneHead This bit is set immediately after OHC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
SF	2	0b	RW/ RW	Start of Frame This bit is set by OHC at each start of a frame and after the update of HccaFrameNumber. OHC also generates a SOF token at the same time.
RD	3	0b	RW/ RW	Resume Detected This bit is set when OHC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRESUME state.
UE	4	0b	RW/ RW	UnrecoverableError This bit is set when OHC detects a system error not related to USB. OHC should not proceed with any processing or signaling before the system error has been corrected. HCD clears this bit after OHC has been reset.
FNO	5	0b	RW/ RW	FrameNumberOverflow This bit is set when the MSB of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.

Key	Bit	Reset	HCD/HC	Description
RHSC	6	0b	RW/ RW	RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
OC	30	0b	RW/ RW	Ownership Change This bit is set by HC when HCD sets the Ownership Change Request field in HcCommandStatus. This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.
Rsvd	29:7			Reserved

HcInterruptEnable

Each enable bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control which events generate a hardware interrupt. When a bit is set in the HcInterruptStatus register AND the corresponding bit in the HcInterruptEnable register is set AND the MasterInterruptEnable bit is set, then a hardware interrupt is requested on the host bus.

Key	Bit	Reset	HCD/HC	Description
SO	0	0b	RW/ R	Scheduling Overrun 0 – Ignore 1 – Enable interrupts generation due to Scheduling Overrun.
WDH	1	0b	RW/R	WritebackDoneHead 0 – Ignore 1 – Enable interrupts generation due to HcDoneHead Write back.
SF	2	0b	RW/ R	Start of Frame 0 – Ignore 1 – Enable interrupts generation due to Start of Frame.
RD	3	0b	RW/R	Resume Detected 0 – Ignore 1 – Enable interrupts generation due to Resume Detect.
UE	4	0b	RW/R	UnrecoverableError 0 – Ignore 1 – Enable interrupts generation due to Unrecoverable Error.

Key	Bit	Reset	HCD/HC	Description
FNO	5	0b	RW/R	FrameNumberOverflow 0 – Ignore 1 – Enable interrupts generation due to Frame Number Overflow.
RHSC	6	0b	RW/R	RootHubStatusChange 0 – Ignore 1 – Enable interrupts generation due to Root Hub Status Change.
OC	30	0b	RW/R	Ownership Change 0 – Ignore 1 – Enable interrupts generation due to Ownership Change.
MIE	31	0b	RW/R	MasterInterruptEnable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.
Rsvd	29:7			Reserved

HcInterruptDisable

Each disable bit in the HcInterrupJTAG_TDisable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterrupJTAG_TDisable register is coupled with the HcInterruptEnable register. Thus, writing a '1' to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing a '0' to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged. On read, the current value of the HcInterruptEnable register is returned.

Key	Bit	Reset	HCD/HC	Description
SO	0	0b	RW/ R	Scheduling Overrun 0 – Ignore 1 – Disable interrupts generation due to Scheduling Overrun.
WDH	1	0b	RW/ R	WritebackDoneHead 0 – Ignore 1 – Disable interrupts generation due to HcDoneHead Write back.
SF	2	0b	RW/ R	Start of Frame 0 – Ignore 1 – Disable interrupts generation due to Start of Frame.

Key	Bit	Reset	HCD/HC	Description
RD	3	0b	RW/ R	Resume Detected 0 – Ignore 1 – Disable interrupts generation due to Resume Detect.
UE	4	0b	RW/ R	UnrecoverableError 0 – Ignore 1 – Disable interrupts generation due to Unrecoverable Error.
FNO	5	0b	RW/ R	FrameNumberOverflow 0 – Ignore 1 – Disable interrupts generation due to Frame Number Overflow.
RHSC	6	0b	RW/ R	RootHubStatusChange 0 – Ignore 1 – Disable interrupts generation due to Root Hub Status Change.
Rsvd	29:7	0		Reserved
OC	30	0b	RW/ R	Ownership Change 0 – Ignore 1 – Disable interrupts generation due to Ownership Change.
MIE	31	0b	RW/ R	MasterInterruptEnable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.

HcHCCA

The HcHCCA register contains the physical address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Open Host Controller and the Host Controller Driver.

Key	Bit	Reset	HCD/HC	Description
HCCA	31:8	0x400F_D1 (OHCI1) 0x400F_E1 (OHCI2)	R/R	Host Controller Communication Area This is the base address of the Host Controller Communication Area.
Rsvd	7:0	0	R/R	Reserved

HcPeriodCurrentED

The HcPeriodCurrentED register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Key	Bit	Reset	HCD/HC	Description
PCED	31:4	0h	R/ RW	PeriodCurrentED This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
Rsvd	3:0	0h		Reserved

HcControlHeadED

The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list.

Key	Bit	Reset	HCD/HC	Description
CHED	31:4	0h	RW/ R	ControlHeadED OHC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
Rsvd	3:0	0h		Reserved

HcControlCurrentED

Key	Bit	Reset	HCD/HC	Description
CCED	31:4	0h	RW/ RW	ControlCurrentED This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the Control List Enable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
Rsvd	3:0	0h		Reserved

HcBulkHeadED

The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list.

Key	Bit	Reset	HCD/HC	Description
BHED	31:4	0h	RW/R	BulkHeadED HC traverses the Bulk list starting with the HcBulkHeadED pointer.
Rsvd	3:0	0h		Reserved

HcBulkCurrentED

The HcBulkCurrentED register contains the physical address of the current endpoint of the Bulk list.

Key	Bit	Reset	HCD/HC	Description
BCED	31:4	0h	RW/ RW	BulkCurrentED This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the Bulk List Enable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
Rsvd	3:0	0h		Reserved

HcDoneHead

The HcDoneHead register contains the physical address of the last completed Transfer Descriptor that was added to the done queue. In normal operation, the Host Controller Driver should not need to read this register as its content is periodically written to the HCCA.

Key	Bit	Reset	HCD/HC	Description
DH	31:4	0h	R/RW	DoneHead When a TD is completed, HC writes the content of HcDoneHead to the Next TD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the write back Done Head of HcInterruptStatus.
Rsvd	3:0	0h		Reserved

HcFmInterval

The HcFmInterval register contains a 14-bit value which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the Host Controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustment on the Frame Interval by writing a new value over the present one at each SOF. This provides the programmability necessary for the Host Controller to synchronize with an external clocking resource.

Key	Bit	Reset	HCD/HC	Description
FI	13:0	2EDFh	RW/ R	Frame Interval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.
Rsvd	15:14	0h		Reserved
FSMPS	30:16	-	RW/ R	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
FIT	31	0b	RW/ R	FrameIntervalToggle HCD toggles this bit whenever it loads a new value to Frame Interval.

HcFmRemaining

The HcFmRemaining register is a 14-bit down counter showing the bit time remaining in the current Frame.

Key	Bit	Reset	HCD /HC	Description
FR	13:0	0h	R/RW	Frame Remaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the Frame Interval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the Frame Interval of HcFmInterval and uses the updated value from the next SOF.
Rsvd	30:14	0h		Reserved
FRT	31	0b	R/RW	Frame Remaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever Frame Remaining reaches 0. This bit is used by HCD for the synchronization between Frame Interval and Frame Remaining.

HcFmNumber

The HcFmNumber register is a 16-bit counter. It provides a timing reference among events happening in the Host Controller and the Host Controller Driver.

Key	Bit	Reset	HCD/HC	Description
FN	15:0	0h	R/RW	Frame Number This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When entering the USBOPERATIONAL state, this will be incremented. The content will be written to HCCA after HC has incremented the Frame Number at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the Start of Frame in HcInterruptStatus.
Rsvd	31:16	0h		Reserved

HcPeriodicStart

The HcPeriodicStart register has a 14-bit programmable value which determines when is the earliest time HC should start processing the periodic list.

Key	Bit	Reset	HCD/HC	Description
PS	13:0	0h	RW/ R	PeriodicStart After hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.
Rsvd	31:14	0h		Reserved

HcLSThreshold

The HcLSThreshold register contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF.

Key	Bit	Reset	HCD/HC	Description
LST	11:0	0628h	RW/ R	LSThreshold This field contains a value which is compared to the Frame Remaining field prior to initiating a Low Speed transaction. The transaction is started only if Frame Remaining this field.
Rsvd	31:12	0h		Reserved

All registers included in this partition are dedicated to the USB Root Hub which is an integral part of the Host Controller though still a functionally separate entity. The HCD emulates USBD accesses to the Root Hub via a register interface. The HCD maintains many USB-defined hub features which are not required to be supported in hardware.

HcRhDescriptorA

The HcRhDescriptorA register is the first register of two describing the characteristics of the Root Hub. Reset values are implementation-specific. The descriptor length (11), descriptor type (TBD), and hub controller current (0) fields of the hub Class Descriptor are emulated by the HCD.

Key	Bit	Reset	HCD/HC	Description
NDP	7:0	IS	R/ R	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15.
PSM	8	IS	RW/R	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0: All ports are powered at the same time. 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
NPS	9	IS	RW/R	NoPowerSwitching These bits are used to specify whether power switching is supported or ports are always powered. It is implementation specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0: Ports are power switched 1: Ports are always powered on when the HC is powered on
DT	10	0	R/R	DeviceType This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.

Key	Bit	Reset	HCD/HC	Description
OCPM	11	IS	RW/R	OverCurrentProtectionMode This bit describes how the overcurrent statuses for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0: Over-current status is reported collectively for all downstream ports 1: Over-current status is reported on a per-port basis
NOCP	12	IS	RW/R	NoOverCurrentProtection This bit describes how the overcurrent statuses for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0: Over-current status is reported collectively for all downstream ports 1: No overcurrent protection supported
Rsvd	23:13	0		Reserved
POTPGT	31:24	IS	RW/R	PowerOnToPowerGoodTime This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT*2 ms.

HcRhDescriptorB

The HcRhDescriptorB register is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to correspond with the system implementation. Reset values are implementation-specific.

Key	Bit	Reset	HCD/HC	Description
DR	15:0	IS	RW/ R	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit 15: Device attached to Port #15

Key	Bit	Reset	HCD/HC	Description
PPCM	31:16	IS	RW/ R	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit 15: Ganged-power mask on Port #15

HcRhStatus

The HcRhStatus register is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the Hub Status Change field.

Key	Bit	Reset	HCD/HC	Description
LPS	0	0	RW/ R	(read) LocalPowerStatus The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (write) ClearGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect .
OCI	1	0	R/ RW	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
Rsvd	14:2	0		Reserved

Key	Bit	Reset	HCD/HC	Description
DRWE	15	0	RW/R	(read) DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the Resume Detected interrupt. 0 = ConnectStatusChange is not a remote wakeup event. 1 = ConnectStatusChange is a remote wakeup event. (write) SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
LPSC	16	0	RW/R	(read) LocalPowerStatusChange The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (write) SetGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
OCIC	17	0	RW/RW	OverCurrentIndicatorChange This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a '1'. Writing a '0' has no effect.
Rsvd	30:18	0		Reserved
CRWE	31		W/R	(write) ClearRemoteWakeupEnable Writing a '1' clears DeviceRemoveWakeupEnable. Writing a '0' has no effect.

HcRhPortStatus1

The HcRhPortStatus1 register is used to control and report port events on a per-port basis. NumberDownstreamPorts represents the number of HcRhPortStatus registers that are implemented in hardware. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits.

Key	Bit	Reset	HCD/HC	Description
CCS	0	0	RW/RW	(read) CurrentConnectStatus This bit reflects the current state of the downstream port. 0 = no device connected 1 = device connected (write) ClearPortEnable The HCD writes a '1' to this bit to clear the PortEnableStatus bit. Writing a '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read '1b' when the attached device is nonremovable (DeviceRemoveable[NDP]).
PES	1	0	RW/RW	(read) PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 = port is disabled 1 = port is enabled (write) SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.

Key	Bit	Reset	HCD/HC	Description
PSS	2	0	RW/RW	(read) PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0 = port is not suspended 1 = port is suspended (write) SetPortSuspend The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.
POCI	3	0	RW/RW	(read) PortOverCurrentIndicator This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0 = no overcurrent condition. 1 = overcurrent condition detected. (write) ClearSuspendStatus The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.

Key	Bit	Reset	HCD/HC	Description
PRS	4	0	RW/RW	(read) PortResetStatus When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 = port reset signal is not active 1 = port reset signal is active (write) SetPortReset The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.
Rsvd	7:5	0		Reserved

Key	Bit	Reset	HCD/HC	Description
PPS	8	0	RW/RW	(read) PortPowerStatus This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NDP]. In global switching mode (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0 = port power is off 1 = port power is on (write) SetPortPower The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. Note: This bit is always reads '1b' if power switching is not supported.
LSDA	9	x		(read) LowSpeedDeviceAttached This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 = full speed device attached 1 = low speed device attached (write) ClearPortPower The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.
Rsvd	15:10	0		Reserved

Key	Bit	Reset	HCD/HC	Description
CSC	16	0	RW/RW	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 = no change in CurrentConnectStatus 1 = change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
PESC	17	0	RW/RW	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 = no change in PortEnableStatus 1 = change in PortEnableStatus
PSSC	18	0	RW/RW	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resynchronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 = resume is not completed 1 = resume completed
OCIC	19	0	RW/RW	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 = no change in PortOverCurrentIndicator 1 = PortOverCurrentIndicator has changed

Key	Bit	Reset	HCD/HC	Description
PRSC	20	0	RW/RW	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 = port reset is not complete 1 = port reset is complete
Rsvd	31:21	0		Reserved

6.4 EHCI Register Set

Configuration Registers

Offset	Register Name	Default	Access
09-0Bh	USBClassCode	24'h0C_0320	RO
10-13h	BAR	32'h400F_C000	RO
60h	SerialBusReleaseNumber	8'h20	RO
61h	FrameLengthAdjust	8'h20	RW
62-63h	PortWakeCapability	16'h0003	RW

Capability Registers

The Capability registers address is calculated by adding the **BAR0** base address of the enhanced host controller function to the offset mentioned below.

BAR0 (of EHCI function) + <Offset>

Offset	Register Name	Default	Access
00h	CAPLENGTH	8’h20	RO
01h	Reserved		
02h	HCIVERSION	16’h0100	RO
04-07h	*HCSPARAMS	32’h0000_1191	RO
08-0Bh	*HCCPARAMS	32’h0000_0016	RO
0C-13h	*HCSPPORTROUTE	***	RO

* Note: 1. Bit 7 in the HC Structural parameters is I2C programmable.
2. Host Controller Port Route is also I2C programmable.

*** Depending on the EHCI function, the default value for HCSPPORTROUTE changes as described below

Function	Value
Function 1	60’h0
Function 3	60’h1
Function 5	60’h2
Function 7	60’h3

Operational Registers

The Operational Registers base address is calculated by adding the value in the Capability Registers Length (i.e. 20h) to the **BAR0** base address of the enhanced host controller function and to the offset mentioned below.

BAR0 (of EHCI function) + <Capability Registers Length = 20h> + <Offset>

Offset	Register Name	Default	Access
00-03h	USBCMD	32'h0008_0B00	RW
04-07h	USBSTS	32'h0000_1000	RO/RW/RWC
08-0Bh	USBINTR	32'h0000_0000	RW
0C-10h	FRINDEX	32'h0000_0007	RW
14-17h	PERIODICLISTBASE	32'h0000_0000	RW
18-1Bh	ASYNCLISTADDR	32'h0000_0000	RW
40-43h	CONFIGFLAG	32'h0000_0000	RW
44-47h	PORTSC	32'h0000_2000	RW

6.4.1 Description of EHCI Capability and Operational Registers

USBClassCode

Bit	Name	Access	Default	Description
23:16	Base Class Code	RO	0Ch	Serial Bus Controller
15:8	Sub Class Code	RO	03h	Universal Serial Bus Host Controller
7:0	Programming Interface	RO	20h	USB2.0 Host controller that conforms to this specification.

BAR

Bit	Name	Access	Default	Description
31:8	Base Address	RO	400F_C0h	Corresponds to memory address signals
7:3	Rsvd			Reserved
2:1	Type	RO	00b	00b—May only be mapped into 32-bit addressing space. 01b—May be mapped into 64-bit addressing space.
0	Rsvd			Reserved

SerialBusReleaseNumber

Bit	Name	Access	Default	Description
7:0	Serial Bus Specification Release Number	RO	20h	Release of the USB Specification with which this USB Host Controller module is compliant.

FrameLengthAdjust

Bit	Name	Access	Default	Description
7:6	Rsvd			Reserved
5:0	Frame Length Timing Value	RW	20h	Each decimal value change to this register corresponds to 16-high speed bit times.

PortWakeCapability

Bit	Name	Access	Default	Description
15:0	Port Wake up capability mask	RW	16'h0003	Bit position zero of this register indicates whether the register is implemented. A one in bit position zero indicates that the register is implemented. Bit positions 1 through 15 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, position 2 to port 2, etc

CAPLENGTH

Bit	Name	Access	Default	Description
7:0	CapLen	RO	8'h20	This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

HCIVERSION

Bit	Name	Access	Default	Description
15:0	IntfVerNum	RO	16'h0100	This is a two-byte register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

HCSPARAMS

Bit	Name	Access	Default	Description
31:24	Rsvd			Reserved
23:20	DbgPortNum	RO	0h	*Optional.* This register identifies which of the host controller ports is the debug port. The value is the port number (one-based) of the debug port. A nonzero value in this field indicates the presence of a debug port. The value in this register must not be greater than *N_PORTS*
19:17	Rsvd			Reserved
16	PortIndi	RO	0h	This bit indicates whether the ports support port indicator control. When this bit is a one, the port status and control registers include a read/writeable field for controlling the state of the port indicator.
15:12	NumCompCntrl	RO	4'h1	This field indicates the number of companion controllers associated with this USB 2.0 host controller. A zero in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports.
9:8	NumPortCompCntrl	RO	4'h1	This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software.
7	PortRoutRules	RO	1'b1	This field indicates the method used by this implementation for how all ports are mapped to companion controllers. 0 – The first *N_PCC* ports are routed to the lowest numbered function companion host controller, the next *N_PCC* port are routed to the next lowest function companion controller, and so on 1 – The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-Port Route Array.
6 :5	Rsvd			Reserved

Bit	Name	Access	Default	Description
4	PortPwrCntrl	RO	1'b1	This field indicates whether the host controller implementation includes port power control. A one in this bit indicates the ports have port power switches. A zero in this bit indicates the port do not have port power switches.
3:0	Nports	RO	4'h1	This field specifies the number of physical down stream ports implemented on this host controller.

HCCPARAMS

Bit	Name	Access	Default	Description
31:16	Rsvd			Reserved
15:8	EHCIExtCapPtr	RO	0h	This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability
7:4	IsocSchdThr	RO	4'h1	This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame
3	Rsvd			Reserved
2	AsynSchdParkCap	RO	1h	If this bit is set to one, the park mode feature is enabled for High speed queue heads of the asynchronous schedule.

Bit	Name	Access	Default	Description
1	PFLF	RO	1h	If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to a one, then system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	64-bit AddrCap	RO	0h	This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the data structures defined in Section 3 (32-bit) or those defined in Appendix B (64-bit). Values for this field have the following interpretation: 0b-- data structures using 32-bit address memory pointers 1b-- data structures using 64-bit address memory pointers

HCSPPORTROUTE

Register bits for updating bits [3:0] of HCSPPORTROUTE register for each port.

Bit	Name	Access	Default	Description
59:0	PortRouteDescNum	RO	60'hx	This field is a 15-element nibble array (each 4 bits is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE[0] corresponds to the first PORTSC port, PORTROUTE[1] to the second PORTSC port, etc.

USBCMD - USB Command register

Bit	Name	Access	Default	Description
31:24	Rsvd			Reserved
23:16	IntThrCntrl	RW	08h	This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. Value - Maximum Interrupt Interval 00h - Reserved 01h - 1 micro-frame 02h - 2 micro-frames 04h - 4 micro-frames 08h - 8 micro-frames 10h - 16 micro-frames (Default, 1ms) 20h - 32 micro-frames (2ms) 40h - 64 micro-frames (8 ms)
15:12	Rsvd			Reserved
11	AsynSchdParkModeEnable	RW	0b	1 - Park mode enabled. 0 - Park Mode is disabled.
10	Rsvd			Reserved
9:8	AsynSchdParkModeCount	RW	0b	It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. Software must not write a zero to this bit when Park Mode Enable is a one as this will result in undefined behavior.

Bit	Name	Access	Default	Description
7	LightHostCntrlReset	RW	1b	If implemented, it allows the driver to reset the Host controller without affecting the state of the ports or the relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values. A host software read of this bit as one indicates the Light Host Controller Reset has completed and it is safe for host software to re-initialize the host controller. A host software read of this bit as a zero indicates the Light Host Controller Reset has not yet completed.
6	IntrptOnAsyncAdvDoorBell	RW	0b	This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one. Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.

Bit	Name	Access	Default	Description
5	AsyncSchdEnable	RW	0b	0 - Do not process the Asynchronous schedule. 1- Use the ASYNCLISTADDR register to access the Asynchronous schedule.
4	PeriodicSchdEnable	RW	0b	0 - Do not process the Periodic schedule. 1 - Use the PERIODICLISTBASE register to access the Periodic schedule.
3:2	FrameListSize	RW	00b	This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean: 00b - 1024 elements (4096 bytes) Default value 01b - 512 elements (2048 bytes) 10b - 256 elements (1024 bytes) # for resource-constrained environments 11b - Reserved
1	HCRESET	RW	1b	This control bit is used by software to reset the host controller. The effects of this are similar to a Chip Hardware Reset.
0	RunStop	RW	0b	1 – Run 0 – Stop

USBSTS - USB Status Register

Bit	Name	Access	Default	Description
31:16	Rsvd			Reserved

Bit	Name	Access	Default	Description
15	AsyncSchdStatus	RO	0b	The bit reports the current real status of the Asynchronous schedule. Zero: The status of the Asynchronous schedule is disabled. One: The status of the Asynchronous schedule is Enabled. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous schedule is either enabled (1) or disabled (0).
14	PeriodicSchdStatus	RO	0b	The bit reports the current real status of the periodic schedule. Zero: The status of the periodic schedule is disabled. One: The status of the periodic schedule is Enabled. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic schedule is either enabled (1) or disabled (0).
13	Reclamation	RO	0b	Used to detect an empty asynchronous schedule.
12	HCHalted	RO	1b	This bit is a zero whenever Run/Stop bit is one. The host controller set this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0.either by software or by the hardware (e.g. Internal error).
11:6	Rsvd			Reserved
5	IntrptOnAsyncAdv	RW	0	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.

Bit	Name	Access	Default	Description
4	HostSysError	RW	0	The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled Tds.
3	FrameListRollover	RW	0	The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, If the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	PortChangeDetect	RW	0	The Host Controller sets this bit to a one when port has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a one. This bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change).
1	USBERRINT	RW	0	The Host Controller sets this bit to 1 when the completion of a USB transaction results in an error condition. (E.g. Error counters underflow).
0	USBINT	RW	0	The Host controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set.

USBINTR -USB Interrupt Enable Register

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USBSTS to allow the software to poll for events.

Bit	Name	Access	Default	Description
31:6	Rsvd			Reserved
5	IntrptOnAsyncAdvEnable	RW	1'b0	When this bit is one, and the Interrupt on Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the interrupt on Async Advance bit.
4	HostSysErrEnable	RW	1'b0	When this bit is a one, and the Host System Error Status bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	FrameListRolloverEnable	RW	1'b0	When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	PortChangeIntrptEnable.	RW	1'b0	When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged edged by software clearing the Port Change Interrupt bit.

Bit	Name	Access	Default	Description
1	USBErrIntrptEnable	RW	1'b0	When this bit is one, and the USBERRINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	USBIntrptEnable	RW	1'b0	When this bit is alone, and the USBINT bit in the UBSSTS register is one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

FRAME INDEX - Frame Index register

This register is used by the host controller to index into the periodic frame list. The register updates every 125 us (Once each micro-frame). Bits [N:3] are used to select a particular entry in the periodic Frame List during scheduled execution. The number of bits used for the index depends on the size of the frame list as set by system software in the Frame List Size field in the USBCMD register.
This register cannot be written unless the Host controller is in the Halted state. SOF frame number value for the bus SOF token is derived from this register. The value of FRINDEX must be 125 us ahead of the SOF token value.

Bit	Name	Access	Default	Description
31:14	Rsvd		0b	Reserved
13:0	FrameIndex	RW	0000_0000h	The value in this register increment at the end of each time frame (e.g. Micro-frame). Bits [N: 3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values on N based on the value of the Frame List Size in the USBCMD register.

USBCMD	Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

PERODICLISTBASE - Periodic Frame List Base Address Register

This 32-bit register contains the beginning address of the Periodic frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host controller. The Memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.

Bit	Name	Access	Default	Description
31:12	BaseAddr	RW	20'h0	These bits correspond to memory address signals [31:12], respectively.
11:0	Rsvd			Reserved

ASYNCLISTADDR - Current Asynchronous List Address register

This 32-bit register contains the address of the next asynchronous queue head to be executed. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte aligned.

Bit	Name	Access	Default	Description
31:5	LinkPtr	RW	27'h0	These bits correspond to memory address signals [31:5] respectively. This field may only reference Queue Head (QH).
4:0	Rsvd			Reserved

CONFIGGLAG – Configuration Flag Register

Bit	Name	Access	Default	Description
0	ConfigFlag	RW	0b	This bit controls the default port-routing control logic. Host software sets this bit as the last action in its process of configuring the host controller
31:1	Rsvd			Reserved

PORTSC - Port Status and Control register

A host controller must implement one or more port registers. Software uses this information as an input parameter to determine how many ports need to be serviced.

1.1 Initial Conditions of a port
1.2 No device connected
1.3 Port disabled.

If the port has port power control, software cannot change the state of the port until after it applies power to the port by setting port power to 1. The host is required to have power stable to the port within 20milliseconds of the zero to one transition.

Bit	Name	Access	Default	Description
31:23	Rsvd			Reserved
22	WKOCE	RW	0b	Wake on Over-current Enable. Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events.
21	WKDSCNNTE	RW	0b	Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
20	WKCNNTE	RW	0b	Writing this bit to a one enables the port to be sensitive to device connects as wake-up events.
19:16	PortTestControl	RW	0000b	When this field is zero, the port is NOT operating in test mode. 0000b - Test mode not enabled. 0001b - Test J_STATE 0010b - Test K_STATE 0011b - Test SE0_NAK 0100b - Test Packet 0101b - Test FORCE_ENABLE
15:14	PortIndiCntrl		00b	Writing to these bits has no effect if the P_INDICTAOR bit in the HCPARAMS register is a zero.
13	PortOwner	RW	1b	This bit unconditionally goes to a 0b when the configured bit in the CONFIGFLAG register makes a 0b to 1b transition
12	PortPower	RW	1'b0	Host controller has port power control switches. This bit represents the current setting of the switch (0=Off, 1=On). When power is not available on a port (i.e. PP equals a 0), the port is non-functional and will not report attaches, detaches etc.

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Default</th><th>Description</th></tr>
<tr><td>11:10</td><td>LineStatus</td><td>RO</td><td></td><td>These bits reflect the current logical levels of the D+ and D- signal lines.
These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the Bits[11:10] are
<table>
<tr><th>Value</th><th>USB State</th><th>Interpretation</th></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform reset</td></tr>
<tr><td>01b</td><td>J_STATE</td><td>Not Low-speed device, perform reset</td></tr>
<tr><td>10b</td><td>K_STATE</td><td>Not Low-speed device, perform reset</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform reset</td></tr>
</table></td></tr>
<tr><td>9</td><td>Rsvd</td><td></td><td></td><td>Reserved</td></tr>
<tr><td>8</td><td>PortReset</td><td>RW</td><td>1'b0</td><td>1 - Port is in reset
0 - Port is not in reset</td></tr>
<tr><td>7</td><td>Suspend</td><td>RW</td><td>1'b0</td><td>1 - Port is in suspend
0 - Pot not in suspend state</td></tr>
<tr><td>6</td><td>ForcePortResume</td><td>RW</td><td>1'b0</td><td>1 - Resume detected/driven on port
0 - No resume (K_STATE) detected/driven on port</td></tr>
<tr><td>5</td><td>OverCurrentChange</td><td>RWC</td><td>0b</td><td>This bit gets set to a one when there is a change to Over-Current Active. Software clears this bit by writing to a one to this bit position</td></tr>
<tr><td>4</td><td>OverCurrentActive</td><td>RO</td><td>0b</td><td>1 = This port currently has an over current condition
0 = This port does not have an over-current condition.</td></tr>
<tr><td>3</td><td>PortEnableDisableChange</td><td>RWC</td><td>0b</td><td>1 = Port enabled/disabled status has changed.
0 = No change.
For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point.</td></tr>
</table>

Bit	Name	Access	Default	Description
2	PortEnableDisable	RW	0b	Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled (0b) downstream propagation of data is blocked on this port, except for reset. This field is zero if Port Power is zero.
1	ConnectStatusChange	RWC		1 = Change in current Connect status. 0 = No change.
0	CurrentConnectStatus	RO	0b	1 = Device is present on port 0 = No device is present

6.5 OTG Register Set

BAR0 (of OTG function) + <Offset>

Offset	Register Name	Default	Category	Description
00-03h	OTGDevIntEnable	32'h0000_0000	Device	Device interrupt enable Register
04-07h	OTGDevIntStatus	32'h0000_0000	Device	Device interrupt register
08-0Bh	OTGDevStateAdd	32'h0004_1000	Device	Device state Address register
0C-0Fh	CntrlEPReqBaseAdd	32'h0000_0000	Device	Control IN Register
10-13h	CntrlInTDBaseAdd	32'h0000_0000	Device	Control Out Register
14-17h	IntEP1Cntrl	32'h0000_0200	Device	Endpoint 1 Control Register
18-1Bh	IntEP1TDBaseAdd	32'h0000_0000	Device	Endpoint 1 Base Address
1C-1Fh	BulkInEP2Cntrl	32'h0000_0200	Device	Endpoint 2 Control Register
20-23h	BulkInEP2TDBaseAdd	32'h0000_0000	Device	Endpoint 2 Base Address
24-27h	BulkOutEP3Cntrl	32'h0000_0000	Device	Endpoint 3 Control Register
28-2Bh	BulkOutEP3BaseAdd	32'h0000_0000	Device	Endpoint 3 Base Address
2C-2Fh	EPTDCount	32'h0000_0000	Device	End point TD count register
30-33h	OTGControl	32'h0000_00C0	OTG	OTG Controller register
34-37h	OTGIntEnable	32'h0000_0000	OTG	OTG interrupt enable register
38-3Bh	OTGIntStatus	32'h0000_0000	OTG	OTG interrupt status register
3C-3Fh	IDSampling	32'h002D_C46A	OTG	ID Sampling Register
40-43h	OTGBConnectLongDebounce	32'h005B_88D0	OTG	OTG B-connect long debounce Register
44-47h	OTGDataLinePulse Time	32'h0004_C471	OTG	OTG Data line pulse time Register
48-4Bh	OTGChargeVBUS	32'h001B_7740	OTG	OTG charge VBUS register
4C-4Fh	BulkInEP4Cntrl	32'h0000_0000	Device	EP4 Control
50-53h	BulkInEP4BaseAdd	32'h0000_0000	Device	EP4 Base Address
54-57h	BulkOutEP5Cntrl	32'h0000_0000	Device	EP5 Control
58-5Bh	BulkOutEP5BaseAdd	32'h0000_0000	Device	EP5 Base Address
70-73h	BulkInEPMaxPacketSize	32'h0000_0200	Device	Bulk in endpoint max packet size register

Offset	Register Name	Default	Category	Description
74-77h	USBDevEPCntrl	32'h0000_0001	Device	Bulk endpoint control register
78-7Ch	BulkOutEP3SoftTimer	32'h0000_0000	Device	EP3 soft timer register
7C-7Fh	BulkOutEP5SoftTimer	32'h0000_0000	Device	EP5 soft timer register
84-87h	CntrlOutEPTDBaseAdd	32'h0000_0000	Device	Control Out EP transfer descriptor base address register

6.5.1 Description of OTG Device Registers

OTGDevIntEnable

This register will help to enable or disable interrupts on various events. A value of '1' will enable a specific interrupt, while a '0' will disable it.

Bit	Name	Access	Default	Description
31:11	Rsvd	RW	0h	Reserved
10	CntrlOUTEPIntrptEn	RW	1'b0	Setting this bit to '1' enables the Control OUT endpoint (EP) data stage interrupt.
9	BulkOutEP5IntrptEn	RW	1'b0	Setting this bit to '1' enables the Bulk OUT (EP5) interrupt
8	BulkInEP4IntrptEn	RW	1'b0	Setting this bit to '1' enables the Bulk IN (EP4) interrupt
7	HostResetDetect	RW	1'b0	Setting this bit to '1' enables USB protocol reset interrupt.
6	HostResumeDetectIntrptEn	RW	1'b0	Setting this bit to '1' enables USB resume interrupt
5	SuspendDetectIntrptEn	RW	1'b0	Setting this bit to '1' enables USB suspend interrupt.
4	BulkOutEP3IntrptEn	RW	1'b0	Setting this bit to '1' enables the Bulk OUT (EP3) interrupt
3	BulkInEP2IntrptEn	RW	1'b0	Setting this bit to '1' enables the Bulk IN (EP2) interrupt
2	IntrptEP1IntrptEn	RW	1'b0	Setting this bit to '1' enables the Interrupt IN (EP1) interrupt
1	CntrlEPReqPacketIntrptEn	RW	1'b0	When set device controller generates an interrupt, for control endpoint setup stage packet
0	CntrlInEPIntrptEn	RW	1'b0	Setting this bit to '1' enables the Control IN endpoint (EP) data stage interrupt.

OTGDevIntStatus

This register will give status of all the interrupts. The events generating the interrupt are same as listed above. Writing a value of '1' to a specific bit will clear the status to '0'.

Bit	Name	Access	Default	Description
31:11	Rsvd		0h	Reserved
10	CntrlOutEP0DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Control OUT endpoint (EP0) DMA transfer completion from hardware buffer to system memory
9	BulkOutEP5DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Bulk OUT endpoint (EP5) DMA transfer completion from hardware buffer to system memory
8	BulkInEP4DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Bulk IN endpoint (EP4) DMA transfer completion from system memory to hardware buffer
7	USBHostResetDetectIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB protocol Reset signaling from peer USB host
6	USBHostResumeDetectIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Resume signal detection during device suspend
5	USBDevSuspendIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB device is in suspend state.
4	BulkOUTEP3DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Bulk OUT endpoint (EP3) DMA transfer completion from hardware buffer to system memory.
3	BulkInEP2DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Bulk IN endpoint (EP2) DMA transfer completion from system memory to hardware buffer.
2	IntrptInEP1DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Interrupt IN endpoint (EP1) DMA transfer completion from system memory to hardware buffer.

Bit	Name	Access	Default	Description
1	CntrlInEP0DataIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device Control IN endpoint (EP0) DMA data transfer completion from system memory to hardware buffer.
0	CntrlEP0SetupStageIntrpt	RWC	1'b0	Setting this bit to '1' indicates USB Device control endpoint (EP0) setup stage packet DMA transfer completion from hardware buffer to system memory.

OTGDevStateAdd

Bit	Name	Access	Default	Description
31:20	Rsvd			Reserved
19	SetAddr	RW	1'b0	Used to retain the default address during USB set address command. Software sets this bit to '1' after receiving USB set address command from external host. Hardware clears this bit to '0' after sending the zero length packets for USB set address command in status stage. Note: The access of set address as well as device address is to be done simultaneously.
18	DevSpeed	RO	1'b1	1 - Indicates that device operates in Full Speed mode. 0 - indicates that device operates in High Speed mode.
17	ConfigDone	RW	1'b0	Configuration done. It is set by the software when it configured the get descriptors.
16	ClearOutPID	RW	1'b0	Setting this bit to '1' clears Bulk OUT PID check logic. This bit is self cleared.
15:13	Rsvd	R0	3'b000	Reserved
12	DevReset	RW	1'b1	Device reset bit. USB Device Soft Reset Control bit. Writing this bit to '0' resets USB device controller.
11:8	Test	RW	1'b0	Test signal for USB device controller Test[8] = 1, Test J_STATE Test[9] = 1, Test K_STATE Test[10] = 1, Test SE0_NAK Test[11] = 1, Test Packet

Bit	Name	Access	Default	Description
7	Rsvd	RO	1'b0	Reserved
6:0	DevAddr	RW	7'h0	It represents USB Device address. Note: This is to be updated whenever the set address is accessed.

CntrlEPReqBaseAdd

The Control Endpoint functionality is implemented with the help of 2 registers 'Control Data IN' and 'Control Data OUT'. All the Control Requests will be handled in software.

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	System software allocates a chunk of memory large enough to accept an incoming Control request and write the memory base address in this register
1:0	Rsvd	RW	0h	Reserved

CntrlInTDBaseAdd

When a Control Request comes, the hardware will generate an ACK in the Setup stage, copies the request in the memory pointed by Control Data IN register and raise an interrupt to indicate this to the software. The software will decode the request and prepare the data to be sent in the response. The software will store this response data in a memory buffer which is DWORD aligned. Then it will write to the Control Data OUT register with ACK and Done bit set. If there was any error while processing the request, it will reset the ACK bit and set the done bit, which will result in STALL being sent out.

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	System software writes this register with Control IN TD base pointer. It is DWORD aligned address.
1	ACK	RW	0b	This bit gives the response code to be sent in the Data or Status stage. 1 = ACK 0 = STALL
0	Done	RW	0b	This bit is set by the system software when it has completed the control request processing. This bit is self clearing.

IntEP1Cntrl

This register holds some important fields of Endpoint Descriptor as described below:

Bit	Name	Access	Default	Description
31	Enable	RW	0h	Software writes '1' to this bit to enable Interrupt IN endpoint. This endpoint and the related 2 registers are valid only if this bit is set.
30:23	Interval	RW	0h	Interval for polling the endpoint for data transfers. Expressed in frames of microframes depending on the device operating speed.
22:14	Rsvd		0h	Reserved
13	EPStall	RW	0h	When Set to '1' STALL response is sent for Interrupt EP request.
12:10	MaxPacketSize	RW	3'b011 for EP0 and EP1 3'b110 for EP2,3,4, 5	Max packet size indicates that this endpoint is capable of sending or receiving those many number of bytes when this configuration is selected 3'b000 – 8bytes 3'b001 – 16bytes 3'b010 – 32bytes 3'b011 – 64bytes 3'b100 – 128bytes 3'b101 – 256bytes 3'b110 – 512bytes 3'b111 – 1024bytes
9	Direction	RO	1b	1 = IN endpoint
8:5	Number	RW	0h	It represents the endpoint number
4:3	Rsvd	RO	0h	Reserved
2:0	Type	RW	0h	Endpoint Descriptor Type

The endpoint is valid only when the Enable bit (31) is set.

IntEP1TDBaseAdd

The Base Address Register, as the name implies, contains the base address or the pointer to the memory in the system area. The software will allocate the memory required for that endpoint operation and initialize this register with the memory address.

Bit	Name	Access	Default	Description
31:0	BaseAddr	RW	0h	Software writes the Interrupt IN TD base pointer value in this register

BulkInEP2Cntrl

This register holds some important fields of Endpoint Descriptor as described below:
The endpoint is valid only when the Enable bit (31) is set.

Bit	Name	Access	Default	Description
31	Enable	RW	0h	Software writes '1' to this bit to enable Interrupt IN endpoint. This endpoint and the related 2 registers are valid only if this bit is set.
30:23	Interval	RW	0h	Interval for polling the endpoint for data transfers. Expressed in frames of microframes depending on the device operating speed.
22:14	Rsvd		0h	Reserved
13	EPStall	RW	0h	STALL response to be sent for corresponding end point.
12:10	MaxPacketSize	RW	3'b011 for EP0 and EP1 3'b110 for EP2,3,4, 5.	Max packet size indicates that this endpoint is capable of sending or receiving those many number of bytes when this configuration is selected. 3'b000 – 8bytes 3'b001 – 16bytes 3'b010 – 32bytes 3'b011 – 64bytes 3'b100 – 128bytes 3'b101 – 256bytes 3'b110 – 512bytes 3'b111 – 1024bytes
9	Direction	RO	1b	1 = IN endpoint
8:5	Number	RW	0h	It represents the endpoint number
4:3	Rsvd		0h	Reserved
2:0	Type	RW	0h	Endpoint Descriptor Type

BulkInEP2TDBaseAdd

The Base Address Register, as the name implies, contains the base address or the pointer to the memory in the system area. The software will allocate the memory required for that endpoint operation and initialize this register with the memory address.

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	It points to the Bulk IN EP transfer descriptor linked list.
1	Rsvd	RW	0h	Reserved

Bit	Name	Access	Default	Description
0	TDValidBit	RW	0h	Software sets this bit after preparing the data structures for associate Endpoint. When this bit is set, hardware loads the software written base address register into local hardware TD base address register, if local hardware TD base address register contains NULL pointer. Hardware clears this bit after loading the base address register value.

BulkOutEP3Cntrl

This register holds some important fields of Endpoint Descriptor as described below:
The endpoint is valid only when the Enable bit (31) is set.

Bit	Name	Access	Default	Description
31	Enable	RW	0h	This endpoint and the related 2 registers are valid only if this bit is set.
30:23	Interval	RW	0h	Interval for polling the endpoint for data transfers. Expressed in frames of micro frames depending on the device operating speed.
22:14	Rsvd		0h	Reserved
13	EPStall	RW	0h	STALL response is sent for corresponding end point.
12:10	MaxPacketsize	RW	3'b011 for EP0 and EP1 3'b110 for EP2,3,4, 5.	Max packet size indicates that this endpoint is capable of sending or receiving those many number of bytes when this configuration is selected 3'b000 – 8bytes 3'b001 – 16bytes 3'b010 – 32bytes 3'b011 – 64bytes 3'b100 – 128bytes 3'b101 – 256bytes 3'b110 – 512bytes 3'b111 – 1024bytes
9	Direction	RO	0b	0 = OUT endpoint
8:5	Number	RW	0h	It represents the endpoint number
4:3	Rsvd	R	0h	Reserved
2:0	Type	RW	0h	Endpoint Descriptor Type

BulkOutEP3BaseAdd

The Base Address Register, as the name implies, contains the base address or the pointer to the memory in the system area. The software will allocate the memory required for that endpoint operation and initialize this register with the memory address.

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	It points to the Bulk OUT EP transfer descriptor linked list.
1	Rsvd	RW	0h	Unused
0	TDValidBit	RW	0h	Software sets this bit after preparing the data structures for associate Endpoint. When this bit is set, hardware loads the software written base address register into local hardware TD base address register, if local hardware TD base address register contains NULL pointer. Hardware clears this bit after loading the base address register value

EPTDCount

EP0 TD count is for Control end point, which is incremented by software and it is decremented by hardware.
EP1 data available for Interrupt end point, which is updated by software and it is cleared by hardware

Bit	Name	Access	Default	Description
31:29	Rsvd		3'b000	Reserved
8	EP1DataAvailable	RW	1'b0	Interrupt Endpoint EP1 TD data available register
7:5	Rsvd		3'b000	Reserved
4:0	EP0TDCount	RW	5'b00000	Control Endpoint EP0 TD count register.

OTGControl

Note: Hardware Read Only. Software Read/Write

Bit	Name	Access	Default	Device	Description
0	ABusDrop	RW	1'b0	A-device	A-device bus drop. Writing '1' to this bit drops the power to USB bus. This is applicable to OTG A-device

Bit	Name	Access	Default	Device	Description
1	ABusReq	RW	1'b0	A-device	A-device bus request. Writing '1' to this bit enables the USB bus power. This is applicable to OTG A- device .
2	ASetBHNPEn	RW	1'b0	A-device	A-device set BHNPEn. OTG A-device sets this bit at the same time when it sets BHNPEn bit in the B-device.
3	Rsvd	RW	1'b0		Reserved
4	BHNPEn	RW	1'b0	B-device	Setting this feature indicates to the B-device that it has been enabled to perform HNP. An A-device sets this feature if, and only if, the B-device is connected directly to an A-device port that supports HNP.
5	BBusReq	RW	1'b0	B-device	B-device bus request. B-device application sets this bit when it wants to use the bus. It clears when application running on the B-device does not want to use the bus.
6	SRPDetEn	RW	1'b1	A-device	Writing '1' to this bit enables the SRP detection at the OTG A-device. SRP Detection Enable is used by A-Device. This bit will be set and cleared by software.
7	Rsvd				Reserved
8	DevSuspendDisable	RW	1'b0	A-device	Software running on A-device clears this bit when it does not want to enable suspend detection logic. Writing '1' to this bit enables suspend detection logic
31:9	Rsvd	-	'b0	-	Reserved

OTGIntEnable

Bit	Name	Access	Default	Description
31:18	Rsvd			Reserved
17	IDPinVldIntrptEn	RW	1'b0	Setting this bit to '1' enables ID pin valid interrupt.
16	AConnIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device connect interrupt.
15	BConnIntrptEn	RW	1'b0	Setting this bit to '1' enables B-device connect interrupt.
14	SessionReqDoneIntrptEn	RW	1'b0	Setting this bit to '1' enables Session request done interrupt
13	AVbusErrIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device Vbus error interrupt
12	DevNoResponseIntrptEn	RW	1'b0	Setting this bit to '1' enables Device no response interrupt
11	PeripheralOnIntrptEn	RW	1'b0	Setting this bit to '1' enables Peripheral on interrupt
10	HostOnIntrptEn	RW	1'b0	Setting this bit to '1' enables Host on interrupt
9	ASessVldIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device session valid interrupt.
8	BSessVldIntrptEn	RW	1'b0	Setting this bit to '1' enables B-device session valid interrupt.
7	AVbusVldIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device VBUS valid interrupt.
6	IDIntrptEn	RW	1'b0	Setting this bit to '1' enables Identification bit interrupt.
5	ABusResumeIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device bus resume interrupt.
4	BBusResumeIntrptEn	RW	1'b0	Setting this bit to '1' enables B-device bus resume interrupt.
3	ABusSuspendIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device bus suspend interrupt.
2	BBusSuspendIntrptEn	RW	1'b0	Setting this bit to '1' enables B-device suspend interrupt enable.
1	BSessEndIntrptEn	RW	1'b0	This bit is asserted when there is a change in B-device session end bit in OTG status register. Setting this bit to '1' enables B-device session end interrupt.
0	ASRPDetIntrptEn	RW	1'b0	Setting this bit to '1' enables A-device SRP detect interrupt.

OTGIntStatus

Bit	Name	Access	Default	Description
31	IDPinVld	RO	1'b0	'1' indicates OTG Identification pin valid signaling
30	IDDig	RO	1'b1	This bit reflects the logical level of the ID pin.
29	HostOn	RO	1'b0	'1' indicates OTG device is operating in host mode
28	PeripheralOn	RO	1'b0	'1' indicates OTG device is operating in peripheral mode.
27:18	Rsvd			Reserved
17	IDPinVldP	RWC	1'b0	'1' indicates ID pin has changed from logical state '0' to '1'
16	AConnP	RWC	1'b0	'1' indicates A-device connect signaling
15	BConnP	RWC	1'b0	'1' indicates B-device connect signaling
14	SessionRequestDoneP	RWC	1'b0	'1' indicates B-device SRP session request completion signaling
13	AVbusErrP	RWC	1'b0	'1' indicates A-device VBUS error signaling
12	DevNoResponseP	RWC	1'b0	'1' indicates device no response signaling
11	PeripheralOnPn	RWC	1'b0	'1' indicates peripheral mode change signaling
10	HostOnPn	RWC	1'b0	'1' indicates host mode change signaling.
9	ASessVldP	RWC	1'b0	'1' indicates A-device session is valid.
8	BSessVldP	RWC	1'b0	'1' indicates B-device session is valid.
7	AVbusVldP	RWC	1'b0	'1' indicates A-device VBUS valid signaling.
6	IDDigPn	RWC	1'b0	Hardware asserts this bit to '1' when it detects a change in identification pin logical value
5	ABusResume	RWC	1'b0	'1' indicates A-device has detected USB resume signaling
4	BBusResume	RWC	1'b0	'1' indicates B-device has detected USB resume signaling

Bit	Name	Access	Default	Description
3	ABusSuspend	RWC	1'b0	'1' indicates A-device has detected USB suspend signaling
2	BBusSuspend	RWC	1'b0	'1' indicates B-device has detected USB suspend signaling.
1	BSessEndP	RWC	1'b0	'1' indicates B-device session end signaling on positive edge change.
0	ASRPDetP	RWC	1'b0	'1' indicates A-device has detected SRP request from the B-device on positive edge.

BulkInEP4Cntrl

This register holds some important fields of Endpoint Descriptor as described below:

Bit	Name	Access	Default	Description
31	Enable	RW	0h	Software writes '1' to this bit to enable Interrupt IN endpoint. This endpoint and the related 2 registers are valid only if this bit is set.
30:23	Interval	RW	0h	Interval for polling the endpoint for data transfers. Expressed in frames of micro frames depending on the device operating speed.
22:14	Rsvd		0h	Reserved
13	EPStall	RW	0h	STALL Request response to be sent for corresponding end point.
12:10	MaxPacketSize	RW	3'b011 for EP0 and EP1 3'b110 for EP2, 3, 4, 5.	Max packet size indicates that this endpoint is capable of sending or receiving those many number of bytes when this configuration is selected 3'b000 – 8bytes 3'b001 – 16bytes 3'b010 – 32bytes 3'b011 – 64bytes 3'b100 – 128bytes 3'b101 – 256bytes 3'b110 – 512bytes 3'b111 – 1024bytes
9	Direction	RO	1b	1 = IN endpoint
8:5	Number	RW	0h	It represents the endpoint number
4:3	Rsvd	R	0h	Reserved
2:0	Type	RW	0h	Endpoint Descriptor Type

The endpoint is valid only when the Enable bit (31) is set.

BulkInEP4BaseAdd

The Base Address Register, as the name implies, contains the base address or the pointer to the memory in the system area. The software will allocate the memory required for that endpoint operation and initialize this register with the memory address.

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	It points to the Bulk IN EP transfer descriptor linked list.
1	Reserved	RW	0h	Reserved
0	TDValidBit	RW	0h	Software sets this bit after preparing the data structures for associate Endpoint. When this bit is set, hardware loads the software written base address register into local hardware TD base address register, if local hardware TD base address register contains NULL pointer. Hardware clears this bit after loading the base address register value.

BulkOutEP5Cntrl

This register holds some important fields of Endpoint Descriptor as described below:

Bit	Name	Access	Default	Description
31	Enable	RW	0h	This endpoint and the related 2 registers are valid only if this bit is set.
30:23	Interval	RW	0h	Interval for polling the endpoint for data transfers. Expressed in frames of microframes depending on the device operating speed.
22:14	Rsvd		0h	Reserved
13	EPStall	RW	0h	STALL Request response is sent for corresponding end point.

Bit	Name	Access	Default	Description
12:10	MaxPacketSize	RW	3'b011 for EP0 and EP1 3'b110 for EP2, 3, 4, 5.	Max packet size indicates that this endpoint is capable of sending or receiving those many number of bytes when this configuration is selected 3'b000 -- 8bytes 3'b001 – 16bytes 3'b010 – 32bytes 3'b011 – 64bytes 3'b100 – 128bytes 3'b101 – 256bytes 3'b110 -- 512bytes 3'b111 – 1024bytes
9	Direction	RO	0b	0 = OUT endpoint
8:5	Number	RW	0h	It represents the endpoint number
4:3	Rsvd	R	0h	Reserved
2:0	Type	RW	0h	Endpoint Descriptor Type

The endpoint is valid only when the Enable bit (31) is set.

BulkOutEP5BaseAdd

The Base Address Register, as the name implies, contains the base address or the pointer to the memory in the system area. The software will allocate the memory required for that endpoint operation and initialize this register with the memory address.

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	It points to the Bulk OUT EP transfer descriptor linked list.
1	Rsvd	RW	0h	Reserved
0	TDValidBit	RW	0h	Software sets this bit after preparing the data structures for associate Endpoint. When this bit is set, hardware loads the software written base address register into local hardware TD base address register, if local hardware TD base address register contains NULL pointer. Hardware clears this bit after loading the base address register value.

BulkInEPMaxPacketSize

Bit	Name	Access	Default	Description
9:0	BulkInEPMaxPacketSize	RW	200h	Software writes this register with supported Bulk In max packet size value
31:10	Rsvd			Reserved

USBDevEPCntrl

Bit	Name	Access	Default	Description
0	CntrlOutEPEnable	RW	1h	Writing '1' to this bit enables Control OUT endpoint logic
1	BulkOutEP3TimeOutIntrptEnable	RW	0h	Writing '1' this bit enable Bulk out endpoint3 time out interrupt logic
2	BulkOutEP5TimeOutIntrptEnable	RW	0h	Writing '1' this bit enable Bulk out endpoint5 time out interrupt logic
3	Rsvd			Reserved
4	BulkInEP2DataToggleEnable	RW	0h	Writing '1' to this bit enables the hardware to load the data toggle bit from the Bulk IN EP2 data structure
5	BulkInEP4DataToggleEnable	RW	0h	Writing '1' to this bit enables the hardware to load the data toggle bit from the Bulk IN EP4 data structure.

BulkOutEP3SoftTimer

Bit	Name	Access	Default	Description
31:0	BulkEP3SoftTimer	RW	0h	Software loads this register with a 32-bit value. USB deice waits for the reception of bulk out packet, until this timer expires. It generates a bulk time out interrupt to the system if it does not receive a packet during this time.

BulkOutEP5SoftTimer

Bit	Name	Access	Default	Description
31:0	BulkEP5SoftTimer	RW	0h	Software loads this register with a 32-bit value. USB device waits for the reception of bulk out packet, until this timer expires. It generates a bulk time out interrupt to the system if it does not receive a packet during this time.

CntrlOutEPTDBaseAdd

Bit	Name	Access	Default	Description
31:2	AddrPtr	RW	30'h0	System software will allocate a chunk of memory large enough to accept an incoming Control Out EP data and write the address in this register.
1:0	Rsvd	RW	0h	Reserved

6.6 GPIO Register Set

If EEPROM is present and signature ID matches then the DIR register gets updated with the EEPROM contents present in the location from 143-145h, similarly PIN register gets updated with EEPROM contents present in the location from 146-148h.

Address for accessing the GPIO registers in **2USB+OTG+GPIO** is **BAR0 + 16'h0800 + Offset** as mentioned. These registers cannot be accessed in any other mode.

Offset	Name	Type	Default	Functional Description
140h	PIN	RW	N/A	When DIR bits are ones, gives Pin [7:0] bit values and when DIR bits are zeros, writing this register sets the pin out values.
144h	DIR	RW	24'hFF_FFFF	Default all pins are in input mode.
148h	EventMode	RW	24'h00_0000	1: To detect '0' to '1' transition on the PINS. 0: To detect '1' to '0' transition on the PINS. (DIR bits should be set to input mode).
14Ch	OpenDrain	RW	24'h00_000	Controls open drain connectivity of GPIO pads. 1: Enable Open Drain 0: Disable Open Drain
150h	PullUp	RW	24'h00_0000	Controls pull up connectivity to GPIO pads. 1: Enable Pull Up 0: Disable Pull Up
154h	EventDetect	RW	24'h00_0000	Event detect status on the GPIO lines. Set when there is event on GPIO line of which corresponding EVENT EN bit is set and DIR bits should be set to input mode. 1: Event Occurred 0: No event Once event occurs, write on the same bit to clear the interrupt.

Offset	Name	Type	Default	Functional Description
158h	EventEN	RW	24'h00_0000	Enable the event detection on GPIO line. 1: Enable event detection 0: Disable event detection
160h	PINPS	RW	N/A	When PIN SELECT bit is high, when DIR bit is one, gives Pin bit value for the selected pin and when DIR bits is zero, writing to the LSB of this register sets the pin out value for the selected pin.
164h	DIRPS	RW	24'h00_0000	When PIN SELECT bit is high, writing at the LSB of register, sets the direction for the selected pin.
168h	EventModePS	RW	24'h00_0000	When PIN SELECT bit is high, 1 : To detect '0' to '1' transition on the PINS. 0 : To detect '1' to '0' transition on the PINS. (DIR bit should be set to input mode).
16Ch	OpenDrainPS	RW	24'h00_000	When PIN SELECT bit is high, controls open drain connectivity of selected GPIO pad. 1: Enable Open Drain 0: Disable Open Drain
170h	PullUpPS	RW	24'h00_0000	When PIN SELECT bit is high, controls pull up connectivity to selected GPIO pad. 1: Enable Pull Up 0: Disable Pull Up

Offset	Name	Type	Default	Functional Description
174h	EventDetectPS	RW	24'h00_0000	When PIN SELECT bit is high, gives event detect status on the selected GPIO line. Set when there is event on GPIO line of which corresponding EVENT EN bit is set and DIR bits should be set to input mode. 1: Event Occurred 0: No event Once event occurs, write on the same bit to clear the interrupt.
178h	EventENPS	RW	24'h00_0000	When PIN SELECT bit is high, enable the event detection on GPIO line. 1: Enable event detection 0: Disable event detection
17Ch	PINSelect	RW	24'h00_0000	When any bit is set then particular pin is only selected for any operation.
180h	EventDetectCntrl	RW	24'hFF_FFFF	To enable the event detection (both positive & negative edge) on the particular GPIO line.

6.7 ISA Register Set

Offset	Name	Type	Default	Description
104h	ISABridgeReg	RW		ISACountReg : 8-bit register which stores read-write counter information ISABrdgReg : 8-bit register which stores mode selection information

6.7.1 Description of ISA Bridge Registers

ISABridgeReg

Bit	Name	Default	Description
0	ISARstSel = ISABrdgReg[0]	1'b1	High in case of Active High Reset for the device to be connected (Default case). Low in case of Active Low reset for the device to be connected.
1	ISAModeSel = ISABrdgReg[1]	1'b1	Mode Selection bit. High in case of Intel mode (Default case). Low in case of Motorola mode.
2	ISAAddPPSel = ISABrdgReg[2]	1'b0	Used to generate an extra address line used if parallel port is configured & need extra address line to configure ECP mode.
3	ISAUARTSel = ISABrdgReg[3]	1'b0	Work in Motorola mode. High in case of single UARTs are connected through ISA interface.
4	ISADualUARTSel = ISABrdgReg[4]	1'b0	Work in Motorola mode. High in case of DUAL UARTs are connected through ISA interface.
5	ISAQuadUARTSel = ISABrdgReg[5]	1'b0	Work in Motorola mode. High in case of QUAD UARTs are connected through ISA interface.
6	ISAPP1Prsnt = ISABrdgReg[6]	1'b0	Parallel port is present on Port-A of ISA Interface
7	ISAPP2Prsnt = ISABrdgReg[7]	1'b0	Parallel port is present on Port-C of ISA Interface
11:8	ISARdCount = ISACountReg[3:0]	4'd4	Read counter to made flexibility in changing the width of read signal.
15:12	ISAWrCount = ISACountReg[7:4]	4'd4	Write counter to made flexibility in changing the width of write signal.
31:16	Rsvd	16'd0	Reserved

6.8 EEPROM Access Register Set

Address for accessing the register is BAR0 + 16'h0800 + Offset as mentioned below in all the modes, except for **2USB+OTG+ISA** opmode where address will be BAR4 + 16'h0800 + Offset.

Offset	Name	Type	Default	Description
100h	I2C	RW		Contains information read or write access to EEPROM.

6.8.1 Description of I2C Registers

I2C

Bit	Name	Default	Description
7:0	I2CData	8'h00	During the write operation write data has to be placed and during read operation read data is placed.
23:8	I2CAdrs	16'h00	I2C address needs to be sent on I2C lines to access EEPROM.
24	I2C8-16BitAdrs	1'b1	8 -16 bit addressing of EEPROM. 1'b1 – 16 bit addressing. 1'b0 – 8 bit addressing.
30:25	I2CDeviceAdrs	6'h28	EERPROM device address.
31	I2CWRN/ I2CError	1'b0	I2C read or write operation. 1'b0 – Read Operation 1'b1 – Write Operation. This bit is read as one when there is no EEPROM indicating eeprom error.

6.9 Miscellaneous Register Set

Offset	Register Name	Type	Default	Description
D0h	LinkCapRevID	RW		Contains information about Link capabilities and the Revision ID.
D4h	ConfigSpaceUpdate	R		Used to enable programmability of configuration space registers
108h	PwrMgtCntrl	R		disable_usb_phy: 4-bit register used to disable USB PHYs.. pm_reg : 6-bit register used for PCIe power management control feature.
10Ch	ConfigSpaceBaseAdrs	R		Used to select the base address for accessing the configuration space and peripheral control registers.
110h	TrafficClass	R		Used to define traffic class for the functions.
114h	KGbl1	R		Global register used to configure internal device parameters
118h	KGbl2	R		Global register used to configure internal device parameters
11Ch	PCIeTest	R		PCIe test bytes
120h	BridgeCntrl	R		PCIe bridge control signals
124h	EepromMaxReadreqSZ	RW		Setting maximum read request size
128h	PwrMgtAdvErrSupport	R		To provide clock power management & advance error report capability.
NA	WakeCount	NA		Count for asserting the WAKE_N signal to wake the system.
12Ch	KPtr01	R		KPTR0 register used to configure internal device parameters
130h	KPtr02	R		KPTR0 register used to configure internal device parameters
134h	ReplayAckTimer	R		To provide programmability for Replay timer & ACK latency timer.
204h	INTAMask	RW		Programmability for INTA mask reg
204h	INTBMask	RW		Programmability for INTB mask reg
208h	INTCMask	RW		Programmability for INTC mask reg
208h	INTDMask	RW		Programmability for INTD mask reg

6.9.1 Description of Misc Registers

LinkCapRevID

Bit	Name	Default	Description
31:24	Rsvd	8'd0	Reserved
23:16	Rsvd	8'd0	Reserved
15:13	LinkCap	3'b111	L1 Exit Latency for separated clock = [17:15] bit field of Link Capability Register for every function if common clock is not present.
12:10		3'b111	L1 Exit Latency for common clock = [17:15] bit field of Link Capability Register for every function if common clock is present.
9		1'b1	L1 ASPM support = [11] bit field of Link Capability Register for every function.
8		1'b1	L0 ASPM support = [10] bit field of Link Capability Register for every function.
7:0	RevID	8'd0	Revision ID field for every function.

ConfigSpaceUpdate

Bit	Name	Default	Description
0	ConfigSpaceUpdate	1'b0	To enable programmability of PCI express configuration space registers, write 1'b1 over here.
31:1	Rsvd	31'h00	Reserved

PwrMgtCntrl

Bit	Name	Default	Description
0	EnableWake	1'b1	1'b1: Supports remote wake-up through wake-up mechanism. 1'b0 : Does not support
1	Rsvd	1'b0	
2	DisableUSBCH0	1'b0	1'b1 : Disable USB CH0 1'b0 : Normal operation.
3	DisableUSBCH1	1'b0	1'b1 : Disable USB CH1 1'b0 : Normal operation.
4	DisableUSBCH2	1'b0	1'b1 : Disable USB CH2 1'b0 : Normal operation.
5	DisableUSBCH3	1'b0	1'b1 : Disable USB CH3 1'b0 : Normal operation.
7:6	Rsvd	2'b00	Reserved
8	DisableUSBPhyCH0	1'b1	1'b0 : Disable USB PHY CH0 1'b1: Normal operation.

Bit	Name	Default	Description
9	DisableUSBPhyCH1	1'b1	1'b0 : Disable USB PHY CH1 1'b1: Normal operation.
10	DisableUSBPhyCH2	1'b1	1'b0 : Disable USB PHY CH2 1'b1 : Normal operation.
11	DisableUSBPhyCH3	1'b1	1'b0 : Disable USB PHY CH3 1'b1 : Normal operation.
12	OTGTxResume	1'b0	OTG Transmission resume bit
31:13	Rsvd	20'h0	Reserved

ConfigSpaceBaseAdrs

Bit	Name	Default	Description
1:0	ConfigSpaceBaseAdrs	2'b10	To select the base address for accessing the configuration space and peripheral control registers. 2'b00 : Base address is 1K. 2'b01 : Base address is 1K. 2'b10 : Base address is 2K. 2'b11 : Base address is 3K.
2	TestBusSel1-3-0-2	1'b0	Testbus set selection line 1'b0 : Testbus set for Port-0 & Port-2 will be selected 1'b1 : Testbus set for Port-1 & Port-3 will be selected
31:3	Rsvd	30'h00	Reserved

TrafficClass

Bit	Name	Default	Description
2:0	F0TC	3'b000	To select Traffic class for Function-0
5:3	F1TC	3'b000	To select Traffic class for Function-1
7:6	Rsvd	2'b00	Reserved
10:8	F2TC	3'b000	To select Traffic class for Function-2
13:11	F3TC	3'b000	To select Traffic class for Function-3
15:14	Rsvd	2'b00	Reserved
18:16	F4TC	3'b000	To select Traffic class for Function-4
21:19	F5TC	3'b000	To select Traffic class for Function-5
23:22	Rsvd	2'b00	Reserved
26:24	F6TC	3'b000	To select Traffic class for Function-6
29:27	F7TC	3'b000	To select Traffic class for Function-7
31:30	Rsvd	2'b00	Reserved

KGbl1

Bit	Name	Default	Description
31:0	KGbl1	32'h11FF_0001	PCIe global register (KGbl[31:0])

KGbl2

Bit	Name	Default	Description
31:0	KGbl2	32'h0000_0000	PCIe global register (KGbl[63:32])

PCIeTest

Bit	Name	Default	Description
31:0	PCIeTest	32'h0000_0008	PCIe test register

BridgeCntrl

Bit	Name	Default	Description
4:0	BrdgConn	5'h01	PCIe arbiter connect signal
7:5	Rsvd	3'b000	Reserved
12:8	BrdgT2nT1	5'h00	Selection line to connect either to tier1 or tier2
15:13	Rsvd	3'b000	Reserved
31:16	Rsvd	16'h00	Reserved

EepromMaxReadreqSZ

Bit	Name	Default	Description
2:0	EepromMaxReadReqSZ	3'b000	To select max read request size (in Dword) 3'b000 : 128 DW(i.e. 512 byte data) 3'b001 : 32 DW 3'b010 : 64 DW 3'b011 : 128 DW 3'b100 : 256 DW 3'b101 : 512 DW 3'b110 : 1024 DW
31:3	Rsvd	29'd0	Reserved

PwrMgtAdvErrSupport

Bit	Name	Default	Description
0	F0AdvErrRep	1'b1	Advance error report capability feature for Function-0
1	F0ClkPwrMgmtSprt	1'b1	Clock power management support for Function-0
2	F1AdvErrRep	1'b1	Advance error report capability feature for Function-1
3	F1ClkPwrMgmtSprt	1'b1	Clock power management support for Function-1
4	F2AdvErrRep	1'b1	Advance error report capability feature for Function-2

Bit	Name	Default	Description
5	F2ClkPwrMgmtSprt	1'b1	Clock power management support for Function-2
6	F3AdvErrRep	1'b1	Advance error report capability feature for Function-3
7	F3ClkPwrMgmtSprt	1'b1	Clock power management support for Function-3
8	F4AdvErrRep	1'b1	Advance error report capability feature for Function-4
9	F4ClkPwrMgmtSprt	1'b1	Clock power management support for Function-4
10	F5AdvErrRep	1'b1	Advance error report capability feature for Function-5
11	F5ClkPwrMgmtSprt	1'b1	Clock power management support for Function-5
12	F6AdvErrRep	1'b1	Advance error report capability feature for Function-6
13	F6ClkPwrMgmtSprt	1'b1	Clock power management support for Function-6
14	F7AdvErrRep	1'b1	Advance error report capability feature for Function-7
15	F7ClkPwrMgmtSprt	1'b1	Clock power management support for Function-7
31:16	Rsvd	16'd0	Reserved

KPtr01

Bit	Name	Default	Description
31:0	KPtr01	32'hFF83_BE00	PCIe KPTR0 register (KPTR0[31:0])

KPtr02

Bit	Name	Default	Description
3:0	KPtr02	4'hF	PCIe KPTR0 register (KPTR0[35:32])
31:4	Rsvd	28'd0	Reserved

ReplayAckTimer

Bit	Name	Default	Description
14:0	AckLatencyTimer	15'h0000	Ack latency timer
15	Rsvd	1'b0	Reserved
30:16	ReplayTimer	15'h0000	Replay timer
31	Rsvd	1'b0	Reserved

INTAMask

Programmable register used to select the interrupts that can be mapped to PCIe INTA pin.

Bit	Name	Default	Description
0	CH0USBOHCIIntrpt	1'b1	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
1	CH0USBEHCIIntrpt	1'b1	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
2	CH1USBOHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
3	CH1USBEHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
4	CH2USBOHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
5	CH2USBEHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
6	CH2HostIntrOTG	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
7	CH3USBOHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
8	CH3USBEHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
9	ISAIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
10	GPIOIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt

INTBMask

Programmable register used to select the interrupts that can be mapped to PCIe INTB pin.

Bit	Name	Default	Description
0	CH0USBOHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
1	CH0USBEHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
2	CH1USBOHCIIntrpt	1'b1	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
3	CH1USBEHCIIntrpt	1'b1	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
4	CH2USBOHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
5	CH2USBEHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
6	CH2HostIntrOTG	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
7	CH3USBOHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
8	CH3USBEHCIIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
9	ISAIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
10	GPIOIntrpt	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt

INTCMask

Programmable register used to select the interrupts that can be mapped to PCIe INTC pin.

Bit	Name	Mode	Deafult	Description
0	CH0USBOHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
1	CH0USBEHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
2	CH1USBOHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
3	CH1USBEHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
4	CH2USBOHCIIntrpt	Any functional mode	1'b1	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
5	CH2USBEHCIIntrpt	Any functional mode	1'b1	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
6	CH2HostIntrOTG	4USB	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
		2USB+OTG	1'b1	
		2USB+OTG+ISA	1'b1	
		2USB+OTG+GPIO	1'b1	
7	CH3USBOHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
8	CH3USBEHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt

Bit	Name	Mode	Deafult	Description
9	ISAIntrpt	Any functional modes	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
10	GPIOIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt

INTDMask

Programmable register used to select the interrupts that can be mapped to PCIe INTD pin.

Bit	Name	Mode	Deafult	Description
0	CH0USBOHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
1	CH0USBEHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
2	CH1USBOHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
3	CH1USBEHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
4	CH2USBOHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
5	CH2USBEHCIIntrpt	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
6	CH2HostIntrOTG	Any functional mode	1'b0	Programmable bit for masking the interrupt. 1'b0: Mask interrupt 1'b1: Unmask interrupt
7		4USB	1'b1	Programmable bit for masking

Bit	Name	Mode	Deafult	Description
	CH3USBOHCIIntrpt	2USB+OTG	1'b0	the interrupt.
		2USB+OTG+ISA	1'b0	1'b0: Mask interrupt
		2USB+OTG+GPIO	1'b0	1'b1: Unmask interrupt
8	CH3USBEHCIIntrpt	4USB	1'b1	Programmable bit for masking the interrupt.
		2USB+OTG	1'b0	
		2USB+OTG+ISA	1'b0	1'b0: Mask interrupt
		2USB+OTG+GPIO	1'b0	1'b1: Unmask interrupt
9	ISAIntrpt	4USB	1'b0	Programmable bit for masking the interrupt.
		2USB+OTG	1'b0	
		2USB+OTG+ISA	1'b1	1'b0: Mask interrupt
		2USB+OTG+GPIO	1'b0	1'b1: Unmask interrupt
10	GPIOIntrpt	4USB	1'b0	Programmable bit for masking the interrupt.
		2USB+OTG	1'b0	
		2USB+OTG+ISA	1'b0	1'b0: Mask interrupt
		2USB+OTG+GPIO	1'b1	1'b1: Unmask interrupt

7. Clocks and Resets

MCS9990 requires two input clock sources

- Differential reference clock of 100MHz (PCIE_REFCLKn/PCIE_REFCLKp) from PCIe interface
- External crystal oscillator of 12MHz

MCS9990 device requires one master reset coming from PCIe connector which is also called "Fundamental Reset". The PCIe Fundamental Reset does not reset MCS9990 USB host controllers. Please contact ASIX sales (sales@asix.com.tw) to get MCS9990 Errata document.

8. EEPROM Content Layout

The MCS9990 requires a 3.3V 24C32 or higher size I2C EEPROM (in 16-bit addressing mode, up to 400 KHz) for configuring various configurations and device parameters. Please refer to **MCS9990 EEPROM User Guide** for detailed EEPROM setting information.

MCS9990 supports 4 functional modes through mode select pins (Refer to Section 4 for details) and can be configure at more extended configuration modes via EEPROM.

MCS9990 Configuration Modes	EEPROM Required?
4 USB Host	Yes
3 USB Host	Yes
2 USB Host	Yes
1 USB Host	Yes
2 USB Host + OTG	Yes
1 USB Host + OTG	Yes
2 USB Host + OTG + GPIO	Yes
2 USB Host + GPIO	Yes
1 USB Host + OTG + GPIO	Yes
1 USB Host + GPIO	Yes
2 USB Host + OTG + ISA (4S/3S/2S2P/2S/2P/1S1P/1S/1P)	Yes
2 USB Host + ISA (4S/3S/2S2P/2S/2P/1S1P/1S/1P)	Yes
1 USB Host + OTG + ISA (4S/3S/2S2P/2S/2P/1S1P/1S/1P)	Yes
1 USB Host + ISA (4S/3S/2S2P/2S/2P/1S1P/1S/1P)	Yes

9. Power Management

MCS9990 cannot support well the power management feature. Please contact ASIX sales (sales@asix.com.tw) to get MCS9990 Errata document.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Stresses beyond the indicated values in table below may cause permanent damage to the MCS9990 device, even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced device life span and reduced reliability.

Symbol	Parameter	Min	Max	Units
+1.2V	Core Power Supply	-0.5	1.6	V
+3.3VIO	Power Supply of 3.3V I/O	-0.5	4.6	V
+3.3VIN_REG	Input Voltage of 3.3V I/O	-0.5	4.6	V
+3.3V	3.3V IO's with 5V tolerance capability	-0.5	5.8	V
T_{STG}	Storage Temperature	-45	150	°C
T_{OP}	Operating Temperature (MCS9990CV-AA)	0	70	°C
T_{OP}	Operating Temperature (MCS9990IV-AA)	-40	85	°C
T_j	Junction Operating temperature	0	125	°C
ESD HBM	(MIL-STD 883E Method 3015-7 Class 2)		2000	V
ESD MM	(JEDEC EIA/JESD22 A115-A)		200	V
CDM	(JEDEC JESD22 C101-A)		500	V
θ_{JA}	Thermal Resistance of Junction to Ambient		44	C/W
θ_{JC}	Thermal Resistance of Junction to Case		13	C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		0.54	C/W

C/W – ^{o}C per Watt , For Still Air Condition

10.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
+1.2V	1.2V Core Power Supply	1.08	1.2	1.32	V
+1.2VA	1.2V Analog/IO Power supply	1.14	1.2	1.32	V
+1.2VA_AUX	1.2V analog aux power for PCIE PHY	1.14	1.2	1.32	V
+3.3VIO	3.3V Digital IO Power Supply	2.97	3.3	3.63	V
+3.3VA_PLL	3.3V Analog Power Supply for internal PLL used in PCIE PHY	3.15	3.3	3.63	V
+3.3VA_AUX	3.3V analog aux power for PCIE PHY	3.15	3.3	3.63	V
+3.3VA	3.3V Analog supply voltage for USB PHY	3.0	3.3	3.6	V
	3.3V Analog supply voltage for internal PLL in the USB PHY	3.0	3.3	3.6	V
	3.3V Analog Power Supply for Voltage Detector used for USB OTG PHY	2.7	3.3	3.6	V
+3.3VIN_REG	Power supply input for Voltage Regulator	2.7	3.3	3.6	V
+1.2VOUT_REG	Regulator output Voltage	1.08	1.2	1.32	V
+1.2VOUT_REG	Current rating of Voltage Regulator			125	mA
$I_{1.2V}$	Current in 1.2V Supply		80	90	mA
$I_{1.2VA}$	Current in 1.2VA Supply		20	30	mA
$I_{3.3V}$	Current of 3.3V Supply		7	10	mA
$I_{3.3V\ A}$	Current in 3.3VA Supply		150	160	mA

10.3 Power Consumption

Symbol	Description	Min	Typ	Max	Units
4 USB full load at High-Speed					
I_{12}	Current Consumption of 1.2V	-	120	-	mA
I_{33}	Current Consumption of 3.3V	-	155	-	mA
USB no load					
I_{12}	Current Consumption of 1.2V	-	109	-	mA
I_{33}	Current Consumption of 3.3V	-	104	-	mA

10.4 PCI Express PHY Electrical Specifications

10.4.1 Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VCC12A	Analog supply current		1.14	1.2	1.32	V
VCC12A_AUX	Analog supply current		1.14	1.2	1.32	V
VCC33A_PLL	Analog supply current	-	3.15	3.3	3.63	V
VCC33A_AUX	Analog supply current	-	3.15	3.3	3.63	V
VCC12K	Digital supply current	-	1.14	1.2	1.32	V
I_{CC12}	1.2 V operating supply current	Operating in the P0 mode	-	39	-	mA
I_{CC33}	3.3 V operating supply current	Operating in the P0 mode	-	51	-	mA
$I_{CC(susp)}$	Suspend supply current	In the P2 mode without the beacon signal transmitted	-	90u	-	mA

10.4.2 Static Characteristics: Digital Pins

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage	-	-	-	0.4	V
V_{IH}	High-level input voltage	-	1.0	-	-	V
Output levels						
V_{OL}	Low-level output voltage	-	-	-	0.1	V
V_{OH}	High-level output voltage	-	VCC−0.1	-	-	-

10.4.3 Static Characteristics: Analog I/O Pins

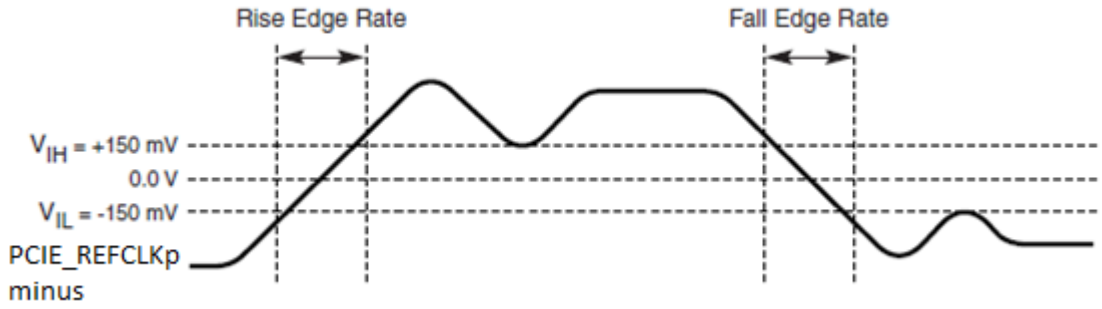
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Input levels (RX)						
$V_{RX-DIFF-PP}$	Differential RX peak-peak voltage	2 * |VRX(DIP) – VRX(DIN)|, measured at the connection of receiver's near end.	175	-	1200	mV
V_{IDLE}	Electrical idle detect threshold	Peak voltage	65	-	175	mV
$V_{RX-CM-AC}$	RX AC common-mode voltage	Peak voltage	-	-	150	mV
Input levels (REFCLK, 100MHz)						
Rising Edge Rate	Rising Edge Rate (Note 1 & 2)	-	0.6	-	4.0	V/ns
Falling Edge Rate	Falling Edge Rate (Note 1 & 2)	-	0.6	-	4.0	V/ns
V_{IH}	Differential Input High Voltage (Note 1)	-	+150	-	-	mV
V_{IL}	Differential Input Low Voltage (Note 1)	-	-	-	-150	mV
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation) (Note 1 & 3)	-	9.847		10.203	ns
Output levels (TX)						
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	2 * |VTX(DOP) – VTX(DON)|, measured at the connection of transmitter's near end.	800	-	1200	mV
T_{TX-EYE}	Transmitter eye including all jitter sources	Does not include SSC or Refclk jitter	0.75	-	-	UI
$V_{TX-IDLE-AC}$	Electrical idle differential peak output voltage	-	-	-	20	mV
V_{T-D-R}	The amount of voltage change allowed during receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	600	mV
$V_{TX\_CM\_AC}$	TX AC common-mode voltage	Measured as AC RMS value	-	-	20	mV
$V_{TX\_DEM-ratio}$	TX de-emphasis level	Non-transient bits are driven out with degrading amplitude	-3	-	-4	dB
F_{BEACON}	A signal of wake-up mechanism	Signal frequency	1	-	15	MHz

Resistance						
R_{RX}	Built-in receiver input impedance	-	40	50	60	Ω
R_{TX}	Built-in driver output impedance	-	40	50	60	Ω
Capacitance						
C_{TX}	AC coupling capacitor	-	75	-	200	nF

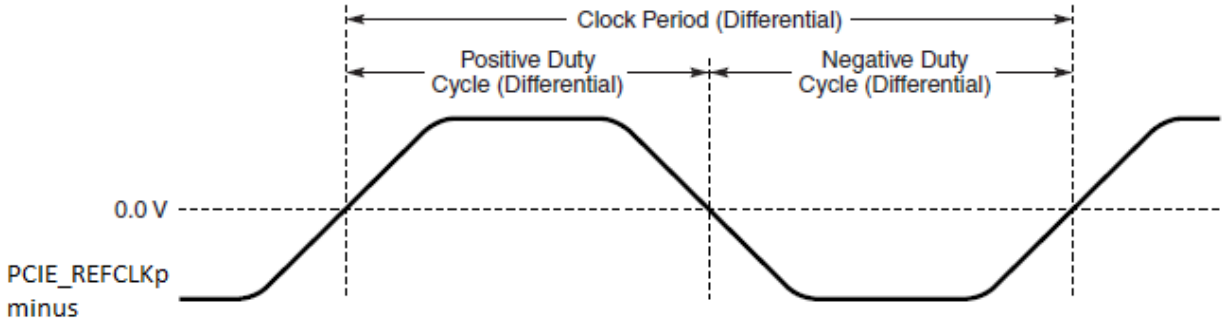
Notes:

1. Measurement taken from differential waveform.
2. Measured from -150 mV to +150 mV on the differential waveform (derived from PCIE_REFCLKp minus PCIE_REFCLKn). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See below "Differential Measurement Points for Rise and Fall Time" figure for details.
3. Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation. See below "Differential Measurement Points for Duty Cycle and Period" figure for details.

Differential Measurement Points for Rise and Fall Time:

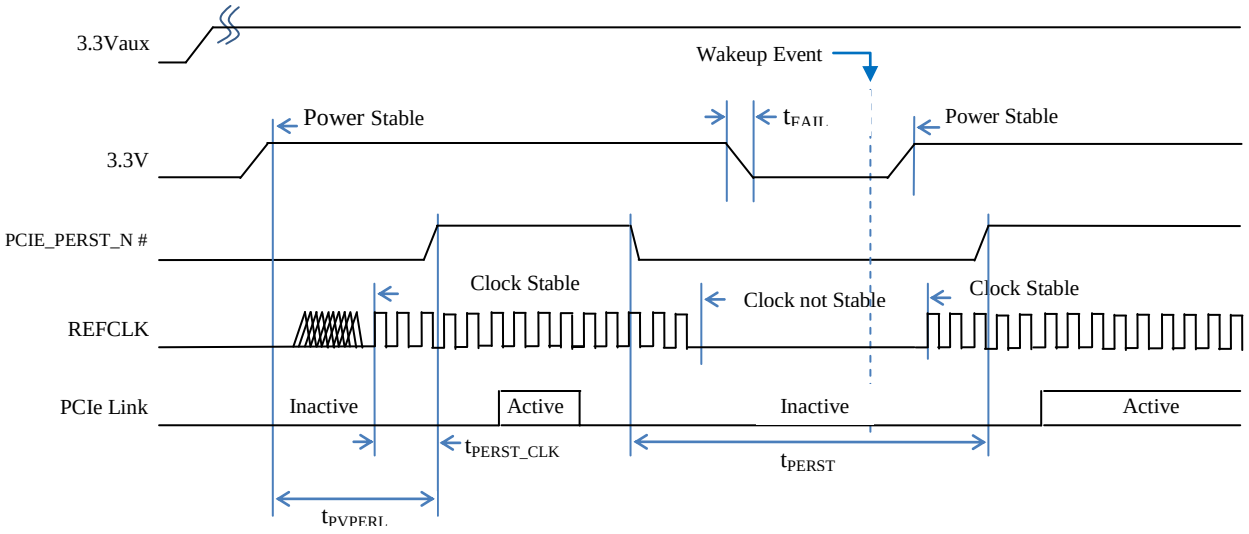


Differential Measurement Points for Duty Cycle and Period:



10.4.4 Auxiliary Signal Timing (power up & reset)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PVPERL}	Power stable to PCIE_PERST_N inactive		100			ms
$t_{PERST-CLK}$	REFCLK stable before PCIE_PERST_N inactive		100			µs
t_{PERST}	PCIE_PERST_N active time		100			µs
t_{FAIL}	Power level invalid to GND inactive				500	ns



10.5 USB PHY Electrical Specifications

10.5.1 Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
VCCA	Analog power supply	VCC33A_HSRT and VCC33A_PLL belong to the VCCA group		3.0	3.3	3.6	V
VCC	Digital power supply	VCC12D_U20		1.08	1.2	1.32	V
V_{noise}	Allowable power noise on analog supply	1 Hz ~ 100 kHz		-	-	300	mV
V_{noise}	Allowable power noise on digital supply	1 Hz ~ 100 kHz		-	-	100	mV
I_{VCC33A_HSRT}	Operating current of VCC33A_HSRT domain in different modes	-	At HS (480 Mbps)	-	-	35	mA
			At FS (12 Mbps)	-	-	20	mA
			At LS (1.5 Mbps)	-	-	15	mA
			In suspend mode (Without pull-up resistor connected on DP)	-	-	5	µA
I_{VCC33A_PLL}	Operating current of VCC33A_PLL domain in different modes	-	At HS (480 Mbps)	-	-	7	mA
			At FS (12 Mbps)	-	-	6	mA
			At LS (1.5 Mbps)	-	-	6	mA
			In suspend mode (Without pull-up resistor connected on DP)	-	-	5	µA
I_{VCC12D_U20}	Operating current of VCC12D_U20 domain in different modes	-	At HS (480 Mbps)	-	-	4	mA
			At FS (12 Mbps)	-	-	2	mA
			At LS (1.5 Mbps)	-	-	2	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		In suspend mode at 25 ℃ (Without pull-up resistor connected on DP)	-	-	200	μA
		In suspend mode at 125 ℃ (Without pull-up resistor connected on DP)	-	-	2	mA
$I_{OZ5.25V}$	5-V tolerance current	Measured at DP/DM in suspend mode	-	-	100	uA

10.5.2 Static Characteristics: Digital Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage	-	-	-	0.8	V
V_{IH}	High-level input voltage	-	2.0	-	-	V
Output levels						
V_{OL}	Low-level output voltage	-	-	-	0.2	V
V_{OH}	High-level output voltage	-	VCC − 0.2	-	-	V

10.5.3 Static Characteristics: Analog I/O Pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB 2.0 transceiver (HS)						
Input levels (Differential receiver)						
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$ Measured at the connection as an application circuit.	300	-	-	mV
V_{HSCM}	High-speed data signaling common mode voltage range	-	−50	-	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch detected	-	-	100	mV
		No squelch detected	200	-	-	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection detected	625	-	-	mV
		Disconnection not detected	-	-	525	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output levels						
V_{HSOI}	High-speed idle level output voltage (Differential)	-	−10	-	10	mV
V_{HSOL}	High-speed low level output voltage (Differential)	-	−10	-	10	mV
V_{HSOH}	High-speed high level output voltage (Differential)	-	360	400	440	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential)	-	700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential)	-	−900	-	−500	mV
$I_{DP/DM}$	Allowable output current of DP/DM	When the termination is 45 Ω ±10%	14.55	17.78	21.79	mA
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
Z_{HSTERM}	Differential impedance	-	76.5	90	103.5	Ω
USB 1.1 transceiver (FS/LS)						
Input levels (Differential receiver)						
V_{DI}	Differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common mode voltage	-	0.8	-	2.5	V
ZHSDRV	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
RPU1	Pull-up resistor during idle	Equivalent resistance used for the internal chip	900	-	1575	Ω
RPU2	Driver output resistance	Equivalent resistance used for the internal chip	525	-	1515	Ω
RPD	Driver output resistance	Equivalent resistance used for the internal chip	14.25	-	24.8	kΩ
Input levels (Single-ended receiver)						
V_{SE}	Single-ended receiver threshold	-	0.8	-	2.0	V
Output levels						
V_{OL}	Low-level output voltage	-	0	-	0.3	V
V_{OH}	High-level output voltage	-	2.8	-	3.6	V

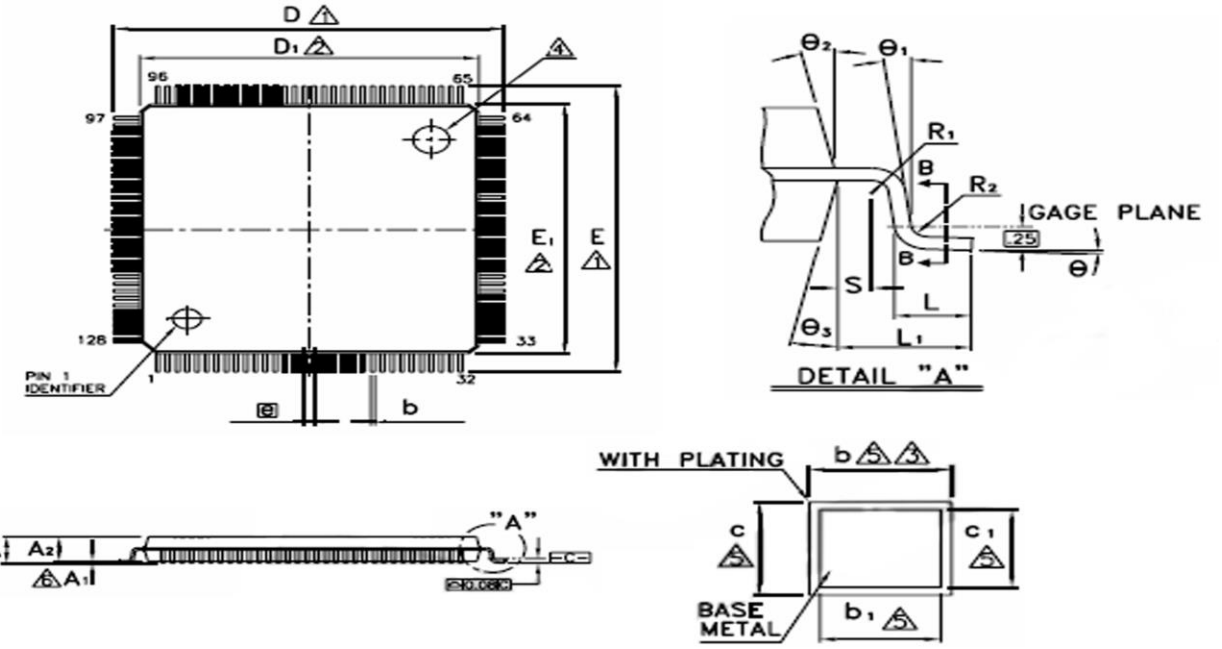
10.5.4 Dynamic Characteristics: Analog I/O Pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver characteristics						
High-speed mode						
$T_{HSRDRATE}$	High-speed TX data rate	-	479.76	-	480.24	Mbps
$T_{HSRDRATE}$	High-speed RX data rate	-	479.76	-	480.24	Mbps
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Full-speed mode						
$T_{FSDRATE}$	Full-speed TX data rate	-	11.994	-	12.006	Mbps
$T_{FSRDRATE}$	Full-speed RX data rate	-	11.97	-	12.03	Mbps
t_{FR}	Rise time	CL = 50 pF 10% ~ 90% of |VOH – VOL|	4	-	20	ns
t_{FF}	Fall time	CL = 50 pF 90% ~ 10% of |VOH – VOL|	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (tFR/tFF)	Excluding the first transition from idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3	-	2.0	V
Low-speed mode						
$T_{LSDRATE}$	Low-speed TX data rate	-	1.49925	-	1.50075	Mbps
$T_{LSRDRATE}$	Low-speed RX data rate	-	1.49625	-	1.50375	Mbps
t_{LR}	Rise time	CL = 200 pF ~ 600 pF 10% ~ 90% of |VOH – VOL|	75	-	300	ns
t_{LF}	Fall time	CL = 200 pF ~ 600 pF 90% ~ 10% of |VOH – VOL|	75	-	300	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{LRMA}	Differential rise/fall time matching (tLR/tLF)	Excluding the first transition in the idle mode	80	-	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition in the idle mode	1.3	-	2.0	V
Driver timing						
Full-speed mode						
VI, FSE0, OE to DP, DM Propagation delay	For a detailed description of VI, FSE0, and OE, please refer to USB 1.1 specification.		-	-	15	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition	-	-2	-	5	ns
T_{JR1}	Receiver jitter	To next transition	-18.5	-	18.5	ns
T_{JR2}	Receiver jitter	For paired transition	-9	-	9	ns
T_{FEOPT}	Source SE0 interval of EOP	-	160	-	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	-	82	-	-	ns
T_{FST}	Width of SE0 interval during differential transition	-	-	-	14	ns
Low-speed mode						
T_{LDEOP}	Source jitter for differential transition to SE0 transition	-	-40	-	100	ns
T_{JR1}	Receiver jitter	To next transition	-75	-	75	ns
T_{JR2}	Receiver jitter	For paired transition	-45	-	45	ns
T_{LEOPT}	Source SE0 interval of EOP	-	1.25	-	1.5	µs
T_{LEOPR}	Receiver SE0 interval of EOP	-	670	-	-	ns
T_{LST}	Width of SE0 interval during differential transition	-	-	-	210	ns
Not specified: Low-speed delay time is dominated by slow tLR and tLR.						
Receiver timing						
Full-speed mode						

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{PLH(rcv)}$ $t_{PHL(rcv)}$	Receiver propagation delay (DP; DM to RX_RCV)	For a detailed description of RCV, please refer to USB 1.1 specification.	-	-	30	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to RX_DP, RX_DM)	-	-	-	30	ns

11. Mechanical Dimensions



Note:

1. TO BE DETERMINED AT SEATING PLANE

2. Dimensions D1 and E1 DO NOT include MOLD PROTRUSION. D1 and E1 are MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

4. EXAT SHAPE OF EACH CORNER IS OPTIONAL.

5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATINF PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

7. CONTROLLING DIMENSION: MILLIMETER

Symbol	Dimension in mm		
	Min	Nom	Max
A	-	-	1.60
A_1	0.05	-	-
A_2	1.35	1.40	1.45
b	0.13	0.18	0.23
b_1	0.13	0.16	0.19
c	0.09	-	0.20
c_1	0.09	-	0.16
D	15.85	16.00	16.15
D_1	13.90	14.00	14.10
E	15.85	16.00	16.15
E_1	13.90	14.00	14.10
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	-	-
R_2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ_1	0°	-	-
θ_2	12°TYP		
θ_3	12°TYP		

12. Errata

Please contact ASIX sales (sales@asix.com.tw) to get MCS9990 Errata document.

Revision History

Revision	Date	Comment
1.0	28/02/2009	Initial release to customers
1.1	30/06/2009	Aesthetic / Font changes made in Page#1 & Page#2
1.2	21/08/2009	Electrical characteristics updated under section 10
1.3	23/02/2011	Document updated for the addition of Industrial grade part number, under ordering information
2.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram in Section 1.4.
2.01	2011/09/21	1. Added Section 10.3, 10.4 and 10.5 to indicate the power consumption, USB/PCIe PHY Electrical Characteristics spec.
2.02	2011/10/03	1. Added Section 10.4.4 to indicate the power-up and reset timing.
2.03	2011/11/25	1. Added the PCIe REFCLK signals timing spec. in Section 10.4.3.
2.04	2012/03/20	1. Modified some descriptions in Section 3.1, 4, 8, 10.1.
2.05	2012/03/30	1. Modified some descriptions in Section 1.1, 1.2, 1.3, 2.
2.06	2012/05/10	1. Modified some descriptions in Section 1.7, 10.1.
2.07	2012/10/05	1. Modified some descriptions in Section 8.
2.10	2014/09/12	1. Modified some descriptions in Section 3.5, 5.
2.20	2014/12/10	1. Modified some descriptions in Section 2, 4, 8.
3.00	2015/03/10	1. Added Section 12 “Errata”. 2. Modified some descriptions in Section 1, 2, 6-2, 7, 9.

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