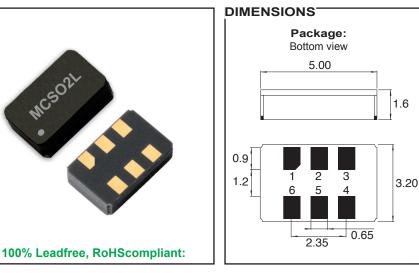
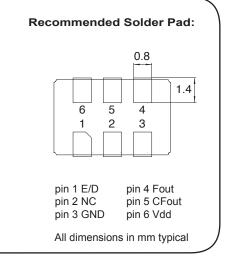


MCSO2L family package 5×3.2 mm From 40 MHz to 130 MHz LVDS Output





SMT LVDS Clock oscillator in ceramic package Fundamental quartz mode frequency High shock and vibration resistance Wide temperature range Low aging Ultra low internal MSL Very fast start-up Excellent solderability Swiss made quality Customer specification on request

DESCRIPTION:

This SMD oscillator in ceramic package has been specially designed for surface mount using infrared, vapor phase or epoxy techniques.

APPLICATIONS:

- Avionics

- Airborne equipments
- Remote control
- Security application
- Radio Transceiver
- Microprocessor clocks

The MCSO2L's are supplied on trays (128 pcs / tray) For pick-and-place equipment, the parts are available in 12mm tapes

with 250 parts min

1000 parts min

ELECTRICAL	
CHARACTERISTICS AT +25°C	

	range)	ΔF/F	≤±100	ppm
Frequency stability version T Over temperature range (see ordering info) Including: adjustment at +25°C long term aging 1 year over supply voltage ±5%		ΔF/F	≤±50	ppm
Supply voltage ± 5	5% 1)*	Vdd	2.5 / 3.3	V
Input current		ldd	see table 1	
Output signal (load	d 100 ohm)		LVDS	
Symmetry (max)			45 / 55	%
Rise & fall time (20	0% to 80%)		<1	ns
Level Logic low (Typ/min)			1.1 / 0.9	V
Level Logic high (Typ/max)			1.4 / 1.6	V
Start-up time		t	<5	ms
Jitter RMS (1KHz	to 1MHz)		<0.3	ps
Phase noise typica Static conditions BW = 1Hz	al at 100MHz 10Hz 100Hz 1 kHz 10 kHz 10 kHz 100kHz		-70 -100 -125 -145 -150	dBc/ Hz

TABLE 1: Idd (Without load)

	Frequency	F= 40MHz	100MHz	130MHz	
W	=Vdd = 2.5V	< 5mA	< 10mA	< 20mA	
V	=Vdd = 3.3V	< 10mA	< 15mA	< 25mA	

STANDARD FREQUENCIES:

Frequency «MHz»			
40	80	100	128
Other frequencies on request			

-65 to +125°C

10 to 2000Hz / 50g

5000g / 0.3ms / 1/2 sine

ENVIRONMENTAL	

CHARACTERISTICS:

TERMINATIONS AND PROCESSING:

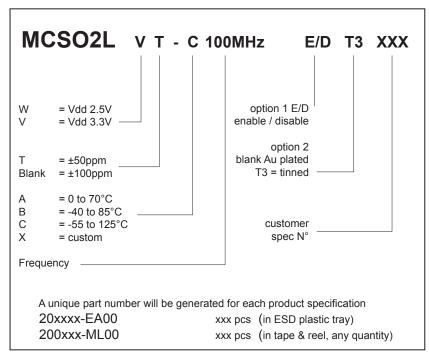
Reflow soldering (peak)	+260°C / 10s max
Package	Ceramic 5 x 3.2 x 1.6mm
Lids	Ceramic
Terminations option T3 on request	with tinned Ag/Cu/Sn
E/D option 1 on request Reaction time < 1µs	$\begin{array}{ccc} \mbox{Pin 1 open} \rightarrow \mbox{Pin 3 Clock} \\ \mbox{H} \rightarrow & \mbox{Clock} \\ \mbox{L} \rightarrow & \mbox{Low} \end{array}$

- No power E/D function (pin 1) before Vdd is setting on

Storage temp. range

Vibration resistance (survival) Shocks resistance (survival)





All specifications subject to change without notice.

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