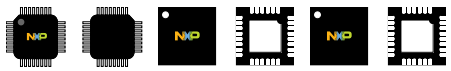
MCXA153, A152, A143, A142, A133, A132 Data Sheet

Arm® Cortex®-M33 48MHz or 96MHz 32-bit MCU, up to 128KB Flash

Rev. 4 — Sept 2024

Data Sheet: Technical Data

MCXA13x
MCXA14x
MCXA15x



LQFP64	HVQFN32	HVQFN48
10 x 10 x 1.4 mm, 0.5 mm	5 x 5 x 0.9 mm, 0.5 mm	7 x 7 x 0.9 mm, 0.5 mm

Features

- Arm Cortex-M33 48MHz(A14x) or 96MHz(A15x, A13x) with 381 CoreMark (3.97 CoreMark/MHz)
- Up to 128 KB Flash, 32 KB SRAM, up to 8 KB SRAM with ECC
- All RAM can be retained down to Deep Power Down mode
- -40 °C to 125 °C temperature range
- Down to 53 µA/MHz active current, 6.5 µA Power Down mode with all SRAM retntion 394 nA Deep Power Down current

Core

- Arm 32-bit Cortex-M33 CPU, no FPU, no DSP extension instruction set, no TrustZone, no MPU

Memories

- Single-bank Flash: Up to 128 KB FLASH with ECC (support one bit correction and two bits detection)
- Cache Engine with 4 KB RAM
- Up to 32 KB RAM, configurable as up to 8 KB RAM with ECC (support single bit correction, two bits detection)
- All RAM can be retained down to Deep Power Down mode
- 16 KB ROM

Security

- 128-bit Universal Unique Identifier (UUID) per device in accordance with IETF's RFC4122 version 5 specification
- Device lifecycle management
- Flash read/write/execute permission protect by MBC and lockable
- Implicit-protected Flash Region (IFR)
- Security Monitoring
  - — Code Watchdog for code flow integrity checking
  - — GLIKEY enhances protection against attacks to gain unauthorized access to sensitive registers

Low-Power Performance

- Active: 53 µA/MHz in Active Mode (While(1) executing from flash, 3.3 V @25 °C)
- Deep Sleep: 20.28 µA, 7.4 µs wake-up (3.3 V @25 °C)
- Power Down: 6.5 µA, 17.1 µs wake-up (full SRAM retention, 3.3 V@ 25 °C)
- Deep Power Down: 394 nA, 2.36 ms wake-up (wake timer disabled, reset pin enabled, all SRAM off, 3.3 V @25 °C)

System and Clocks

- 192 MHz MHz free-running oscillator (FRO192M)
- 12 MHz free-running oscillator (FRO12M)

- 16 kHz free-running oscillator (FRO16k)
- Up to 50 MHz crystal oscillator
- Hardware and Software Watchdogs
- Asynchronous DMA modules (4-channels)

Communication interfaces

- 2x LPSPI, 1x LPI2C, 3x LPUART
- 1x I3C
- USB Full-speed (Device) with on-chip FS PHY

Advanced Motor Control

- 1x FlexPWM each with 3 submodules, providing 6 complementary outputs of PWM (no Nanoedge module)
- 1x Quadrature Decoder (eQDC)
- 1x AOI (AND/OR/INVERT) module support up to 4 output trigger

Analog

- 1x 16-bit ADC
  - up to 3.2 Msps in 16-bit mode, and 4 Msps in 12-bit mode
  - up to 24 ADC Input channels (depending on the package)
  - one integrated temperature sensor
- 2x Low power Comparators (LPCMP) with 8 input pins and 8-bit DAC as internal reference
  - 1x LPCMP is functional down to Deep Power Down mode

Timers

- 3x 32-bit standard general-purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests
- Low power timer
- Frequency measurement timer
- Windowed watchdog Timer
- Wake timer
- Micro-tick timer (UTICK)
- OS event timer

General-purpose input/outputs

- Up to 52 GPIOs
  - Up to eight 20 mA IO
  - 50 MHz IO on P1 and P3
  - Up to 19-pin wake-up sources function down to Deep Power Down mode
  - Support 1.71 V~3.6 V IO supply range

Power Management

- Integrated voltage regulator
  - Core LDO, other LDOs
- Operating voltage: 1.71 V to 3.6 V

- IOs: 1.71 V - 3.6 V full-performance

Target Applications

Industrial

- Energy Storage and Management System
- Smart Metering
- Factory Automation
- Industrial HMI
- Mobile Robotics Ecosystem
- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor (PMSM)

Smart Home

- Home Control Panel
- Major Home Appliances
- Robotic Appliance
- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch

Part Number	Marking	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIOs	Pin Count	Package	Packing
MCXA153VLH	MCXA153VLH	96	128	32	52	64	LQFP	Tray
MCXA153VFT	MCXA153VFT	96	128	32	41	48	HVQFN	Tray
MCXA153VFM	MCXA153VFM	96	128	32	26	32	HVQFN	Tray
MCXA152VLH	MCXA152VLH	96	64	16	52	64	LQFP	Tray
MCXA152VFT	MCXA152VFT	96	64	16	41	48	HVQFN	Tray
MCXA152VFM	MCXA152VFM	96	64	16	26	32	HVQFN	Tray
MCXA143VLH	MCXA143VLH	48	128	32	52	64	LQFP	Tray
MCXA143VFT	MCXA143VFT	48	128	32	41	48	HVQFN	Tray
MCXA143VFM	MCXA143VFM	48	128	32	26	32	HVQFN	Tray
MCXA142VLH	MCXA142VLH	48	64	16	52	64	LQFP	Tray
MCXA142VFT	MCXA142VFT	48	64	16	41	48	HVQFN	Tray
MCXA142VFM	MCXA142VFM	48	64	16	26	32	HVQFN	Tray

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Part Number	Marking	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIOs	Pin Count	Package	Packing
MCXA133VFT	MCXA133VFT	96	128	32	44	48	HVQFN	Tray
MCXA133VFM	MCXA133VFM	96	128	32	29	32	HVQFN	Tray
MCXA132VFT	MCXA132VFT	96	64	16	44	48	HVQFN	Tray
MCXA132VFM	MCXA132VFM	96	64	16	29	32	HVQFN	Tray

Table 1. Device Revision Number

Device Mask Set Number	DIE_ID	JTAG ID Register[PRN]
0P07H	0x0055F1A0	0x0726602B

Table 2. Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	MCXA1xxFS
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXAP64M96FS3RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCXA153_P07H
Package drawing	Package dimensions are provided in package drawings.	• LQFP 64-pin: 98ASS23234W • HVQFN 48-pin: 98ASA01637D • HVQFN 32-pin:98ASA02110D
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso

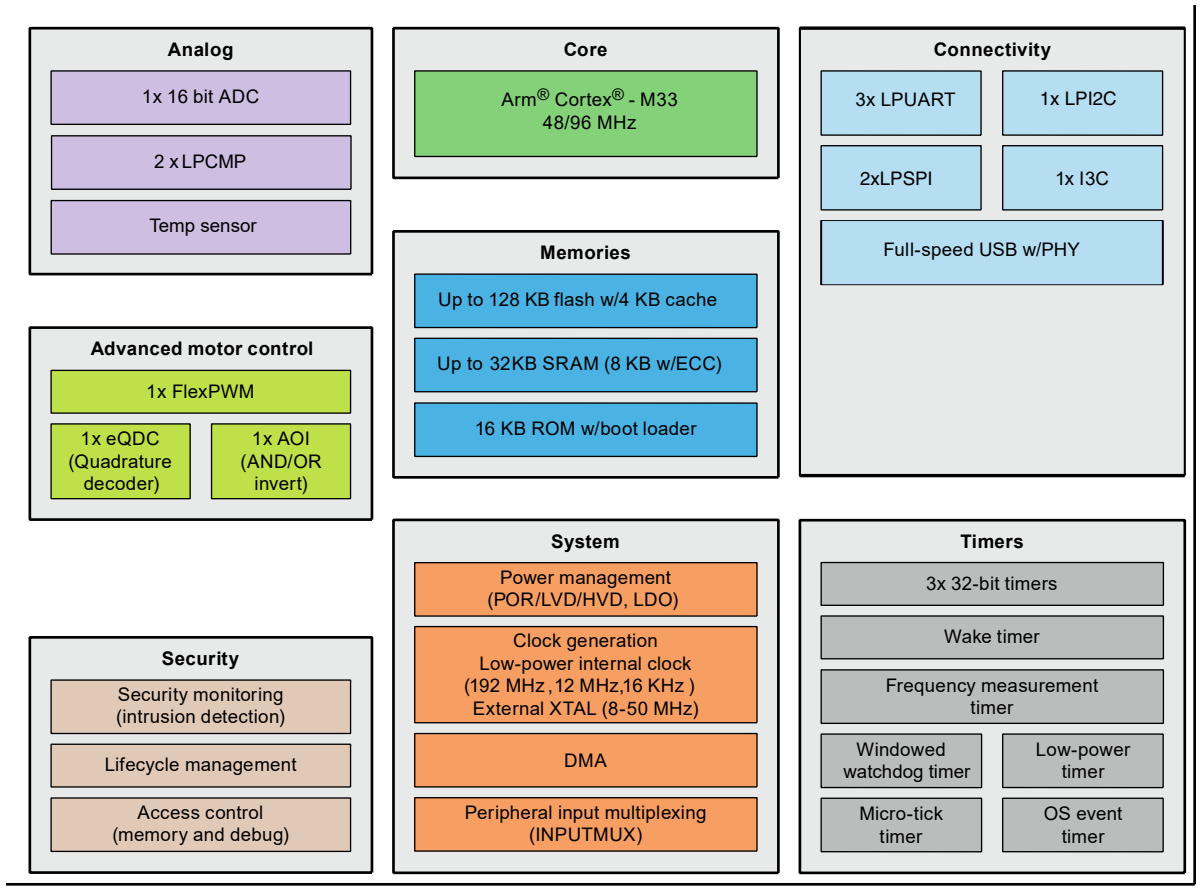

Figure 1. Block Diagram

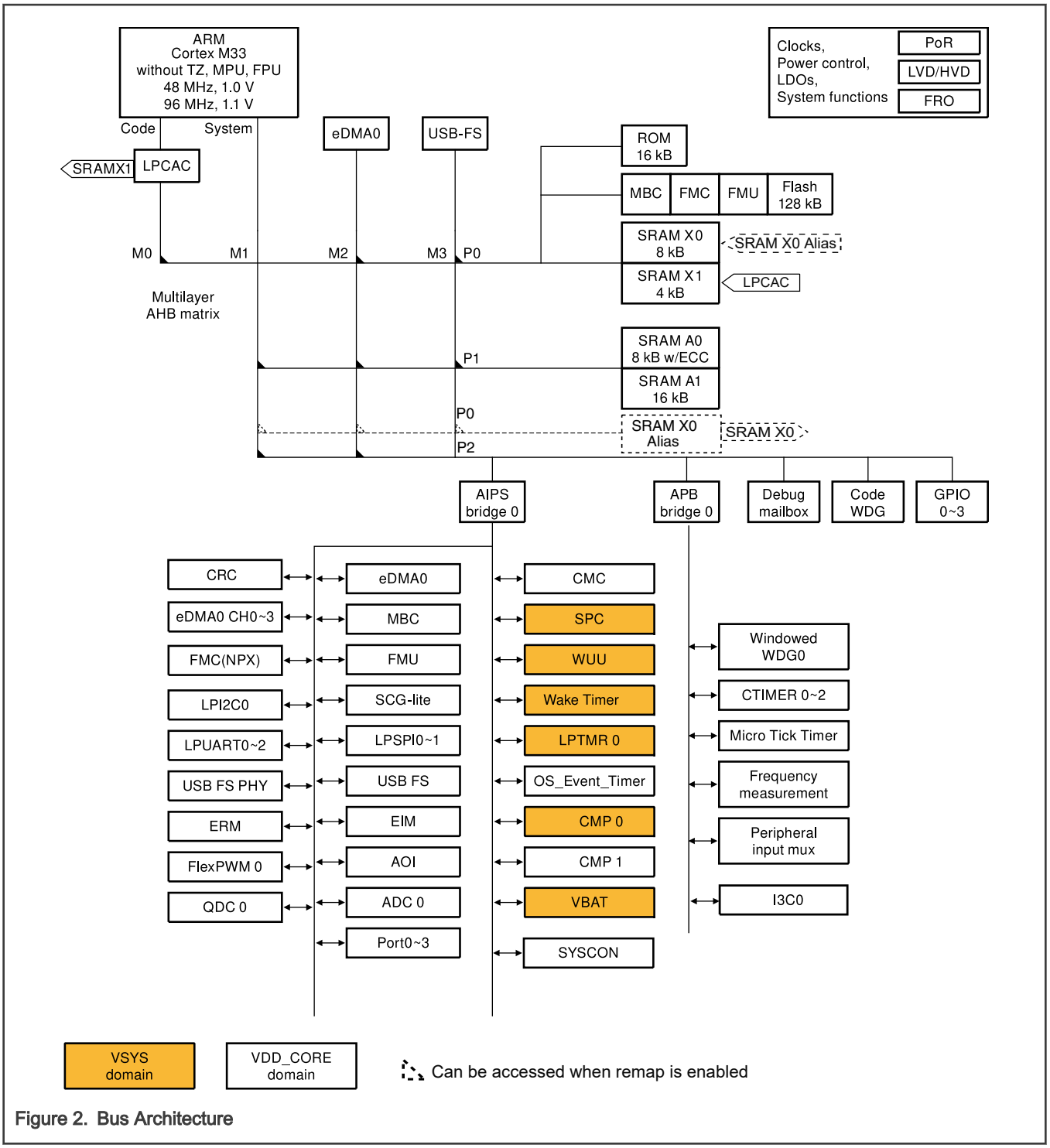

Figure 2. Bus Architecture

Contents

1 Feature Comparison

	Part Number	MCXA133	MCXA132	MCXA143	MCXA142	MCXA153	MCXA152
Core Platform	Core Cortex-M33	96 MHz	96 MHz	48 MHz	48 MHz	96 MHz	96 MHz
	Cache	4 kB					
	DMA	4 Channels					
	Wakeup Unit (WUU)	YES					
	Peripheral Input Multiplexing (INPUTMUX)	YES					
Clock	FRO192M	192 MHz	192 MHz	48 MHz	48 MHz	192 MHz	192 MHz
	FRO12M	12 MHz					
	FRO16K	16.384 KHz					
	System Crystal Oscillator (SOSC)	8-50 MHz					
Memory	Flash	128 kB	64 kB	128 kB	64 kB	128 kB	64 kB
	SRAM	32 kB including 8 kB with ECC	16 kB including 8 kB with ECCC	32 kB including 8 kB with ECC	16 kB including 8 kB with ECCC	32 kB including 8 kB with ECC	16 kB including 8 kB with ECCC
	Error Injection Module (EIM)	YES					
	Error Recording Module (ERM)	YES					
Security	Life Cycle for Read Out Protection (ROP)	YES					
	Memory Block Checker (MBC)	YES					
	GLIKEY	YES					
	UUID	128-bit					
	Code Watchdog (CDOG)	1					

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	Cyclic Redundancy Check (CRC)	1					
Communication Interfaces	LPI2C	1					
	LPUART	3					
	LPSPI	2					
	I3C	1					
	USB FS Device	0	0	1	1	1	1
Analog	Low Power Comparator (LPCMP)	2					
	ADC	1					
Motor Control	FlexPWM	1					
	AND/OR INVERT (AOI)	1					
	Enhanced Quadrature Decoder (eQDC)	1					
Timer	Standard counter/timers (CTimer)	3					
	Low-Power Timer (LPTMR)	1					
	Micro-Tick Timer (UTICK)	1					
	OS Event Timer	1					
	Windowed Watchdog Timer	1					
	Frequency Measurement (FREQME)	1					
	Wake Timer	1					
	5V tolerant IO [1]	2					

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	High Drive IO (20 mA) [2]	Up to 8					
	50 MHz IO [3]	Up to 15					
Packages [4]	LQFP64	–[5]	–[5]	52	52	52	52
	HVQFN48	44	44	41	41	41	41
	HVQFN32	29	29	26	26	26	26
	Temperature Range	-40 °C to 125 °C					

1. P3_27, P3_28 are 5V tolerant IOs.
2. P1_8,P1_9,P1_30,P1_31,P3_1,P3_0,P0_16,P0_17 are High Drive IOs
3. 50 MHz IOs are located on P1, P3 ports
4. Show the package types and GPIO numbers
5. Package is not available on this part

2 Ratings

2.1 Thermal handling ratings

Table 3. Thermal handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
TSTG	Storage temperature [1]	–55	—	150	°C	—
TSDR	Solder temperature, lead-free [2]	—	—	260	°C	—

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

2.2 Moisture handling ratings

Table 4. Moisture handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
MSL	Moisture sensitivity level [1]	—	—	3	—	—

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

2.3 ESD handling ratings

Table 5. ESD handling ratings

Description	Rating	Unit	Notes
Electrostatic discharge voltage, human body model	+/-2000	V	[1]

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Table 5. ESD handling ratings (continued)

Description	Rating	Unit	Notes
Electrostatic discharge voltage, charged-device model	+/-500	V	2
Electrostatic discharge voltage, charged device model (corner pins)	+/-750	V	2
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	—	3

1. Determined according to ANSI/ESDA/JEDEC Standard JS-001-2023, For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Device Level.
2. Determined according to ANSI/ESDA/JEDEC Standard JS-002-2022, For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level.
3. Determined according JEDEC Standard JESD78F, IC Latch-Up Test.

2.4 Voltage and current maximum ratings

The table below shows the absolute minimum and maximum ratings for the device. If the values are violated, the device could be damaged. See Voltage and current operating requirements for operating requirements, and Terminology and guidelines for definitions of terms.

2.4.1 Voltage and current maximum ratings

Table 6. Voltage and current maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage for Port 0, Port 1, Port 2 and Port 3	-0.3	—	3.63	V	—
VDD_ANA	Supply voltage for ADC	-0.3	—	3.63	V	—
VDD_USB	Supply voltage for USB analog	-0.3	—	3.63	V	—
VUSB0_Dx	USB0_DP and USB0_DM input voltage	-0.3	—	3.63	V	—
VDIO	Digital input voltage	-0.3	—	VDD + 0.3	V	—
VDIO_5VTOL	Digital input voltage for 5V tolerant I/O pins	-0.3	—	min(VDD + 3.6V, 5.5V)	V	—
VAIO	Analog input voltageAnalog pins are defined as pins that do not have an associated general-purpose I/O port function. 1	-0.3	—	VDD_ANA + 0.3	V	—
IDD	Digital supply current 2	—	—	100	mA	—
ID	Maximum current single pin limit (digital output pins)	-25	—	25	mA	—

1. Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
2. This limit is per supply pin. It includes all power pins, including VDD, VDD_ANA, VDD_USB.

2.5 Required Power-On-Reset (POR) Sequencing

- VDD and VDD_ANA must be same voltage

3 General

3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

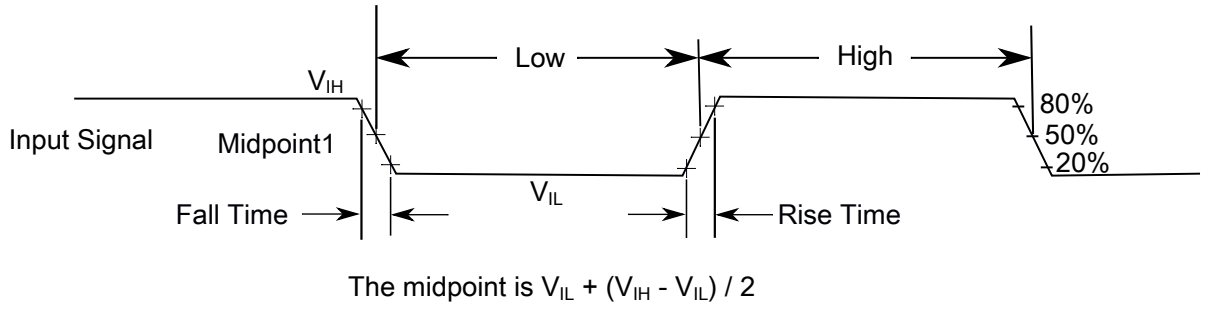

Figure 3. Input signal measurement reference

3.2 Nonswitching electrical specifications

3.2.1 Voltage and current operating requirement

Table 7. Voltage and current operating requirement

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply Voltage for IO, LDO, Flash, and LPCMP	1.71	—	3.6	V	—
VDD_ANA	Supply voltage for ADC	VDD - 0.1	—	VDD + 0.1	V	—
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	-0.1	—	0.1	V	—
VDD_USB	Supply voltage for USB analog	3.0	—	3.6	V	—
VIH	Input high voltage	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIH_5VTOL	Input high voltage of 5V tolerant IO	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIL	Input low voltage	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VIL_5VTOL	Input low voltage of 5 V tolerant IO	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VHYS	Input hysteresis	0.1 × VDD	—	—	V	—

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Table 7. Voltage and current operating requirement (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
VHYS_5VTOL	Input hysteresis of 5 V tolerant IO	0.1 × VDD	—	—	V	—
IICIO	IO pin DC injection current — per pin [1]	-3	—	—	mA	VIN < VSS-0.3 V (negative current injection)
IICIO	IO pin DC injection current — per pin [1]	—	—	3	mA	VIN > VDD+0.3 V (positive current injection)
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	-25	—	—	mA	Negative current injection
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	—	—	25	mA	Positive current injection
VODPU	Open drain pullup voltage level [2]	VDD	—	VDD	V	—

1. All I/O pins are internally clamped to VSS and VDD through an ESD protection diode. If VIN is greater than VDD_MIN(=VSS-0.3 V) or is less than VDD_MAX(=VDD+ 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (-0.3 - VIN)/(-IICIOmin). The positive injection current limiting resistor is calculated as R=(VIN-VDD_MAX)/IICIOmax. The actual resistor should be an order of magnitude higher to tolerate transient voltages
2. Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD as appropriate.

3.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD

3.2.2.1 VDD supply HVD, LVD, and POR Operating Requirements

Table 8. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VHVDH_VDD	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	—
VHVDH_HYS_VDD	VDD High-voltage inhibit reset/ recover hysteresis	—	38	—	mV	—
VLVDH_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - high range	2.567	2.619	2.673	V	—
VLVDH_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - high range	—	27	—	mV	—

Table continues on the next page...

Table 8. VDD supply HVD, LVD, and POR Operating Requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
VLVDL_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - low range	1.618	1.651	1.684	V	—
VLVDL_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - low range	—	16	—	mV	—

3.2.3 Voltage and current operating behaviors

Table 9. Voltage and current operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 4 mA
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 2.5 mA
VOH	Output high voltage — High drive strength [1,2]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 6 mA
VOH	Output high voltage — High drive strength [1,2]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 3.75 mA
IOHT	Output high current total for all ports	—	—	100	mA	—
VOL	Output low voltage — Normal drive strength [1,3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 4 mA
VOL	Output low voltage — Normal drive strength [1,3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 2.5 mA
VOL	Output low voltage — High drive strength [1,2,3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 6 mA
VOL	Output low voltage — High drive strength [1,2,3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 3.75 mA
IOLT	Output low current total for all ports	—	—	100	mA	—
IIN	Input leakage current (per pin) for full temperature range [4]	—	0.02	1	µA	—
IIN	Input leakage current (per pin) at 25 °C [4]	—	0.001	0.025	µA	—
IIN	Input leakage current (total all pins) for full temperature range [4]	—	0.025	41	µA	—
IOZ	Hi-Z (off-state) leakage current (per pin)	—	0.02	1	µA	—
RPU	Internal pullup resistors	33	50	75	kΩ	—

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Table 9. Voltage and current operating behaviors (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
RPU (I3C)	Internal pullup resistors [5]	(VDD - 0.27 V)/3 mA	1.75	—	kΩ	—
RPD	Internal pulldown resistors	33	50	75	kΩ	—
RHPU	High-resistance pullup option (PCRx[PV] = 1) [6]	0.67	—	1.5	MΩ	—
RHPD	High-resistance pulldown option (PCRx[PV] = 1) [6]	0.67	—	1.5	MΩ	—
VBG	Bandgap voltage reference voltage	0.98	1.0	1.02	V	—

1. For the HD pads, when setting DSE1=1, the IOH/IOL are four times higher at the same VOH/VOL.
2. RESET_B pins are always configured in high drive mode
3. Open drain outputs must be pulled to VDD
4. Measured at VDD = 3.6 V.
5. Only I3C pins support this option
6. Only RESET_B pins support this option.

3.2.4 On-chip regulator electrical specifications

3.2.4.1 LDO_CORE electrical specifications

Table 10. LDO_CORE electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	LDO_CORE input supply voltage	1.71	—	3.6	V	—
ILOAD	LDO_CORE max load current	—	—	16	mA	Normal drive strength
ILOAD	LDO_CORE max load current	—	—	2	mA	Low drive strength
IDD	LDO_CORE current consumption	—	—	250	µA	Normal drive strength
IDD	LDO_CORE current consumption	—	—	500	nA	Low drive strength
IINRUSH	LDO_CORE inrush current	—	—	10	mA	—

3.2.5 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- CPU clock = 48 MHz
- AHB clock = 48 MHz
- Clock source = FIRC

3.2.5.1 Power mode transition operating behaviors

Table 11. Power mode transition operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tPOR	After a POR event, amount of time to execution of the first instruction (measured from the point where VDD reach 1.8V) across the operating temperature range of the chip. [1,2]	—	2.31	2.38	ms	—	—
tSLEEP	Sleep → Active [1,2,3,4]	—	0.21	0.25	µs	—	—
tDSLEEP	Deep Sleep → Active [1,2,3,4]	—	7.4	8.7	µs	—	—
tPWDN	Power Down → Active [1,2,3,5]	—	17.1	20.6	µs	—	—
tDPWDN	Deep Power Down → Active [1,2,3,4]	—	2.36	2.45	ms	—	—

1. Max value is mean+3 × sigma of tested values at the worst case of ambient temperature range and VDD 1.71 V to 3.6 V. Max values are based on characterization but not covered by test limits in production.
2. Typical value is the average of values tested at Temperature=25 ℃ and VDD=3.3 V
3. WFE used for low-power mode entry
4. SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured as same level for active and low power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL]=SPC->LP_CFG[CORELDO_VDD_LVL] = 01b).
5. SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x5B and the Core voltage level is configured as different level for active and low power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = 01b for active mode, SPC->LP_CFG[CORELDO_VDD_LVL] = 00b for low power mode)

3.2.6 Power consumption operating behaviors

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself including VDD, VDD_ANA
- VDD_USB current draw are not included
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered

3.2.6.1 Power consumption operating behaviors

Table 12. Power consumption operating behaviors

Symbol	Description	Condition[1]	Min	Typ	Max	Unit
IDD_ACT-MD_1[2]	While(1) loop executing from internal flash, All peripheral clocks disabled, CPU_CLK = 48 MHz; AHB_CLK = 48 MHz; SLOW_CLK = 12 MHz,	25 °C	—	2.54	—	mA
		105 °C	—	2.85	—	mA
		125 °C	—	3.11	—	mA

Table continues on the next page...

Table 12. Power consumption operating behaviors (continued)

Symbol	Description	Condition[1]	Min	Typ	Max	Unit
	CPU_CLK from FRO192M; Flash is configured to LP mode. VDD_CORE (1.0 V)					
IDD_ACT-MD_2	While(1) loop executing from internal flash, All peripheral clocks enabled, CPU_CLK = 48 MHz; AHB_CLK = 48 MHz; SLOW_CLK = 12 MHz, CPU_CLK from FRO192M. VDD_CORE (1.0 V).	25 °C	—	2.97	—	mA
		105 °C	—	3.29	—	mA
		125 °C	—	3.56	—	mA
IDD_ACT-MD-CM_1	Coremark executing from internal flash, All peripheral clocks disabled, CPU_CLK = 48 MHz; AHB_CLK = 48 MHz; SLOW_CLK = 12 MHz, CPU_CLK from FRO192M. Flash is configured to LP mode. VDD_CORE (1.0 V).	25 °C	—	2.82	—	mA
		105 °C	—	3.13	—	mA
		125 °C	—	3.38	—	mA
IDD_ACT-MD-CM_2	Coremark executing from internal flash, All peripheral clocks enabled, CPU_CLK = 48 MHz; AHB_CLK = 48 MHz; SLOW_CLK = 12 MHz, CPU_CLK from FRO192M. VDD_CORE (1.0 V).	25 °C	—	3.25	—	mA
		105 °C	—	3.57	—	mA
		125 °C	—	3.84	—	mA
IDD_ACT_SD_1	While(1) loop executing from internal flash, All peripheral clocks disabled, CPU_CLK = 96 MHz; AHB_CLK = 96 MHz; SLOW_CLK = 24 MHz, CPU_CLK from FRO192M. VDD_CORE (1.1 V)	25 °C	—	5.44	—	mA
		105 °C	—	5.85	—	mA
		125 °C	—	6.17	—	mA
IDD_ACT_SD_2	While(1) loop executing from internal flash, All peripheral clocks enabled, CPU_CLK = 96 MHz; AHB_CLK = 96 MHz; SLOW_CLK = 24 MHz, FRO192M output is 192MHz. VDD_CORE (1.1 V)	25 °C	—	6.92	—	mA
		105 °C	—	7.36	—	mA
		125 °C	—	7.68	—	mA
IDD_ACT_SD_CM_1	Coremark executing from internal flash, All peripheral clocks disabled, CPU_CLK = 96 MHz; AHB_CLK = 96 MHz; SLOW_CLK = 24 MHz, CPU_CLK from FRO192M. VDD_CORE (1.1 V)	25 °C	—	5.94	—	mA
		105 °C	—	6.33	—	mA
		125 °C	—	6.64	—	mA

Table continues on the next page...

Table 12. Power consumption operating behaviors (continued)

Symbol	Description	Condition[1]	Min	Typ	Max	Unit
IDD_ACT_SD_CM_2	Coremark executing from internal flash, All peripheral clocks enabled, CPU_CLK = 96 MHz; AHB_CLK = 96 MHz; SLOW_CLK = 24 MHz, CPU_CLK from FRO192M. FRO192M output is 192MHz. VDD_CORE (1.1 V)	25 °C	—	7.42	—	mA
		105 °C	—	7.84	—	mA
		125 °C	—	8.14	—	mA
IDD_SLEEP_SD	Core in WFI; CPU_CLK = OFF, All peripheral clocks disabled, AHB_CLK = 96 MHz; SLOW_CLK = 24 MHz,AHB_CLK from FRO192M, LDO_CORE drive strenth is normal. VDD_CORE (1.1 V)	25 °C	—	2.92	—	mA
		105 °C	—	3.29	—	mA
		125 °C	—	3.60	—	mA
IDD_SLEEP_MD	Core in WFI; CPU_CLK = OFF, All peripheral clocks disabled, AHB_CLK = 12 MHz; SLOW_CLK = 3 MHz, AHB_CLK from FRO-12M. LDO_CORE drive strenth is low. VDD_CORE (1.0 V)	25 °C	—	0.34	—	mA
		105 °C	—	0.60	—	mA
		125 °C	—	0.85	—	mA
IDD_DEEP_SLEEP_SD	Core in WFI; CPU_CLK = OFF, All peripheral clocks disabled, AHB_CLK = OFF; SLOW_CLK = OFF, FRO-12M disabled, all on-chip SRAM in deep sleep. LDO_CORE drive strenth is normal.VDD_CORE (1.1 V)	25 °C	—	242.05	—	µA
		105 °C	—	537.99	—	µA
		125 °C	—	800.22	—	µA
IDD_DEEP_SLEEP_MD1	Core in WFI; CPU_CLK = OFF, All peripheral clocks disabled, AHB_CLK = OFF; SLOW_CLK = OFF, FRO-12M disabled, all on-chip SRAM in deep sleep. LDO_CORE drive strenth is low. VDD_CORE (1.0 V)	25 °C	—	20.28	—	µA
		105 °C	—	251.85	—	µA
		125 °C	—	472.36	—	µA
IDD_DEEP_SLEEP_MD2	Core in WFI; CPU_CLK = OFF, All peripheral clocks disabled, AHB_CLK = OFF; SLOW_CLK = OFF, FRO-12M enabled. VDD_CORE (1.0 V).	25 °C	—	90.44	—	µA
		105 °C	—	320.75	—	µA
		125 °C	—	541.68	—	µA

Table continues on the next page...

Table 12. Power consumption operating behaviors (continued)

Symbol	Description	Condition[1]	Min	Typ	Max	Unit
IDD_POWER_DOWN	Core in WFI; CPU_CLK = OFF, all VDD_CORE domains power static, AHB_CLK = OFF; SLOW_CLK = OFF; FRO-16K disabled; Flash is OFF.	25 °C	—	6.47	—	µA
		105 °C	—	134.69	—	µA
		125 °C	—	267.54	—	µA
IDD_DEEP_POWER_DOWN_1	Core in WFI; CPU_CLK = OFF, all VDD_CORE domains power gated, AHB_CLK = OFF; SLOW_CLK = OFF; FRO-16K disabled. Wakeup timer is OFF. SRAM is OFF	25 °C	—	0.39	—	µA
		105 °C	—	3.66	—	µA
		125 °C	—	8.06	—	µA
IDD_DEEP_POWER_DOWN_2	Core in WFI; CPU_CLK = OFF, all VDD_CORE domains power gated, AHB_CLK = OFF; SLOW_CLK = OFF, FRO-16K enabled. Wakeup timer is ON. SRAM is OFF	25 °C	—	0.52	—	µA
		105 °C	—	3.78	—	µA
		125 °C	—	8.18	—	µA
IDD_DEEP_POWER_DOWN_3	Core in WFI; CPU_CLK = OFF, all VDD_CORE domains power gated, AHB_CLK = OFF; SLOW_CLK = OFF, FRO-16K enabled. Wakeup timer is ON. RAM A0 retained	25 °C	—	0.72	—	µA
		105 °C	—	6.47	—	µA
		125 °C	—	13.87	—	µA

1. Ambient Temperature
2. SD: standard drive, core voltage is 1.1V. MD: middle drive, core voltage is 1.0V

3.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

3.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

3.2.9 Capacitance attributes

Table 13. Capacitance attributes

Symbol	Description	Min	Typ	Max	Unit	Condition
CIN_A	Input capacitance: analog pins	—	—	7	pF	—
CIN_D	Input capacitance: digital pins	—	—	7	pF	—

3.3 Switching specifications

3.3.1 Device clock specs

Table 14. Device clock specs

Symbol	Description	Min	Typ	Max	Unit	Condition
fCPU	CPU clock (CPU_CLK)	—	—	96	MHz	Standard drive (SD) mode VDD_CORE = 1.1 V
fSYSTEM	SYSTEM clock (SYSTEM_CLK)	—	—	96	MHz	Standard drive (SD) mode VDD_CORE = 1.1 V
fSLOW	Slow clock (SLOW_CLK)	—	—	24	MHz	Standard drive (SD) mode VDD_CORE = 1.1 V
fCPU	CPU clock (CPU_CLK)	—	—	48	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSYSTEM	SYSTEM clock (SYSTEM_CLK)	—	—	48	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSLOW	Slow clock (SLOW_CLK)	—	—	12	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V

3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPI2C, LPI3C, LPSPI functions.

3.3.2.1 General switching specifications

NOTE

Refer to attached pinout spreadsheet.

Table 15. General switching specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path [1]	1.5	—	—	SYSTEM clock cycles	The synchronous and asynchronous timing must be met.
—	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	150	—	—	ns	—
—	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	—	ns	—

Table continues on the next page...

Table 15. General switching specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	External RST pin interrupt pulse width — Asynchronous path [2]	330	—	—	ns	This is the shortest pulse that is guaranteed to be recognized.
—	GPIO pin interrupt pulse width — Asynchronous path [2]	16	—	—	ns	—
—	Port rise/fall time for slow I/O pins [3,4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins [3,4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins [3,4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins [3,4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for medium I/O pins [5,6]	0.8	—	4	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for medium I/O pins [5,6]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for medium I/O pins [5,6]	0.8	—	4	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for medium I/O pins [5,6]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)

Table continues on the next page...

Table 15. General switching specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	HD pins [7]	2.2	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive, fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive (DSE = 0), fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	15	ns	2.7 ≤ VDD ≤ 3.6 V, Normal drive (DSE =0), slow slew rate (SRE = 1)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE=1), Fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE =1), Slow slew rate (SRE=1)
—	RST pins [4]	3	—	8	ns	2.7 ≤ VDD ≤ 3.6 V
—	RST pins [4]	3.6	—	20	ns	1.71 ≤ VDD < 2.7 V

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized
3. For the HD I/O pins, setting DSE1 = 1 will support the same rise/fall time at 4x the load capacitance. For the 5VTOL I/O pins, setting DSE1=1 will support the same fall time at 2x the load capacitance, but the rise time will increase due to the increased loading
4. Load is 25 pF.
5. Assumes default values in CALIB1 and CALIB0 in PORTS
6. 25 pF lumped load
7. Load is 25 pF for DSE=0. Load is 100 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].

3.4 Thermal specifications

3.4.1 Thermal operating requirements

Table 16. Thermal operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
TA	Ambient temperature [1]	-40	25	125	°C	—
TJ	Die junction temperature [2,3,4]	—	—	125	°C	—

1. The device may operate at maximum TA rating as long as TJ maximum of 125 °C is not exceeded. The simplest method to determine TJ is: TJ = TA + RθJA*chip power dissipation.
2. Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage Estimates application note (AN14194)
3. The device operating specification is not guaranteed beyond 125 °C TJ.

4. The maximum operating requirement applies to all chapters unless otherwise specifically stated.

3.4.2 Thermal attributes

Table 17. Thermal attributes

Rating	Board Type[1]	Symbol	HVQFN 32	HVQFN 48	LQFP 64	Unit
Junction to Ambient Thermal Resistance [2]	JESD51-7, 2s2p	$R_{\theta JA}$	37.4	35.0	55.9	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	JESD51-7, 2s2p	Ψ_{JT}	3.3	3.5	6.1	°C/W
Junction to Case Top Thermal Resistance	NA	$R_{\theta JCT}$	36.5[3]	23.7[3]	30.3[4]	°C/W
Junction to Case Bottom Thermal Resistance	NA	$R_{\theta JCB}$	7.6[5]	8.2[5]	24.5[5]	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-7)
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
3. Junction-to-Case top thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center
4. Junction-to-Case top thermal resistance determined using an isothermal cold plate.
5. Junction-to-Case (Bottom) thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center

4 Peripheral operating requirements and behaviors

4.1 Core modules

4.1.1 Debug trace operating behaviors

Table 18. Debug trace operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation	—	—	36	MHz	SD mode
—	Frequency of operation	—	—	25	MHz	MD mode
T1	Clock period	27.78	—	—	ns	SD mode
T1	Clock period	40	—	—	ns	MD mode
T2	Low pulse width	2	—	—	ns	—
T3	High pulse width	2	—	—	ns	—
T4	Clock and data rise time	—	—	3	ns	—
T5	Clock and data fall time	—	—	3	ns	—
T6	Data setup	1.5	—	—	ns	—
T7	Data hold	1.0	—	—	ns	—

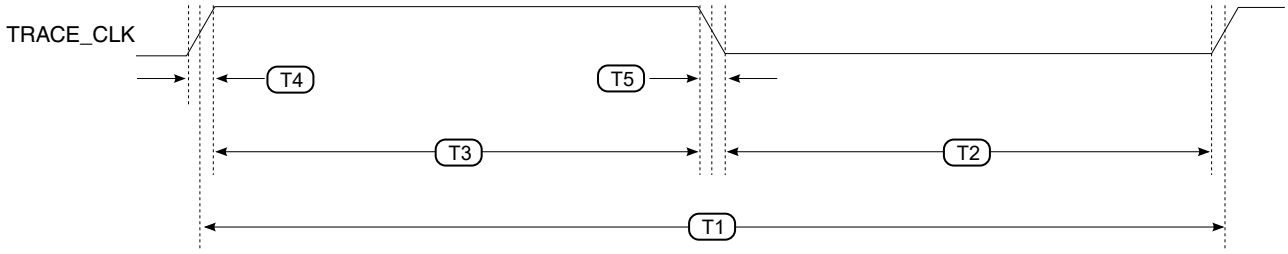


Figure 4. TRACE_CLKOUT specifications

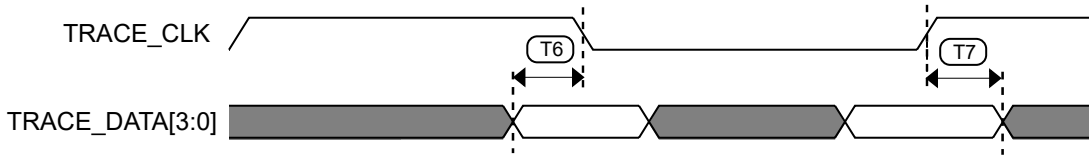


Figure 5. Trace data specifications

4.1.2 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 19. JTAG Debug Interface Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
J1	TCLK frequency of operation	—	—	25	MHz	Boundary Scan (SD mode)
J1	TCLK frequency of operation	—	—	12.5	MHz	Boundary Scan (MD mode)
J1	TCLK frequency of operation	—	—	25	—	JTAG-DP/TAP (SD mode)
J1	TCLK frequency of operation	—	—	12.5	—	JTAG-DP/TAP (MD mode)
J2	TCLK cycle period	1000/J1	—	—	ns	—
J3	TCLK clock pulse width	J2/2	—	—	ns	—
J4	TCLK rise and fall times	—	—	3	ns	—
J5	Boundary scan input data setup time to TCLK rise	8	—	—	ns	SD mode
J5	Boundary scan input data setup time to TCLK rise	16	—	—	ns	MD mode
J6	Boundary scan input data hold time after TCLK rise	-1	—	—	ns	SD mode

Table continues on the next page...

Table 19. JTAG Debug Interface Timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
J6	Boundary scan input data hold time after TCLK rise	-1	—	—	ns	MD mode
J7	TCLK low to boundary scan output data valid	—	—	18	ns	SD mode
J7	TCLK low to boundary scan output data valid	—	—	38	—	MD mode
J8	TCLK low to boundary scan output high-Z	—	—	18	ns	SD mode
J8	TCLK low to boundary scan output high-Z	—	—	38	—	MD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	8	—	—	ns	SD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	16	—	—	—	MD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	ns	SD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	—	MD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	18	—	SD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	38	ns	MD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	18	ns	SD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	38	—	MD mode

TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

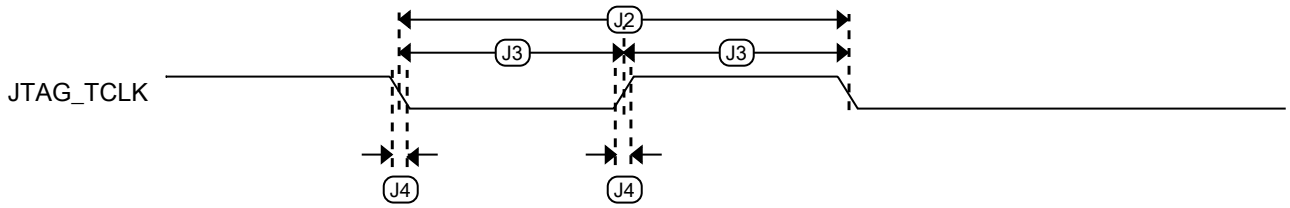


Figure 6. Test clock input timing

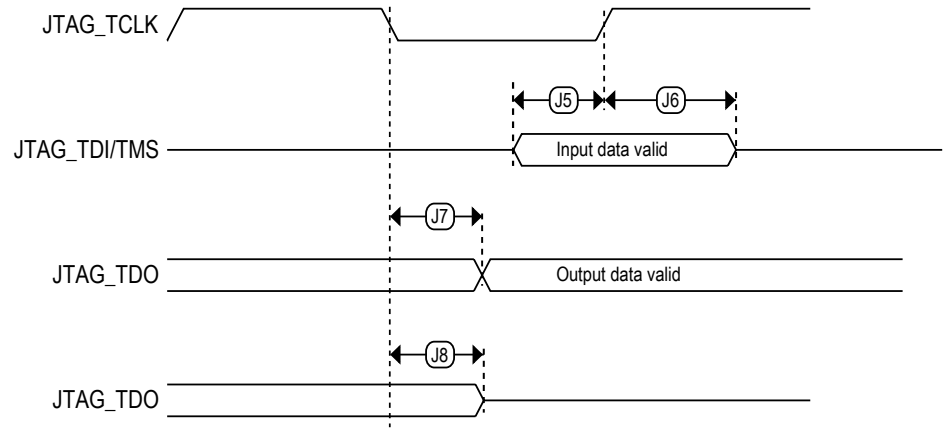


Figure 7. Boundary scan (JTAG) timing

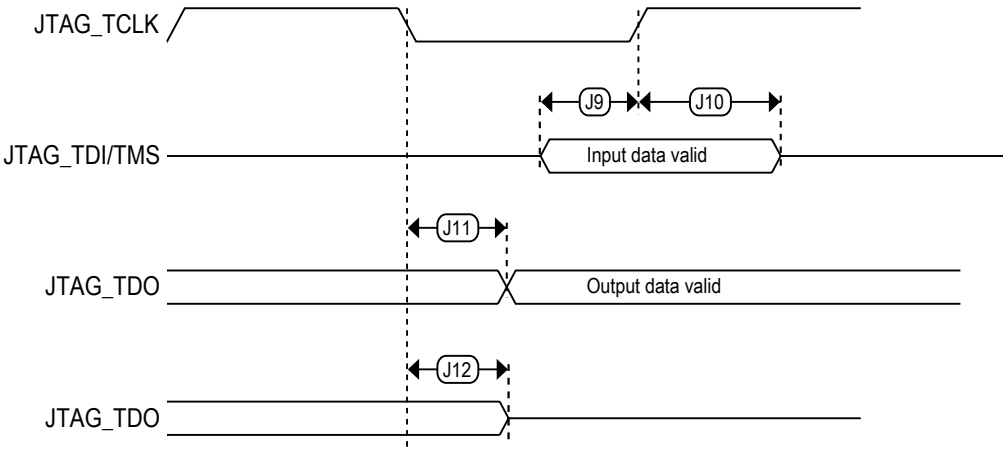


Figure 8. JTAG-DP/TAP timing

4.1.3 Serial Wire Debug (SWD) Timing

The following table gives the Serial Wire Debug specifications for the device.

Table 20. Serial Wire Debug (SWD) Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
S1	SWD_CLK frequency of operation	—	—	25	MHz	SD mode
S1	SWD_CLK frequency of operation	—	—	20	MHz	MD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	SD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	MD mode

Table continues on the next page...

Table 20. Serial Wire Debug (SWD) Timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
S3	SWD_CLK clock pulse width	20	—	—	ns	SD mode
S3	SWD_CLK clock pulse width	25	—	—	ns	MD mode
S4	SWD_CLK rise and fall times	—	—	3	ns	—
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	—	ns	SD mode
S5	SWD_DIO input data setup time to SWD_CLK rise	12.5	—	—	ns	MD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	SD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	MD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	25	ns	SD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	30	ns	MD mode
S8	SWD_CLK high to SWD_DIO high-Z	25	—	—	ns	SD mode
S8	SWD_CLK high to SWD_DIO high-Z	30	—	—	ns	MD mode

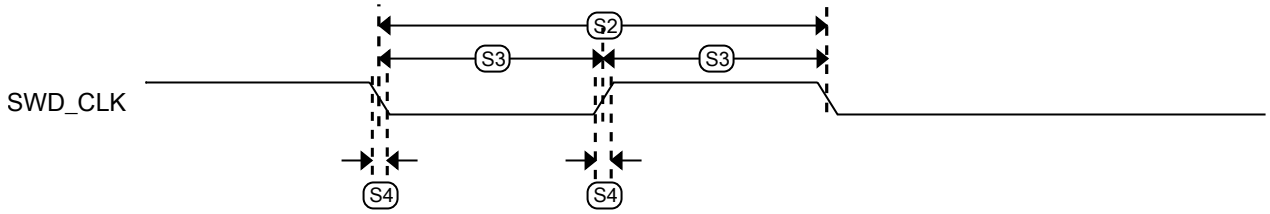


Figure 9. Serial Wire clock input timing

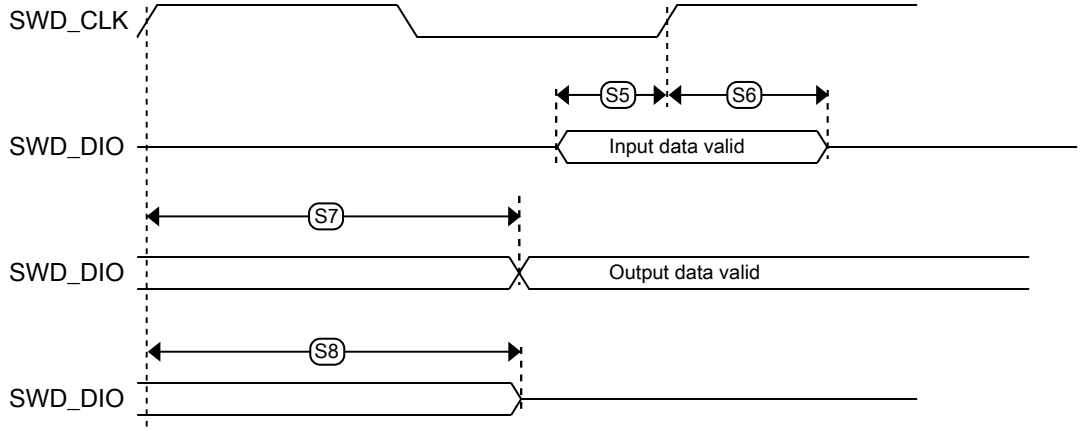


Figure 10. Serial Wire data timing

4.2 Clock modules

4.2.1 Reference Oscillator Specification

This chip is designed to meet targeted specifications with a ±40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

4.2.1.1 System Crystal Oscillator Specification

Table 21. System Crystal Oscillator Specification

Symbol	Description	Min	Typ	Max	Unit	Condition
fosc	Crystal Frequency	8	—	50	MHz	—
Tol	Frequency tolerance	—	±10	±40	ppm	—
Jitosc	Jitter	—	70	—	—	Period jitter (RMS)
Vpp	Peak-to-peak amplitude of oscillation [1]	—	0.6	—	V	—
fec	Externally provided input clock frequency [2]	0	—	50	MHz	—
tDC_EXTAL	External clock duty cycle	45	50	55	%	—
Vec	Externally provided input clock amplitude [2]	Refer to VIH and VIL specification	—	—	—	—

1. When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
2. This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.

4.2.1.2 System Oscillator Crystal Specifications.

Table 22. System Oscillator Crystal Specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
CP	Shunt Capacitance	—	1	2	pF	—
ESR	Crystal equivalent series resistance [1]	—	20	50	Ω	—
Cpara	Parasitic capacitance of EXTAL	—	—	8	pF	—
Cpara	Parasitic capacitance of XTAL	—	—	10	pF	—
Cm	Motional capacitance Cm	2.05	2.05	2.665	fF	—
Lm	Motional inductance Lm	7.7	—	—	mH	—
tstart	Crystal start-up time [2]	—	350	500	µs	—
IOSC	Current consumption	—	270	—	µA	Normal mode
IOSC	Current consumption	—	1	465	—	Sleep mode

1. Maximum crystal equivalent series resistance for 16 MHz is 80 ohms with 2 pF shunt capacitance.
2. Dependent on crystal specifications, proper PC board layout procedures must be followed to achieve specifications

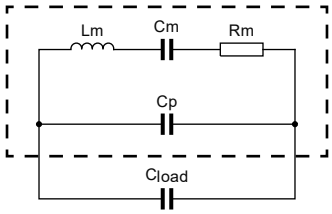


Figure 11. Crystal Electrical Block Diagram

4.2.1.3 System Oscillator Crystal Specifications

Table 23. System Oscillator Crystal Specifications.

Freq Crystal (MHz)	R_m(ohms)	C_p(pF)	C_{load}(pF)	C_m(pF)	L_m(mH)	Typical startup (µs)[1]	Typical Current consumption (µA)[1]	Drive level (µW)	
								min	max
8	100	5.00	18.0	0.008	49.47	1240	168	24	34
16	80	2.00	8.00	0.008	12.37	215	168.3	16	22
16	200	1.00	8.00	0.008	12.37	186	200.4	31	46
25	60	3.00	11.0	0.008	5.07	224	245.6	70	93
25	60	2.00	10.0	0.008	5.07	128	232.5	61	80
25	100	1.00	8.00	0.008	5.07	73.6	232.7	62	82
32	60	3.00	9.00	0.008	3.09	233	269.6	71	95
32	60	2.00	8.00	0.008	3.09	116	253.2	59	80
32	100	1.00	8.00	0.008	3.09	52.4	289.3	91	123
40	50	2.00	8.00	0.008	1.98	80.4	296.9	73	99
40	60	3.00	9.00	0.008	1.98	162	333.2	99	135
48	50	2.00	8.00	0.008	1.37	73.1	359.6	104	140
48	60	3.00	9.00	0.008	1.37	155	407.9	138	188

1. This is based on simulation

4.2.2 FRO-192M specifications

Table 24. FRO-192M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro192m	FRO-192M frequency (nominal)	—	192	—	MHz	—
Δffro192m	Frequency deviation (Ta = 0 °C – 85 °C)	—	—	±1.5	%	Open loop

Table continues on the next page...

Table 24. FRO-192M specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
Δffro192m	Frequency deviation (Ta = –40 °C – 125 °C)	—	—	±3	%	Open loop
Δffro192m	Frequency deviation (Ta = –40 °C – 125 °C)	—	—	±0.25	%	Closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	2	—	µs	Oscillation time with initial accuracy of -20 % to +2 % of enable signal assertion
tstartup	Start-up time	—	—	20	µs	Oscillation time within +/- 2 % from enable signal assertion
fos	Frequency overshoot during startup	—	—	2	%	—
jitper	Period jitter RMS [1]	—	70	—	ps	—
jitper	Accumulated jitter over 10K cycles [1]	—	800	—	ps	—
jitcyc	Cycle to cycle jitter [1]	—	100	—	ps	—
Ifro192m_vdd1p8	Current consumption for vdd1p8	—	70	—	µA	—
Ifro192m_vddlv	Current consumption for vddlv	—	35	—	µA	—

1. Tested at 96 MHz

4.2.3 FRO-12M specifications

Table 25. FRO-12M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro12m	FRO-12M frequency (nominal)	—	12	—	MHz	—
Δffro12m	Frequency deviation	—	—	±3	%	open loop
Δffro12m	Frequency deviation	—	—	±0.6	%	closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	5	—	µs	—
fos	Frequency overshoot during startup	—	10	20	%	—
Ifro12m	Current consumption	—	7	—	µA	—

4.2.4 FRO16K specifications

Table 26. FRO16K specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro16k	FRO16K frequency (nominal)	—	16.384	—	kHz	—
Δffro16k	Frequency deviation over –40 °C to 125 °C Ta	—	—	±6	%	open loop
TRIMstep	Trimming step	—	1.5	—	%	—
tstartup	Start-up time	—	310	—	µs	—
Ifro16k	Current consumption	—	50	—	nA	—

4.3 Memories and memory interfaces

4.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

4.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

4.3.1.1.1 Flash command time specifications

Table 27. Flash command time specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1all128k	Read 1s All execution time (128 KB)	—	—	940	µs	—
trd1blk128k	Read 1s Block execution time (128 KB)	—	—	750	µs	—
trd1scr	Read 1s Sector execution time [1]	—	—	50	µs	—
trd1pg	Read 1s Page execution time [1]	—	—	4.4	µs	—
trd1pglv	Read 1s Page at low voltage execution time [1]	—	—	5.8	µs	—
trd1phr	Read 1s Phrase execution time [1]	—	—	3.8	µs	—
trdphrlv	Read 1s Phrase at low voltage execution time [1]	—	—	4.8	—	—
trdmisr8k	Read into MISR (8 KB) [1]	—	—	50	µs	—
trdmisr128k	Read into MISR (128 KB) [1]	—	—	750	µs	—
trd1iscr	Read 1s IFR Sector execution time [1]	—	—	50	µs	—

Table continues on the next page...

Table 27. Flash command time specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1ipg	Read 1s IFR Page execution time [1]	—	—	4.4	µs	—
trdipglv	Read 1s IFR Page execution time at low voltage execution time [1]	—	—	5.8	µs	—
trd1iphr	Read 1s IFR Phrase execution time [1]	—	—	3.8	µs	—
trd1iphlv	Read 1s IFR Phrase execution time at low voltage execution time [1]	—	—	4.8	µs	—
trdimisr8k	Read IFR into MISR (8 KB) [1]	—	—	50	µs	—
trdimisrk32k	Read IFR into MISR (32 KB) [1]	—	—	190	µs	—
tpgmpg_initial	Program Page execution time at <1k cycles [2]	—	450	600	µs	—
tpgmpg_lifetime	Program Page execution time at >1k cycles [3]	—	450	750	µs	—
tpgmphr_initial	Program Phrase execution time at <1k cycles [2]	—	135	180	µs	—
tpgmphr_lifetime	Program Phrase execution time at >1k cycles [2]	—	135	225	µs	—
tersall128k	Erase All execution time (128 KB)	—	—	400	ms	—
tmasers128k	Mass Erase execution time (via sideband) (128 KB)	—	—	400	ms	—
terrscr	Erase Sector execution time [3]	—	2	22	ms	—

1. Time based on simulation
2. Based on simulation with 3 pulse programming for typ, 6 pulse programming for max.
3. Based on TSMC specification for erase sector time with no added time for verification and overhead.

4.3.1.2 Flash high voltage current behavior

Table 28. Flash high voltage current behavior

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_IO_PGM	Average current adder to VDD during flash programming operation [1]	—	—	6	mA	—
IDD_IO_ERS	Average current adder to VDD during flash erase operation [1]	—	—	4	mA	—

1. See the Power Management chapter in the reference manual for the specific VDD voltage supply powering the flash array.

4.3.1.3 Flash reliability specifications

Table 29. Flash reliability specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tnvmretp10k	Data retention after up to 10 K cycles	10	50	—	years	Program Flash	—
nnvmcycscr	Sector cycling endurance [1]	10 K	500 K	—	cycles	Program Flash	—
tnvmretp1k	Data retention after up to 1 K cycles	20	100	—	years	Program Flash	—
tnvmretp100k	Data retention after up to 100 K cycles	5	50	—	years	Program Flash	—
nnvmcyc256k	Sector cycling endurance for 256 KB [2]	100 K	500 K	—	cycles	Program Flash	—

1. Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40°C ≤ Tj ≤ 125°C.
2. For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

NOTE

Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.

4.4 Analog

4.4.1 ADC electrical specifications

4.4.1.1 ADC operating conditions

Table 30. ADC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDAD	Supply voltage	1.71	—	3.6	V	—
VSSAD	Ground voltage	-0.1	0	0.1	V	—
ΔVDD	— [1]	-0.1	0	0.1	V	—
ΔVSS	— [1]	0.1	0	0.1	V	—
VREFH	Reference Voltage High [2]	0.99	VDDAD	VDDAD	V	—
VREFL	Reference Voltage Low [3]	VSSAD	VSSAD	VSSAD	V	—
VADIN	Input Voltage [3,4,5]	VREFL	—	VREFH	V	—
FADCK	ADC conversion clock frequency	6	—	24	MHz	Low-power mode, PWRSEL=0

Table continues on the next page...

Table 30. ADC operating conditions (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
FADCK	ADC conversion clock frequency	6	—	60	MHz	Normal Mode, 16b, PWRSEL=1
FADCK	ADC conversion clock frequency	6	—	64	MHz	Normal Mode, 12b , PWRSEL=1
RAS	Analog source resistance (external) [6]	—	—	5	kΩ	—
RADIN	Input Resistance ADC channels 7:0 [7,8]	—	—	1.65	kΩ	VDDAD ≥ 1.71 V
RADIN	Input Resistance ADC channels 7:0 [7,8]	—	—	1.525	kΩ	VDDAD ≥ 2.1 V
RADIN	Input Resistance ADC channels 7:0 [7,8]	—	0.925	1.35	kΩ	VDDAD ≥ 2.5 V
CADIN	Input Capacitance	—	1.92	2.4	pF	—

1. DC potential difference
2. Minimum VDDAD/VREFH is 2.4 V in high-speed mode
3. For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
4. ADC selected inputs and unselected dedicated inputs must not exceed VDD_ANA during an ADC conversion. Unselected muxed inputs may exceed VDD_ANA but must not exceed the IO supply associated with the inputs (VDD) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
5. If VREFH is less than VDD_ANA, then voltage inputs greater than VREFH but less than VDD_ANA are allowed but result in a full-scale conversion result
6. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
7. If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type
8. There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual

4.4.1.2 I/O mux resistance table

Table 31. I/O mux resistance table

Symbol	Description	Min	Typ	Max	Unit	Condition
RIOMUX	I/O MUX Resistance	—	—	5.35	kΩ	VDD ≥ 1.71v
RIOMUX	I/O MUX Resistance	—	—	1	kΩ	VDD ≥ 2.1v
RIOMUX	I/O MUX Resistance	—	0.35	0.66	kΩ	VDD ≥ 2.5 v

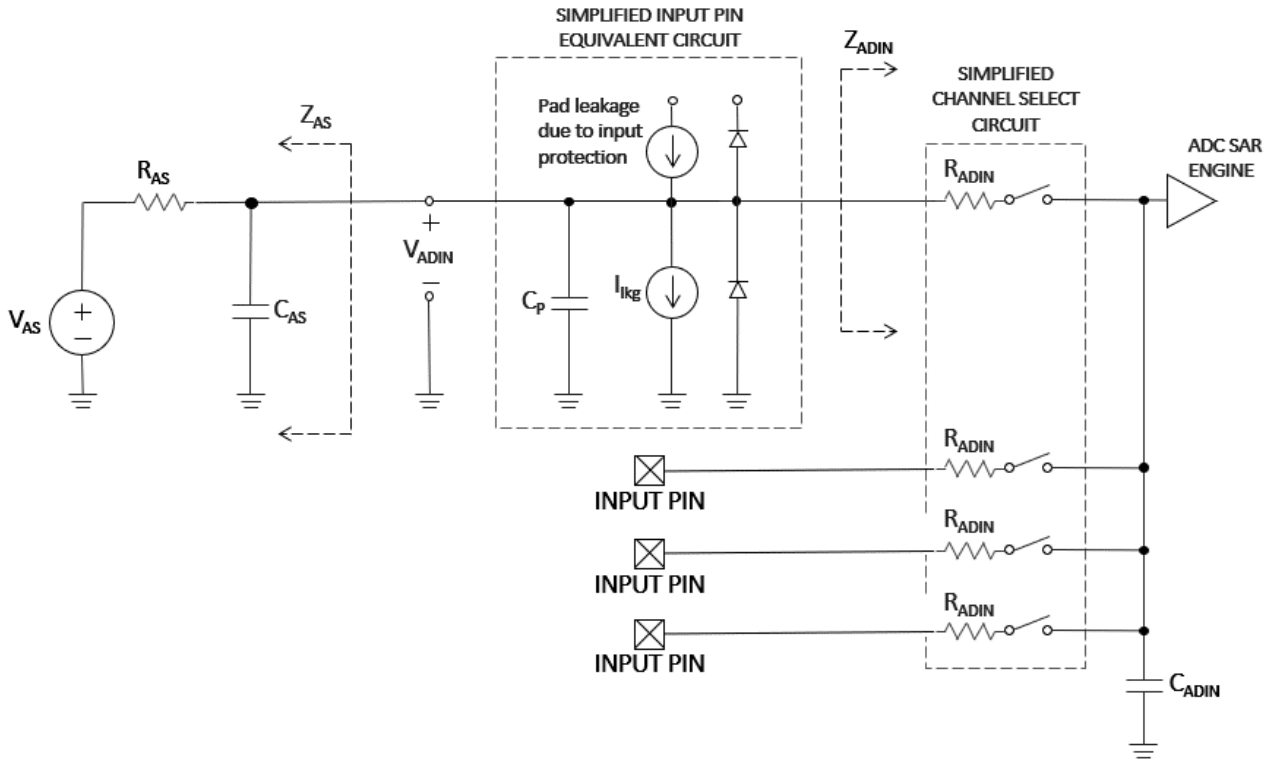


Figure 12. ADC input impedance equivalency diagram

4.4.1.3 ADC electrical characteristics

Table 32. ADC electrical characteristics

Symbol	Description	Min	Typ[1]	Max	Unit	Condition
—	Supply current [2]	—	7	—	—	PWREN=0, Conversions triggered at 10 kS/s
IDDAD	Supply current [2]	—	60	—	µA	PWREN=1, No Conversions
IDDAD	Supply current [2]	—	209	—	µA	Low-power mode, 6 MHz Clock, PWRSEL=0, 16b mode
IDDAD	Supply current [2]	—	272	—	µA	Low-power mode, 24 MHz clock, PWRSEL=0, 16b mode
IDDAD	Supply current [2]	—	708	—	µA	Normal Mode, 64 MHz, PWRSEL=1, 12b mode
IDDAD	Supply cuurent	—	806	—	µA	High Speed Mode, 64 MHz Clock,

Table continues on the next page...

Table 32. ADC electrical characteristics (continued)

Symbol	Description	Min	Typ[1]	Max	Unit	Condition
						PWRSEL=1, HS=1, 12b mode
IDDTS	Temp Sensor Supply Current	—	50	—	µA	Temperature Sensor Adder
CSMP	ADC Sample cycles [3]	3.5	—	131.5	cycles	Low-power mode and High speed mode
Fconv	ADC conversion rate [4]	—	—	4.0	MS/s	12b mode, (HS=1)
Fconv	ADC conversion rate [5]	—	—	3.2	MS/s	16b mode, (HS=1)
TSMP_REQ	Required Sample Time [6]	—	—	—	ns	Use equation based on RAS, RIOMUX, RADIN, CADIN, RAS, CAS, CP and desired accuracy (B)
TSMP	Sample Time [7]	145.8	TSMP_REQ	—	ns	Low-power mode
TSMP	Sample Time [8]	54.7	TSMP_REQ	—	ns	High-speed 16b mode
TSMP	Sample Time [9]	54.7	TSMP_REQ	—	ns	High-speed 12b mode
TSMPINT	Internal channel sample time inputs [10]	2.0	—	—	µs	—
DNL	Differential non-linearity [11,12]	—	±1	—	12b LSB	—
INL	Integral non-linearity [11,12]	—	±1	—	12b LSB	—
ZSE	Zero-scale error (V_ADIN = V_REFL) [11,12]	—	±1	—	12b LSB	—
FSE	Full-scale error (V_ADIN = V_REFH) [11,12]	—	±2	—	12b LSB	—
TUE	Total Unadjusted Error [11,12]	—	±3	—	12b LSB	—
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [12,13]	—	14.1	—	bits	25.2 kS/s (FADCK = 64 MHz, HS =1, AVGS=0111)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [12,13]	—	13.2	—	bits	200 kS/s (FADCK = 64 MHz, HS=1, AVGS =0100)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	12.6	—	bits	800 kS/s (FADCK = 64 MHz, HS=1, AVGS =0010)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	11.6	—	bits	3.2 MS/s (FADCK = 64 MHz, HS=1, AVGS =0000)

Table continues on the next page...

Table 32. ADC electrical characteristics (continued)

Symbol	Description	Min	Typ[1]	Max	Unit	Condition
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [12,13]	—	11.5	—	bits	1.0 MS/s (FADCK = 64 MHz, HS =1, AVGS=0010)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [12,13]	—	11.0	—	bits	4.0 MS/s (FADCK = 64 MHz, HS =1,AVGS=0000)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [12,13]	—	86.6	—	dB	25.2 kS/s (FADCK=64 MHz, HS=1, AVGS=0111)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [12,13]	—	81.2	—	dB	200 kS/s (FADCK=64 MHz, HS=1, AVGS=0100)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [12,13]	—	77.6	—	dB	800 kS/s (FADCK=64MHz, HS=1, AVGS=0010)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input	—	71.6	—	dB	3.2 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [12,13]	—	71.0	—	dB	1.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0010)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [12,13]	—	68.0	—	dB	4.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SFDR	Spurious free dynamic range [12,13]	—	88.0	—	dB	12b/16b Mode, 1kHz input, AVGS =0010
SFDR	Spurious free dynamic range [12,13]	—	82.0	—	dB	12b/16b Mode, 1kHz input, AVGS =0000
Tsu	Start-up time [14]	5	—	—	µs	—
E_TS	Temperature sensor error [15]	—	±1	±3	˚C	Tj=-40 to 105 ˚C
E_TS	Temperature sensor error [15]	—	±2	±4	˚C	Tj=-40 to 125 ˚C
A	Temp Sensor Slope Constant [16]	—	738	—	˚C	—
B	Temp Sensor Offset Constant [16]	—	287.5	—	˚C	—
α	Temp Sensor Bandgap Constant [16]	—	10.06	—	˚C	—

1. Typical values are for reference only and are not tested in production
2. The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 48 MHz. For lowest power operation, PWRSEL should be set to 00.
3. Must meet minimum TSMP requirement
4. fADCK=64 MHz (HS Mode)
5. fADCK=64 MHz (HS Mode)

6. Required sample time is dictated by external components RAS, CAS, internal components RADIN, CADIN, CP, and desired sample accuracy in bits (B). Calculate it with formula: TSMP_REQ = B*ln(2)*[RAS*(CAS+CP)+ (RAS + RIOMUX + RADIN)* CADIN(typ). RIOMUX=0 unless the ADC input channel goes through an analog mux in the IO”
7. Min based on 3.5 cycles
8. Min based on 3.5 cycles @ 64 MHz
9. Min based on 3.5 cycles @ 64 MHz
10. Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
11. 1 LSB = (VREFH - VREFL)/2N (N=14 bits), for 16- bit specifications, multiply by 4.
12. All accuracy numbers assume that the ADC is calibrated with VREFH=VDD_ANA and using a high- speed- dedicated input channel. Typical values assume VDD_ANA = 3.0 V, Temp = 25 °C, fADCK = 24 MHz, sample time of 3.5 ADCK cycles (CMDHn[STS]=0h) unless otherwise stated. Typical values are for reference only, and are not tested in production.
13. Dynamic results assume Fin=1 kHz sinewave, no averaging unless otherwise specified
14. Delay required if PWREN=0
15. The temperature sensor can be calibrated to a +/- 1 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber
16. T(°C) = A*[°α(Vbe8 - Vbe1)/(Vbe8 + α(Vbe8 - Vbe1))] - B where Vbe1 is the first value stored to FIFO as a result of the temperature sensor channel conversion, Vbe8 is the second value stored to FIFO as a result of the temperature sensor channel conversion, A is the slope factor, B is the offset factor, α is the bandgap coefficient

Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.

Ilkg = leakage current (Refer to pin leakage specification in the voltage and current operating behaviours of packaged device)

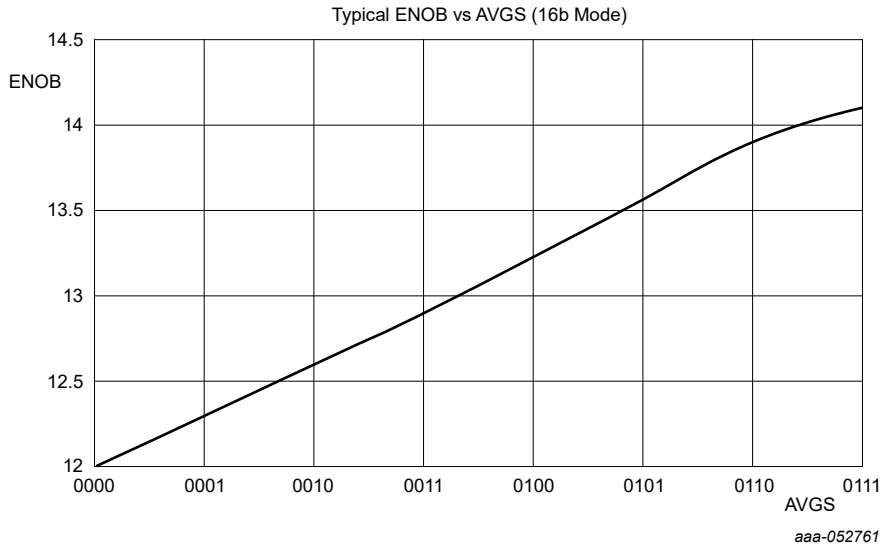


Figure 13. ENOB vs ADC (16b HS Mode)

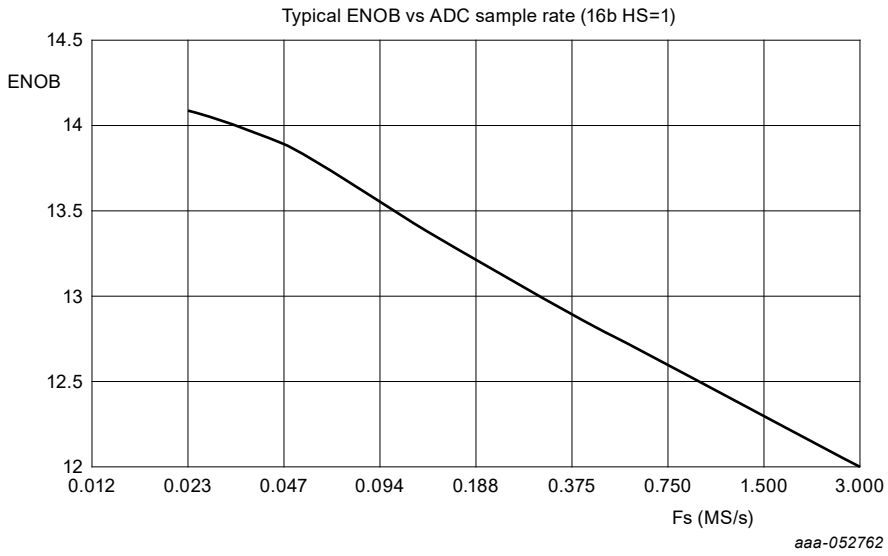


Figure 14. ENOB vs ADC sample rate

4.4.2 Comparator and 8-bit DAC electrical specifications

Table 33. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage	1.71	—	3.6	V	—
VREFH	8-bit DAC reference voltage high	0.97	—	VDD	V	—
IDD_CMP	Supply current	—	200	—	µA	High speed mode (EN=1, HPMD=1)
IDD_CMP	Supply current	—	10	—	µA	Normal mode (EN=1, HPMD=0, NPMD=0)
IDD_CMP	Supply current	—	400	—	nA	Low-power mode (EN=1, HPMD=0, NPMD=1)
VAIN	Analog input voltage	VSS	—	VDD	V	—
VAIO	Analog input offset voltage	—	—	20	mV	High speed mode
VAIO	Analog input offset voltage	—	—	20	mV	Normal mode
VAIO	Analog input offset voltage	—	—	40	mV	Low-power mode
VH	Analog comparator hysteresis [1]	—	0	—	mV	CR0[HYSTCTR] = 00
VH	Analog comparator hysteresis [1]	—	10	—	mV	CR0[HYSTCTR] = 01
VH	Analog comparator hysteresis [1]	—	20	—	mV	CR0[HYSTCTR] = 10
VH	Analog comparator hysteresis [1]	—	30	—	mV	CR0[HYSTCTR] = 11
VCMPOh	Output high	VDD - 0.2	—	—	V	—

Table continues on the next page...

Table 33. Comparator and 8-bit DAC electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
VCMPOI	Output low	—	—	0.2	V	—
tD	Propagation delay [2]	—	—	25	ns	High speed mode, 100 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	50	ns	High speed mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	600	ns	Normal mode, 30 mV overdrive, power > 1. 71V
tD	Propagation delay [2]	—	—	5	µs	Low-power mode, 30 mV overdrive, power > 1.71V
tinit	Analog comparator initialization delay [3]	—	—	40	µs	—
IDAC8b	8-bit DAC current adder (enabled)	—	10	—	µA	High power mode (EN=1, PMODE=1)
IDAC8b	8-bit DAC current consumption	—	1	—	µA	Low power mode (EN=1, PMODE=0)
INL	8-bit DAC integral non-linearity [4]	-1	—	+1.0	LSB	Low/High power mode, supply power > 1.71V
DNL	8-bit DAC differential non-linearity	-1	—	+1.0	LSB	Low/High power mode, power > 1.71V

1. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
2. Overdrive does not include input offset voltage or hysteresis. The propagation delay is defined as the time delay between the change of the voltage on input pin and the output change of the comparator analog part
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
4. 1 LSB = Vreference/256

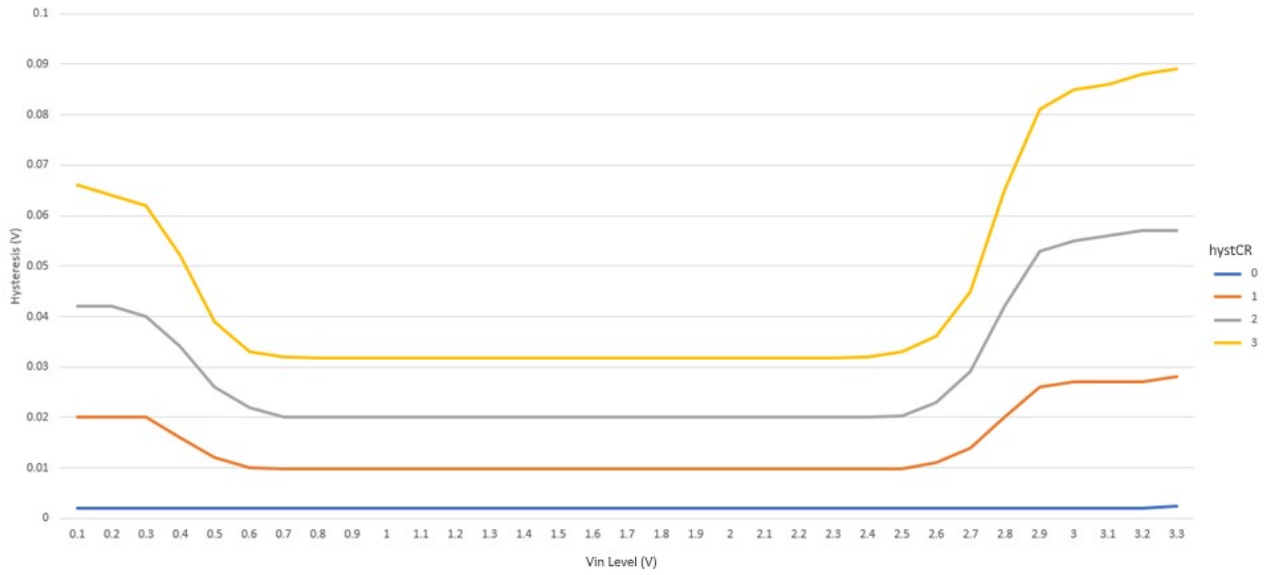


Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

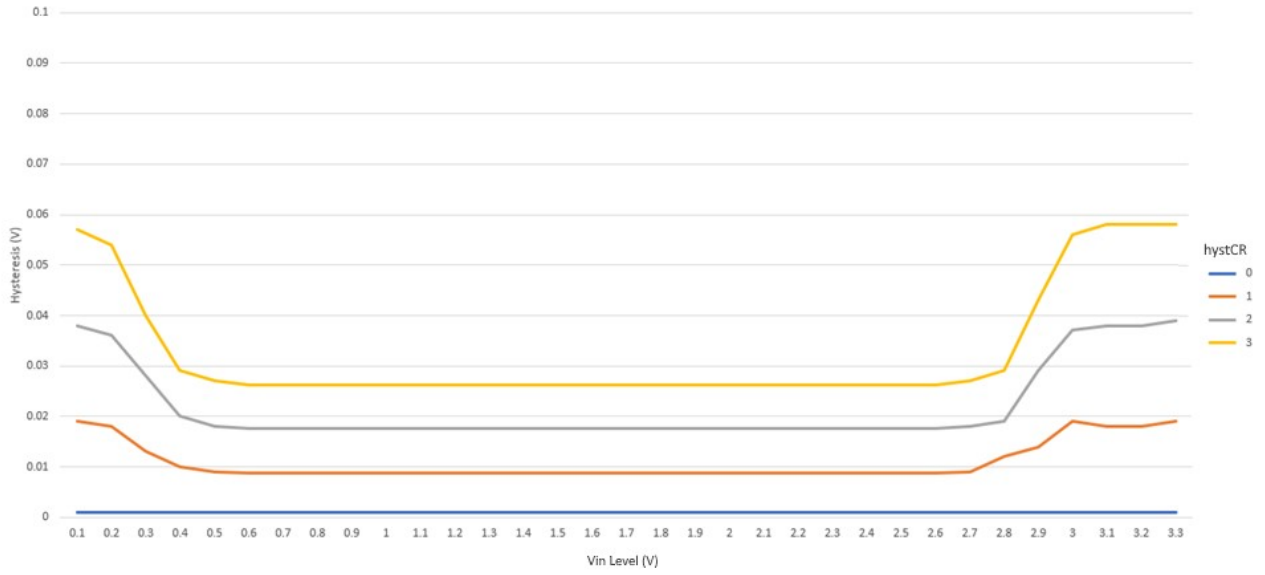


Figure 16. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

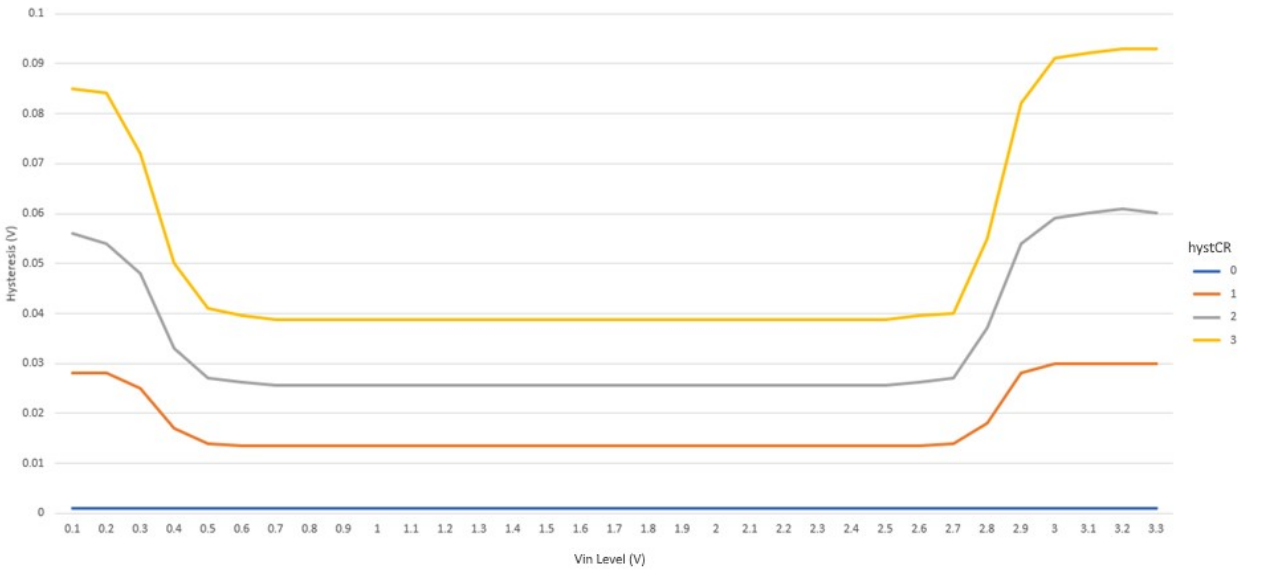


Figure 17. Typical hysteresis vs Vin level (VDD =3.3 V, HPMD = 0, NPMD = 1)

4.5 Timers

See General switching specifications.

4.6 Communication interfaces

4.6.1 LPUART

The Low Power Universal Asynchronous Receiver / Transmitter (LPUART) provides an asynchronous serial bus with master and slave operations, can reach to 24Mbps transfer rate, based on characterization but not covered by test limits in production.See General switching specifications.

4.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

4.6.2.1 LPSPI master mode timing

Table 34. LPSPI master mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation [1]	—	—	—	MHz	—
LP1	LPSPI0 ~ LPSPI1 medium speed pad	—	—	48	MHz	Master in SD mode

Table continues on the next page...

Table 34. LPSPI master mode timing (continued)

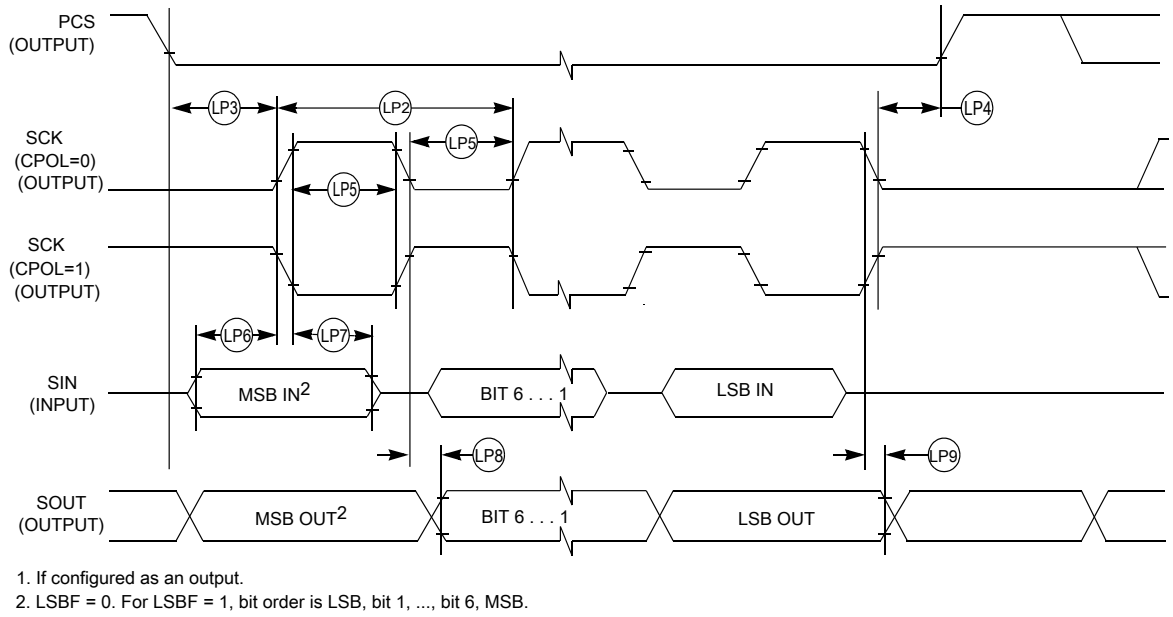
Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	LPSPI0 ~ LPSPI1 slow speed pad	—	—	24	MHz	Master in SD mode
LP1	LPSPI0 ~ LPSPI1 medium speed pad	—	—	24	MHz	Master in MD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad	—	—	24	MHz	Master in MD mode
LP2	SPSCK period	1000/LP1	—	—	ns	—
LP3	Enable lead time [2]	1/2	—	—	tperiph	—
LP4	Enable lag time [2]	1/2	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSCK/2-3	—	tSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	LPSPI0 ~ LPSPI1 medium speed pad	7.2	—	—	ns	Master in SD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad	14.4	—	—	ns	Master in SD mode
LP6	LPSPI0 ~ LPSPI1 medium speed pad	14.4	—	—	ns	Master in MD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad	14.4	—	—	ns	Master in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	LPSPI0 ~ LPSPI1 medium speed pad	0	—	—	ns	Master in SD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad	0	—	—	ns	Master in SD mode
LP7	LPSPI0 ~ LPSPI1 medium speed pad	0	—	—	ns	Master in MD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad	0	—	—	ns	Master in MD mode
LP8	Data valid (after SPSCK edge)	—	—	—	ns	—
LP8	LPSPI0 ~ LPSPI1 medium speed pad	—	—	7.2	ns	Master in SD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad	—	—	14.4	ns	Master in SD mode
LP8	LPSPI0 ~ LPSPI1 medium speed pad	—	—	14.4	ns	Master in MD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad	—	—	14.4	ns	Master in MD mode
LP9	Data hold time (outputs)	—	—	—	ns	—

Table continues on the next page...

Table 34. LPSPI master mode timing (continued)

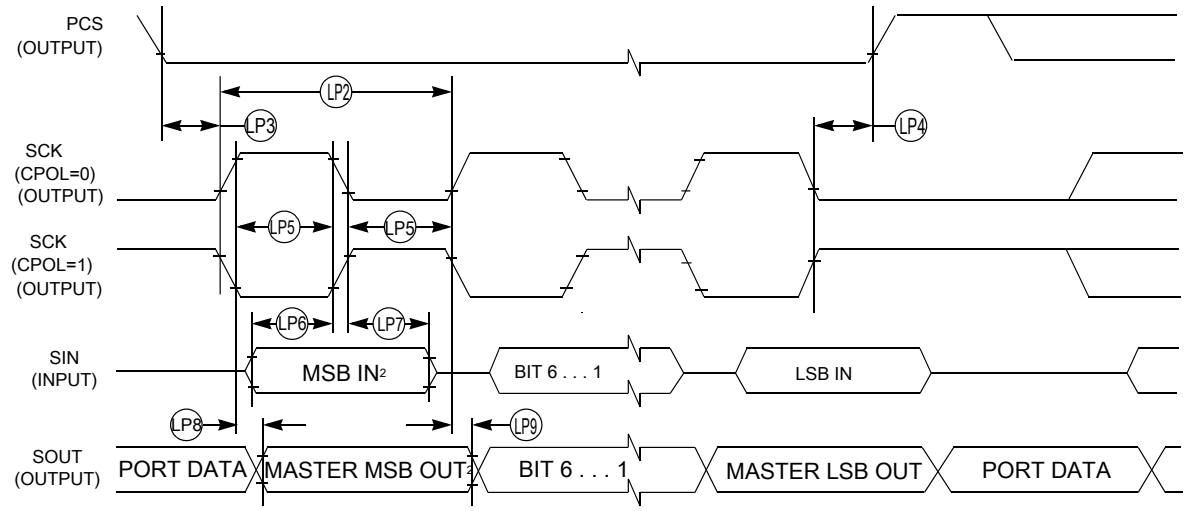
Symbol	Description	Min	Typ	Max	Unit	Condition
LP9	LPSPI0 ~ LPSPI1 medium speed pad	—	—	-1	ns	Master in SD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad	—	—	-1	ns	Master in SD mode
LP9	LPSPI0 ~ LPSPI1 medium speed pad	—	—	-1	ns	Master in MD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad	—	—	-1	ns	Master in MD mode

1. The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LPSPI peripheral functional clock.
2. tperiph = 1/fperiph



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI master mode timing (CPHA = 1)

4.6.2.2 LPSPI slave mode timing

Table 35. LPSPI slave mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation in OD mode [1]	—	—	—	—	—
LP1	lpspi0~lpspi1 medium speed pad [1]	—	—	24	MHz	Slave Tx in SD mode
LP1	lpspi0~lpspi1 slow speed pad [1]	—	—	12	MHz	Slave Tx in SD mode
LP1	lpspi0~lpspi1 medium speed pad [1]	—	—	48	MHz	Slave Rx in SD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	24	MHz	Slave Rx in SD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Slave Tx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Slave Tx in MD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Slave Rx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Slave Rx in MD mode
LP2	SPSCK period	4 x tperiph	—	2048 x tperiph	ns	—
LP3	Enable lead time [2]	1	—	—	tperiph	—
LP4	Enable lag time [2]	1	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSPSCK/ 2 - 5	—	tSPSCK/ 2	ns	—

Table continues on the next page...

Table 35. LPSPI slave mode timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	lpspi0~lpspi1 medium speed pad	3.6	—	—	ns	Slave Rx in SD mode
LP6	lpspi0~lpspi1 slow speed pad	7.2	—	—	ns	Slave Rx in SD mode
LP6	lpspi0~lpspi1 medium speed pad	14.4	—	—	ns	Slave Rx in MD mode
LP6	lpspi0~lpspi1 slow speed pad	14.4	—	—	ns	Slave Rx in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Slave Rx in SD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Slave Rx in SD mode
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Slave Rx in MD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Slave Rx in MD mode
LP8	Slave access time [2,3]	—	—	tperiph	ns	—
LP9	Slave MISO disable time [2,4]	—	—	tperiph	ns	—
LP10	Data valid (after SPSCK edge)	—	—	—	ns	—
LP10	lpspi0~lpspi1 medium speed pad	—	—	15.6	ns	Slave Tx in SD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	31.2	ns	Slave Tx in SD mode
LP10	lpspi0~lpspi1 medium speed pad	—	—	31.2	ns	Slave Tx in MD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	31.2	ns	Slave Tx in MD mode
LP11	Data hold time (outputs)	—	—	—	ns	—
LP11	lpspi0~lpspi1 medium speed pad	—	—	-1	ns	Slave Tx in SD mode
LP11	lpspi0~lpspi1 slow speed pad	—	—	-1	ns	Slave Tx in SD mode
LP11	lpspi0~lpspi1 medium speed pad	—	—	-1	ns	Slave Tx in MD mode
LP11	lpspi0~lpspi1 slow speed pad	—	—	-1	ns	Slave Tx in MD mode

1. The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/4, where fperiph is the LPSPI peripheral functional clock.
2. tperiph = 1/fperiph
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

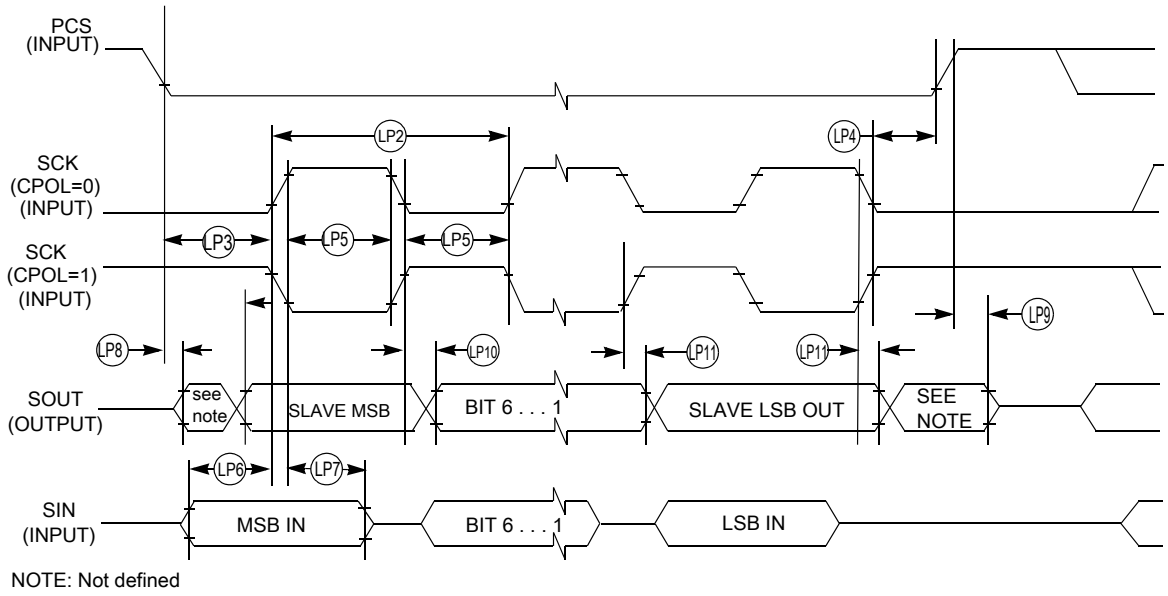


Figure 20. LPSPI slave mode timing (CPHA = 0)

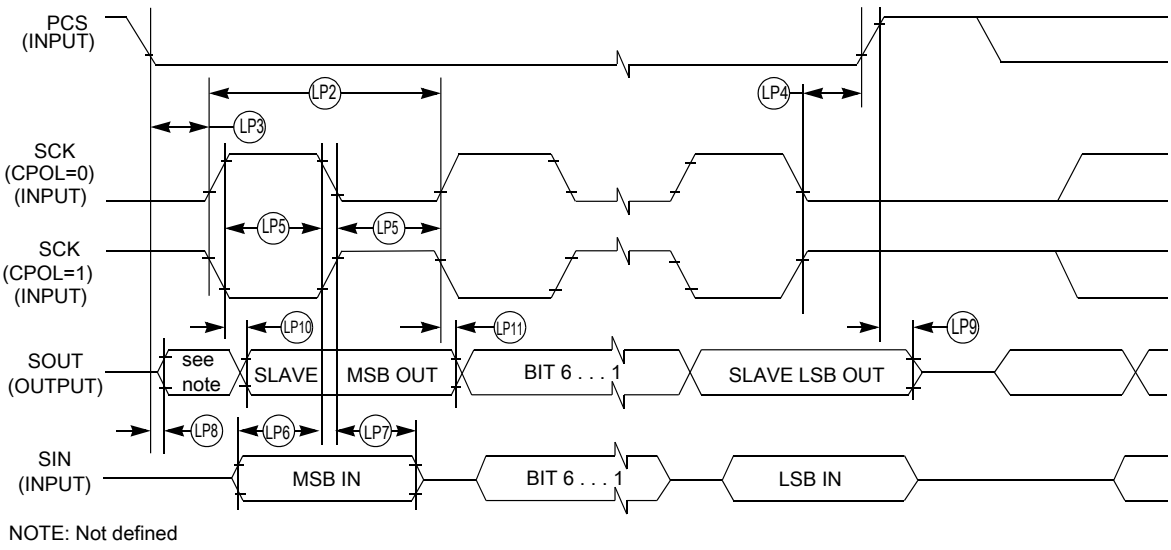


Figure 21. LPSPI slave mode timing (CPHA = 1)

4.6.3 LPI2C timing

Table 36. LPI2C timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency in standard mode	0	—	100	kHz	—
fSCL	SCL Clock Frequency in fast mode	0	—	400	kHz	—

Table continues on the next page...

Table 36. LPI2C timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in standard mode	4	—	—	µs	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in fast mode	0.6	—	—	µs	—
tLOW	LOW period of the SCL clock in standard mode	4.7	—	—	µs	—
tLOW	LOW period of the SCL clock in fast mode	1.25	—	—	µs	—
tHIGH	HIGH period of the SCL clock in standard mode	4	—	—	µs	—
tHIGH	HIGH period of the SCL clock in fast mode	0.6	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in standard mode	4.7	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in fast mode	0.6	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices in standard mode [1,2]	0	—	3.45	µs	—
tHD; DAT	Data hold time for I2C bus devices in fast mode [1,3]	0	—	0.9	µs	—
tSU; DAT	Data set-up time in standard mode [4]	250	—	—	ns	—
tSU; DAT	Data set-up time in fast mode [2,5]	100A	—	—	ns	—
tr	Rise time of SDA and SCL signals in standard mode [6]	—	—	1000	ns	—
tr	Rise time of SDA and SCL signals in fast mode [6]	20 +0.1Cb	—	300	ns	—
tf	Fall time of SDA and SCL signals in standard mode [5]	—	—	300	ns	—
tf	Fall time of SDA and SCL signals in fast mode [5]	20 +0.1Cb	—	300	ns	—
tSU; STO	Set-up time for STOP condition in standard mode	4	—	—	µs	—

Table continues on the next page...

Table 36. LPI2C timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tSU; STO	Set-up time for STOP condition in fast mode	0.6	—	—	µs	—
tBUF	Bus free time between STOP and START condition in standard mode	4.7	—	—	µs	—
tBUF	Bus free time between STOP and START condition in fast mode	1.3	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter in standard mode	N/A	—	N/A	ns	—
tSP	Pulse width of spikes that must be suppressed by the input filter in fast mode	0	—	50	ns	—

1. The master mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement tSU; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.
6. Cb = total capacitance of the one bus line in pF.

4.6.4 I2C 1 Mbps timing

Table 37. I2C 1 Mbps timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	1	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	HIGH period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices	0	—	—	µs	—
tSU; DAT	Data set-up time	50	—	—	ns	—
tr	Rise time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—

Table continues on the next page...

Table 37. I2C 1 Mbps timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tf	Fall time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tSU; STO	Set-up time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

1. Cb = total capacitance of the one bus line in pF for maximum value

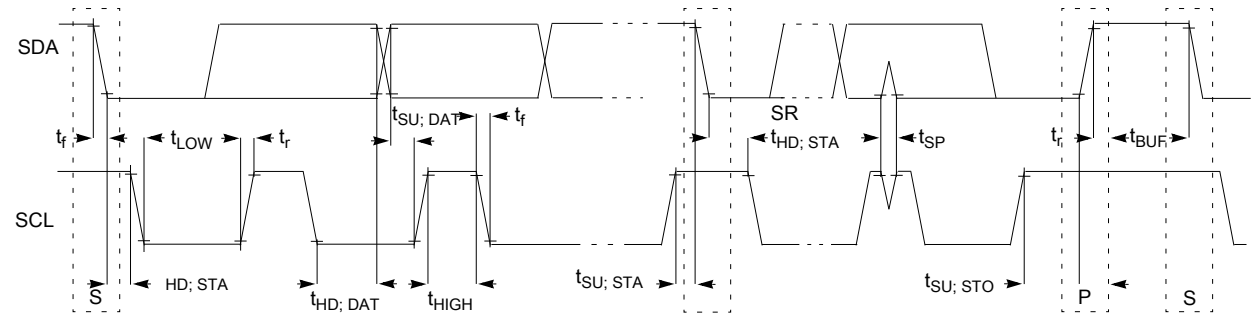


Figure 22. Timing definition for devices on the I2C bus

4.6.5 I2C HS mode timing

Table 38. I2C HS mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	3.4	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	High period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices [1]	0	—	—	µs	—
tSU; DAT	Data setup time	34	—	—	ns	—
tr	Rise time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—

Table continues on the next page...

Table 38. I2C HS mode timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tSU; STO	Setup time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

1. A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time in maximum value.
2. Cb = total capacitance of the one bus line in pF. The max Cb value is 50 pF. Applicable for maximum value.

NOTE

Only PTB4/5, PTA18/19, PTC0/1, PTC4/5 pin can support Fast+ (3 MHz) mode.

4.6.6 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pf, input transition of 1 ns. GPIO-Standard-plus pad configured with DSE = 1'b1 and GPIO-Medium pad with DSE = 1'b1 and SRE = 1'b1. SCL, SDA and PUR combination should be of same pad type. For e.g. I3C medium Data Pads to be used with I3C Medium Clock and PUR Pads Only. I3C Standard plus Data Pads to be used with I3C standard plus Clock and PUR pads only.

Table 39. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0.01	12.5	12.9	MHz	FSCL = 1 / (tDIG_L + tDIG_H)
tDIG_L	SCL Clock Low Period [1,2]	32	—	—	ns	—
tDIG_H	SCL Clock High Period [2]	32	—	—	ns	—
tSCO	Clock in to Data Out for Slave [3,4]	—	—	12	ns	—
tCR	SCL Clock Rise Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tCF	SCL Clock Fall Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Slave [6]	0	—	—	—	Applicable for slave and master loopback modes
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	N/A	ns	Applicable for slave and master loopback modes.

1. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.

2. tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
3. Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Master to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.
4. Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Master may be a Slave in a multi-Master system, and thus shall also adhere to this requirement
5. The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
6. tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Master mode vs. Slave mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

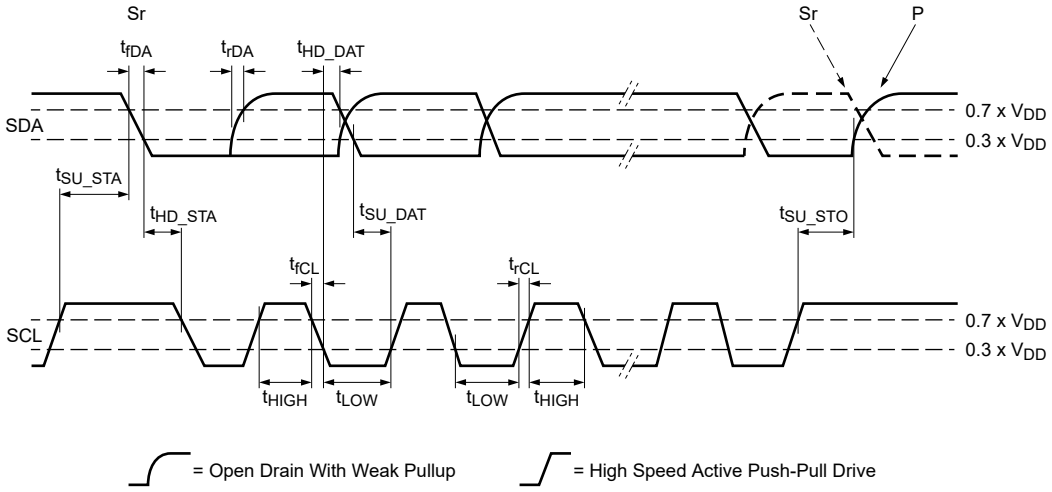


Figure 23. Legacy mode timing

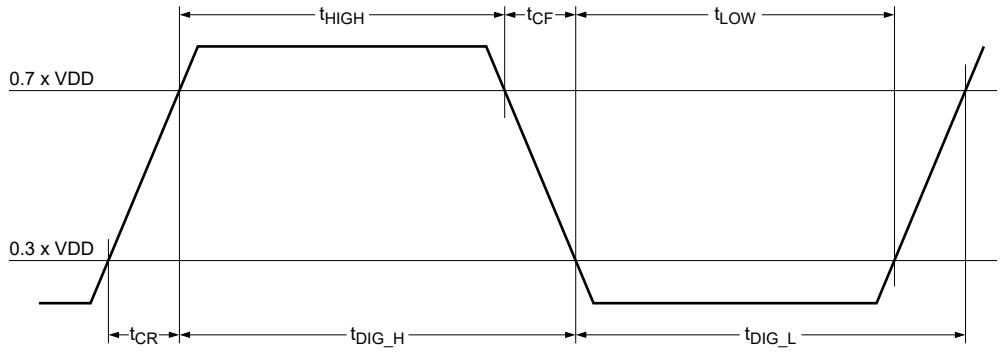


Figure 24. tDIG_H and tDIG_L

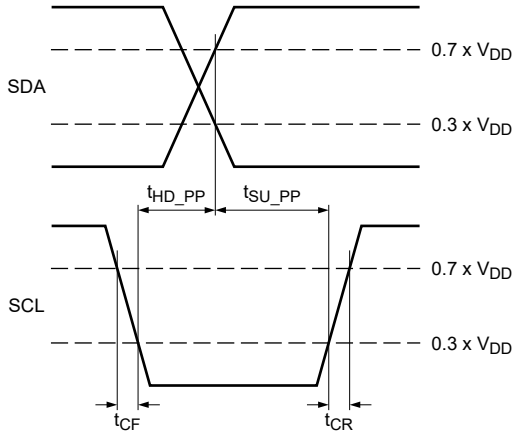


Figure 25. Master out timing

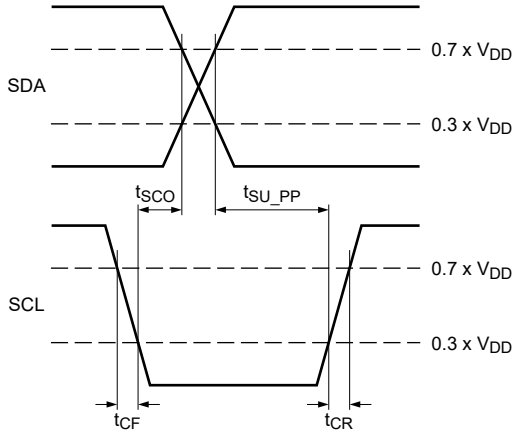


Figure 26. Slave out timing

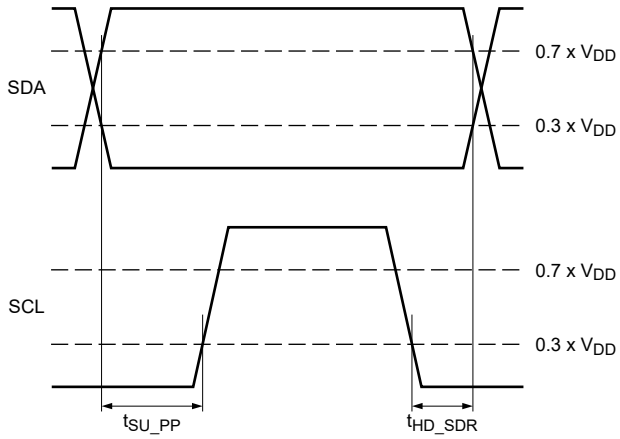


Figure 27. Master SDR timing

4.6.7 USB Full-speed device electrical specifications

This section describes the USB0 port Full Speed/Low Speed transceiver. The USB0 (FS/LS Transceiver) meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5 V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

This SoC does not have a dedicated pin to monitor the state of the USB VBUS signal. Please refer to the USBFS chapter in the Reference Manual for methods which can be used for VBUS Session_Valid detection with either a P4-12/ALT1 pin using an external resistive divider.

4.7 Human Machine Interface (HMI) modules

4.7.1 General Purpose Input/Output (GPIO)

See General switching specifications.

5 Package dimensions

5.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
LQFP 64	98ASS23234W
HVQFN 48	98ASA01637D
HVQFN 32	98ASA02110D

6 Pinout

6.1 MCXA153, A152, 143, A142, A133, A132 Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the "Pinout" tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, pinout table is also given below:

Table 40. Pin Assignments

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
P1_8	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_8 ALT2 - LPUART1_RXD ALT3 - LPI2C0_SDA ALT4 - CT_INP8 ALT5 - CT0_MAT2 ALT10 - I3C0_SDA	ISP - I2C_SDA VDD SYS - WUU0_IN10	IO Supply - VDD Pad type - HD+I3C Default - DIS
P1_9	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_9 ALT2 - LPUART1_TXD ALT3 - LPI2C0_SCL ALT4 - CT_INP9 ALT5 - CT0_MAT3 ALT10 - I3C0_SCL	ISP - I2C_SCL	IO Supply - VDD Pad type - HD Default - DIS
P1_10	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P1_10 ALT2 - LPUART1_RTS_B ALT3 - LPI2C0_SDAS ALT4 - CT2_MAT0	ANALOG - ADC0_A8	IO Supply - VDD Pad type - SLOW Default - DIS
P1_11	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P1_11 ALT1 - TRIG_OUT2 ALT2 - LPUART1_CTS_B ALT3 - LPI2C0_SCLS ALT4 - CT2_MAT1 ALT10 - I3C0_PUR	ANALOG - ADC0_A9 VDD SYS - WUU0_IN11	IO Supply - VDD Pad type - SLOW Default - DIS
P1_12	MCXA14x15x_LQFP64	ALT0 - P1_12 ALT3 - LPUART2_RXD ALT4 - CT2_MAT2	ANALOG - ADC0_A10 VDD SYS - WUU0_IN12	IO Supply - VDD Pad type - SLOW Default - DIS
P1_13	MCXA14x15x_LQFP64	ALT0 - P1_13 ALT1 - TRIG_IN3 ALT3 - LPUART2_TXD ALT4 - CT2_MAT3	ANALOG - ADC0_A11	IO Supply - VDD Pad type - SLOW Default - DIS
P1_29	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_29 ALT1 - RESET_B ALT2 - SPC_LPREQ	VDD SYS - RESET_B	IO Supply - VDD Pad type - RST Default - ALT1
P1_30	MCXA14x15x_LQFP64 MCXA14x15x_QFN48	ALT0 - P1_30 ALT1 - TRIG_OUT3	ANALOG - XTAL48M	IO Supply - VDD Pad type - HD+I3C

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT3 - LPI2C0_SDA ALT4 - CT_INP16 ALT10 - I3C0_SDA		Default - DIS
P1_31	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_31 ALT1 - TRIG_IN4 ALT3 - LPI2C0_SCL ALT4 - CT_INP17 ALT10 - I3C0_SCL	ANALOG - EXTAL48M	IO Supply - VDD Pad type - HD Default - DIS
VSS	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32			IO Supply - VDD
VDD_ANA	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32			IO Supply - VDD
VDD	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32			IO Supply - VDD
P2_0	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P2_0 ALT1 - TRIG_IN6 ALT2 - LPUART0_RXD ALT4 - CT_INP16 ALT5 - CT2_MAT0	ANALOG - ADC0_A0 VDD SYS - WUU0_IN18	IO Supply - VDD Pad type - SLOW Default - DIS
P2_1	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P2_1 ALT1 - TRIG_IN7 ALT2 - LPUART0_TXD ALT4 - CT_INP17 ALT5 - CT2_MAT1	ANALOG - ADC0_A1	IO Supply - VDD Pad type - SLOW Default - DIS
P2_2	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P2_2 ALT1 - TRIG_IN6 ALT2 - LPUART0_RTS_B	ANALOG - ADC0_A4/CMP0_IN0	IO Supply - VDD Pad type - SLOW Default - DIS

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA14x15x_QFN32 MCXA13x_QFN32	ALT3 - LPUART2_TXD ALT4 - CT_INP12 ALT5 - CT2_MAT2		
P2_3	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P2_3 ALT1 - TRIG_IN7 ALT2 - LPUART0_CTS_B ALT3 - LPUART2_RXD ALT4 - CT_INP13 ALT5 - CT2_MAT3	ANALOG - ADC0_A2/CMP1_IN0 VDD SYS - WUU0_IN19	IO Supply - VDD Pad type - SLOW Default - DIS
P2_4	MCXA14x15x_LQFP64	ALT0 - P2_4 ALT4 - CT_INP14 ALT5 - CT1_MAT0		IO Supply - VDD Pad type - SLOW Default - DIS
P2_5	MCXA14x15x_LQFP64	ALT0 - P2_5 ALT4 - CT_INP15 ALT5 - CT1_MAT1		IO Supply - VDD Pad type - SLOW Default - DIS
P2_6	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P2_6 ALT1 - TRIG_OUT4 ALT2 - LPSPI1_PCS1 ALT4 - CT_INP18 ALT5 - CT1_MAT2	ANALOG - ADC0_A3	IO Supply - VDD Pad type - SLOW Default - DIS
P2_7	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P2_7 ALT1 - TRIG_IN5 ALT4 - CT_INP19 ALT5 - CT1_MAT3	ANALOG - VREFI/ADC0_A7	IO Supply - VDD Pad type - SLOW Default - DIS
P2_12	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P2_12 ALT1 - USB0_VBUS_DET ALT2 - LPSPI1_SCK ALT3 - LPUART1_RXD ALT5 - CT0_MAT0	ISP - USB0_VBUS_DET ANALOG - ADC0_A5 VDD SYS - WUU0_IN20	IO Supply - VDD Pad type - SLOW Default - DIS
P2_13	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA13x_QFN32	ALT0 - P2_13 ALT1 - TRIG_IN8 ALT2 - LPSPI1_SDO ALT3 - LPUART1_TXD ALT5 - CT0_MAT1		IO Supply - VDD Pad type - SLOW Default - DIS
P2_16	MCXA14x15x_LQFP64	ALT0 - P2_16	ANALOG - ADC0_A6	IO Supply - VDD

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA13x_QFN32	ALT2 - LPSPI1_SDI ALT3 - LPUART1_RTS_B ALT5 - CT0_MAT2		Pad type - SLOW Default - DIS
	MCXA13x_QFN48 MCXA13x_QFN32	ALT0 - P2_17 ALT1 - TRIG_IN9 ALT2 - LPSPI1_PCS0 ALT3 - LPUART1_CTS_B ALT5 - CT0_MAT3		IO Supply - VDD Pad type - SLOW Default - DIS
	MCXA13x_QFN48	ALT0 - P2_20 ALT1 - TRIG_IN8 ALT2 - LPSPI1_PCS2 ALT4 - CT2_MAT0		IO Supply - VDD Pad type - SLOW Default - DIS
	MCXA13x_QFN48	ALT0 - P2_21 ALT1 - TRIG_IN9 ALT2 - LPSPI1_PCS3 ALT4 - CT2_MAT1		IO Supply - VDD Pad type - SLOW Default - DIS
VDD_USB	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA14x15x_QFN32			IO Supply - VDD_USB
USB0_DM	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA14x15x_QFN32		ANALOG - USB0_DM VDD SYS - WUU0_IN28	IO Supply - VDD_USB Pad type - ANA
USB0_DP	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA14x15x_QFN32		ANALOG - USB0_DP VDD SYS - WUU0_IN29	IO Supply - VDD_USB Pad type - ANA
VSS	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32			IO Supply - VDD
VDD	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48			IO Supply - VDD
P3_31	MCXA14x15x_LQFP64 MCXA14x15x_QFN48	ALT0 - P3_31 ALT1 - TRIG_IN10	ANALOG - ADC0_A12 VDD SYS - LPTMR0_ALT2	IO Supply - VDD Pad type - SLOW

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA13x_QFN48	ALT4 - CT0_MAT3		Default - DIS
P3_30	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P3_30 ALT1 - TRIG_OUT6 ALT4 - CT0_MAT2	ANALOG - ADC0_A13	IO Supply - VDD Pad type - SLOW Default - DIS
P3_29	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_29 ALT1 - ISPMODE_N ALT4 - CT_INP3	ISP - ISPMODE_N ANALOG - ADC0_A14 VDD SYS - WUU0_IN27	IO Supply - VDD Pad type - SLOW Default - ALT1
P3_28	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_28 ALT1 - TRIG_IN11 ALT2 - LPI2C0_SDA ALT4 - CT_INP12	VDD SYS - WUU0_IN26	IO Supply - VDD Pad type - 5VTOL Default - DIS
P3_27	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_27 ALT1 - TRIG_OUT7 ALT2 - LPI2C0_SCL ALT4 - CT_INP13		IO Supply - VDD Pad type - 5VTOL Default - DIS
P3_15	MCXA14x15x_LQFP64	ALT0 - P3_15 ALT2 - LPUART2_TXD ALT4 - CT_INP7		IO Supply - VDD Pad type - SLOW Default - DIS
P3_14	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P3_14 ALT2 - LPUART2_RXD ALT4 - CT_INP6 ALT5 - PWM0_X2	VDD SYS - WUU0_IN25	IO Supply - VDD Pad type - SLOW Default - DIS
P3_13	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P3_13 ALT2 - LPUART2_CTS_B ALT4 - CT1_MAT3 ALT5 - PWM0_X1		IO Supply - VDD Pad type - SLOW Default - DIS
P3_12	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P3_12 ALT2 - LPUART2_RTS_B ALT4 - CT1_MAT2 ALT5 - PWM0_X0		IO Supply - VDD Pad type - SLOW Default - DIS
P3_11	MCXA14x15x_LQFP64	ALT0 - P3_11	VDD SYS - WUU0_IN24	IO Supply - VDD

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT1 - TRIG_IN6 ALT2 - LPSPI1_PCS0 ALT3 - LPUART1_CTS_B ALT4 - CT1_MAT1 ALT5 - PWM0_B2		Pad type - MED Default - DIS
P3_10	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_10 ALT1 - TRIG_IN5 ALT2 - LPSPI1_SCK ALT3 - LPUART1_RTS_B ALT4 - CT1_MAT0 ALT5 - PWM0_A2		IO Supply - VDD Pad type - MED Default - DIS
P3_9	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_9 ALT1 - TRIG_IN4 ALT2 - LPSPI1_SDI ALT3 - LPUART1_TXD ALT4 - CT_INP5 ALT5 - PWM0_B1		IO Supply - VDD Pad type - MED Default - DIS
P3_8	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_8 ALT1 - TRIG_IN3 ALT2 - LPSPI1_SDO ALT3 - LPUART1_RXD ALT4 - CT_INP4 ALT5 - PWM0_A1 ALT12 - CLKOUT	VDD SYS - WUU0_IN23	IO Supply - VDD Pad type - MED Default - DIS
P3_7	MCXA14x15x_LQFP64	ALT0 - P3_7 ALT1 - TRIG_IN2 ALT2 - LPSPI1_PCS2 ALT5 - PWM0_B0		IO Supply - VDD Pad type - MED Default - DIS
P3_6	MCXA14x15x_LQFP64	ALT0 - P3_6 ALT1 - CLKOUT ALT2 - LPSPI1_PCS3 ALT5 - PWM0_A0 ALT12 - FREQME_CLK_OUT1		IO Supply - VDD Pad type - MED Default - DIS
P3_1	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P3_1 ALT1 - TRIG_IN1 ALT4 - CT_INP17		IO Supply - VDD Pad type - HD Default - DIS

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA14x15x_QFN32 MCXA13x_QFN32	ALT5 - PWM0_B0 ALT12 - FREQME_CLK_OUT0		
P3_0	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P3_0 ALT1 - TRIG_IN0 ALT4 - CT_INP16 ALT5 - PWM0_A0	VDD SYS - WUU0_IN22	IO Supply - VDD Pad type - HD Default - DIS
VSS	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32			IO Supply - VDD
VDD	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32			IO Supply - VDD
P0_0	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P0_0 ALT1 - TMS/SWDIO ALT2 - LPUART0_RTS_B ALT3 - LPSPI0_PCS0 ALT4 - CT_INP0		IO Supply - VDD Pad type - SLOW Default - ALT1
P0_1	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P0_1 ALT1 - TCLK/SWCLK ALT2 - LPUART0_CTS_B ALT3 - LPSPI0_SDI ALT4 - CT_INP1		IO Supply - VDD Pad type - SLOW Default - ALT1
P0_2	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P0_2 ALT1 - TDO/SWO ALT2 - LPUART0_RXD ALT3 - LPSPI0_SCK ALT4 - CT0_MAT0 ALT5 - UTICK_CAP0 ALT10 - I3C0_PUR	ISP - UART_RXD	IO Supply - VDD Pad type - SLOW Default - ALT1
P0_3	MCXA14x15x_LQFP64 MCXA14x15x_QFN48	ALT0 - P0_3 ALT1 - TDI	ISP - UART_TXD ANALOG - CMP1_IN1	IO Supply - VDD Pad type - SLOW

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT2 - LPUART0_TXD ALT3 - LPSPI0_SDO ALT4 - CT0_MAT1 ALT5 - UTICK_CAP1 ALT8 - CMP0_OUT		Default - ALT1
P0_6	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P0_6 ALT2 - LPI2C0_HREQ ALT3 - LPSPI0_PCS1 ALT4 - CT_INP2 ALT8 - CMP1_OUT ALT12 - CLKOUT	ANALOG - ADC0_A15	IO Supply - VDD Pad type - SLOW Default - DIS
P0_16	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P0_16 ALT2 - LPI2C0_SDA ALT3 - LPSPI0_PCS2 ALT4 - CT0_MAT0 ALT5 - UTICK_CAP2 ALT10 - I3C0_SDA	VDD SYS - WUU0_IN2	IO Supply - VDD Pad type - HD+I3C Default - DIS
P0_17	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48	ALT0 - P0_17 ALT2 - LPI2C0_SCL ALT3 - LPSPI0_PCS3 ALT4 - CT0_MAT1 ALT5 - UTICK_CAP3 ALT10 - I3C0_SCL		IO Supply - VDD Pad type - HD Default - DIS
P1_0	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_0 ALT1 - TRIG_IN0 ALT2 - LPSPI0_SDO ALT3 - LPI2C0_SDA ALT4 - CT_INP4 ALT5 - CT0_MAT2	ISP - SPI_SDO ANALOG - ADC0_A16/CMP0_IN3 VDD SYS - WUU0_IN6/LPTMR0_ALT3	IO Supply - VDD Pad type - MED+I2C_FILT Default - DIS
P1_1	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_1 ALT1 - TRIG_IN1 ALT2 - LPSPI0_SCK ALT3 - LPI2C0_SCL ALT4 - CT_INP5 ALT5 - CT0_MAT3	ISP - SPI_SCK ANALOG - ADC0_A17/CMP1_IN3	IO Supply - VDD Pad type - MED+I2C_FILT Default - DIS
P1_2	MCXA14x15x_LQFP64	ALT0 - P1_2	ISP - SPI_SDI	IO Supply - VDD

Table continues on the next page...

Table 40. Pin Assignments (continued)

Pin Name	Package	Pinmux Assignment	Alternate Function	Pad Settings
	MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT1 - TRIG_OUT0 ALT2 - LPSPI0_SDI ALT3 - LPI2C0_SDAS ALT4 - CT1_MAT0 ALT5 - CT_INP0	ANALOG - ADC0_A18	Pad type - MED Default - DIS
P1_3	MCXA14x15x_LQFP64 MCXA14x15x_QFN48 MCXA13x_QFN48 MCXA14x15x_QFN32 MCXA13x_QFN32	ALT0 - P1_3 ALT1 - TRIG_OUT1 ALT2 - LPSPI0_PCS0 ALT3 - LPI2C0_SCLS ALT4 - CT1_MAT1 ALT5 - CT_INP1	ISP - SPI_PCS ANALOG - ADC0_A19/CMP0_IN1 VDD SYS - WUU0_IN7	IO Supply - VDD Pad type - MED Default - DIS
VDD	MCXA14x15x_LQFP64			IO Supply - VDD
VSS	MCXA14x15x_LQFP64			IO Supply - VDD
P1_4	MCXA14x15x_LQFP64	ALT0 - P1_4 ALT1 - FREQME_CLK_IN0 ALT2 - LPSPI0_PCS3 ALT3 - LPUART2_RXD ALT4 - CT1_MAT2	ANALOG - ADC0_A20/CMP0_IN2 VDD SYS - WUU0_IN8	IO Supply - VDD Pad type - MED Default - DIS
P1_5	MCXA14x15x_LQFP64	ALT0 - P1_5 ALT1 - FREQME_CLK_IN1 ALT2 - LPSPI0_PCS2 ALT3 - LPUART2_TXD ALT4 - CT1_MAT3	ANALOG - ADC0_A21/CMP1_IN2	IO Supply - VDD Pad type - MED Default - DIS
P1_6	MCXA14x15x_LQFP64	ALT0 - P1_6 ALT1 - TRIG_IN2 ALT2 - LPSPI0_PCS1 ALT3 - LPUART2_RTS_B ALT4 - CT_INP6	ANALOG - ADC0_A22	IO Supply - VDD Pad type - MED Default - DIS
P1_7	MCXA14x15x_LQFP64	ALT0 - P1_7 ALT1 - TRIG_OUT2 ALT3 - LPUART2_CTS_B ALT4 - CT_INP7	ANALOG - ADC0_A23 VDD SYS - WUU0_IN9	IO Supply - VDD Pad type - MED Default - DIS

Note:

- +I3C in Pad Type represents that strong pull up resistor is implemented on the pin. PV bit is implemented in Pin Control register of the pin.
- +I2C_FILT in Pad Type represents that I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.

- HD in Pad Type represents that the pin can support up to 20mA drive strength. I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 5VTOL in Pad Type represents that the pin is 5V tolerant.
- DIS in default column represents that the pin's input buffer is disabled by default
- RST pads support passive filter and 1M ohm pull resistor. PFE and PV bits are implemented in Pin Control register of the pin.
- PE, PS, SRE, ODE and DSE are supported in Pin Control register of all types of IO.
- 5VTol and HD pads support two DSE bits in Pin Control register of the pin.
- SPI and I2C ISP interface are not available in MCXA14x and MCXA15x.
- USB ISP interface is not available in MCXA13x.
- SLOW in Pad Type represents the IO supports 25MHz. MED in Pad Type represents the IO supports 50MHz.

6.2 MCXA153, A152, 143, A142, A133, A132 Pinouts

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, refer to the "Pinout" tab in the Excel file.

6.3 Recommended connection for unused analog and digital pins

Table 41 shows the recommended connections for pins if those pins are not used in the customer's application

Table 41. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD	Must be powered	VDD powers the mux logic for PORT 0, PORT 1, PORT 2, and PORT 3. It must be powered during POR. The recommendation is to keep it powered, but it can be connected to the output of the Smart Power Switch and be left floating in shelf storage mode.
Power	VDD_ANA	Must be powered	
Power	VDD_USB	Tie to ground through a 10 kΩ resistor if VDD_USB is an independent pin in the package version used	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential

Table continues on the next page...

Table 41. Recommended connection for unused interfaces (continued)

Pin Type	Pin Function	Recommendation	Comments
Power	VSS_USB	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n*_*x*	Float	
Analog/non-GPIO	ADC*n*_*x*/DAC*n*_OUT	Float	
Analog/non-GPIO	EXTAL	Float	
Analog/non-GPIO	XTAL	Float	Analog output - Float
Analog/non-GPIO	USB0_DP	Float	Float
Analog/non-GPIO	USB0_DM	Float	Float
GPIO/Analog	Px/ADC*n*_*x*	Float	Float (default is analog input)
GPIO/Analog	Px/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

7 Ordering parts

7.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MCXA143VFM

NOTE

For complete list of Orderable part numbers, please refer
#unique_1/unique_1_Connect_42_GUID-2513F2CE-3B58-4532-A519-FD6F07924968

8 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

8.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8.2 Part number format

Part numbers for this device have the following format:

B PS F D FS T PG SR PT

Table 42. Part number fields descriptions

Field	Description	Values
B	Brand	• MCX
PS	Product series name	• A
F	Family	• 1 = Baseline • 2 = Baseline Enhance • 3 = Analog
C	Core Features	• 3 = 96 MHz, Motor PWM • 4 = 48MHz, Motor PWM, USB FS • 5 = 96MHz, Motor PWM, USB FS
FS	Flash Size	• 1 = 32 KB • 2 = 64 KB • 3 = 128 KB • 4 = 256 KB • 5 = 512 KB • 6 = 1024 KB
T	Junction Temperature range (°C)	• V = –40 to 125
PG	Package	• LH = LQFP 64 • FT = HVQFN 48 • FM = HVQFN 32
SR	Silicon Revision	• A = Initial Mask set • B = 1st Major spin • C = 2nd Major spin
PT	Package Type	• R = Tape and Reel • T = Tray

8.3 Example

This is an example part number:

MCXA143VLH

8.4 Small package marking

8.4.1 Package marking information

Table 43. Package marking

	32HVQFN 5*5	48HVQFN 7*7	64LQFP 10*10
First line	AAAAAA	AAAAAA	AAAAAAA
Second line	MMMMM	MMMMM	AAA MMMMM
Third line	XXYWXX	XXXYWXX	XXXXYYWWXX

Identifier	Description
a	Part number code, refer to Ordering Information
m	Mask set
y	Year
w	Work week
x	NXP internal use

9 Terminology and guidelines

9.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Table continues on the next page...

Table continued from the previous page...

Term	Definition
	NOTE Typical values are provided as design guidelines and are neither tested nor guaranteed.

9.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

9.3 Typical-value conditions

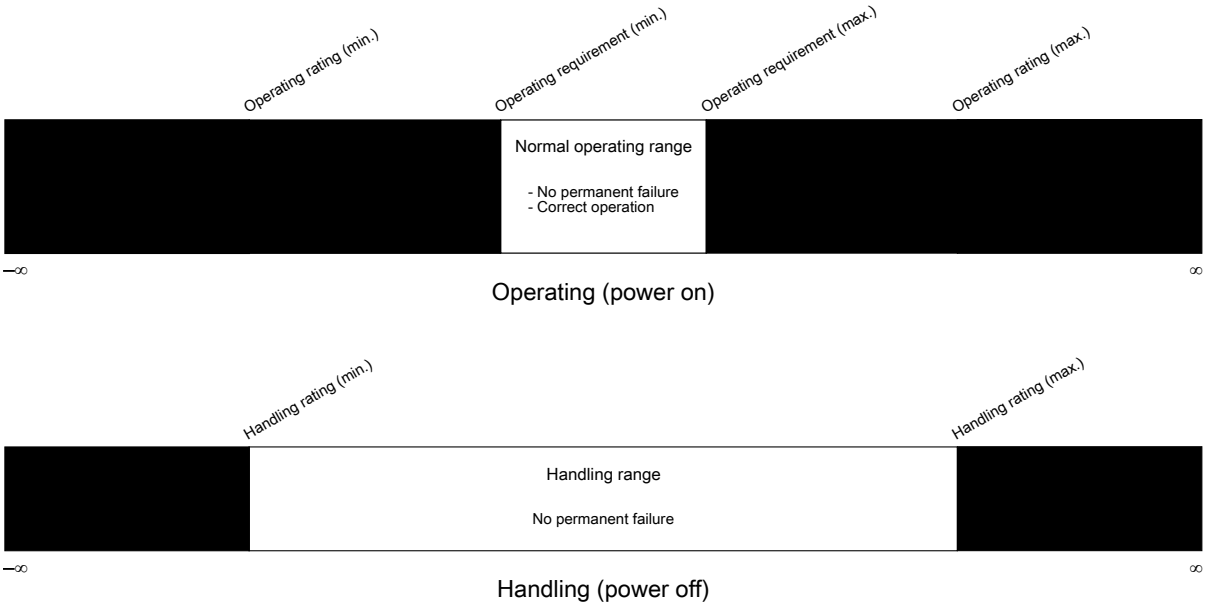
Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

NOTE

Typical values are based on characterization but not covered by test limits in production.

9.4 Relationship between ratings and operating requirements



9.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9.6 Specification Test Methods

Each specification is tested using one of these methods.

Code	Method	Description
P	Production direct	On every chip during production, testing the specification
I	Production indirect	On every chip during production, testing parts of a module that affect whether the chip meets the specification but not testing the specification itself
C	Characterization on a production tester	Measuring a statistically significant number of sample chips across process (matrix lot), voltage, and temperature
L	Characterization on lab equipment or a nonproduction tester	

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Code	Method	Description
		NOTE Typical values are not necessarily characterized across process.
D	Guaranteed by design	Specification based on scientific and engineering principles
O	Other	Using methods such as: • Performing silicon simulations • Performing package thermal simulations • Calculating specifications using reliability data

10 Revision history

The following table lists the changes in this document.

Rev. No.	Date	Substantial Changes
4	Sept 2024	• Added non-USB phantom parts in data sheet • Updated the front matter and Feature comparison • Updated Block diagram and added Bus matrix figure • Added I/O mux resistance table • Updated the content in Power consumption operating behaviors section • Updated CMP to LPCMP and RST_B to RESET_B • Unified power mode naming • Added Junction to Case Top Thermal Resistance in Thermal Attributes • Added Standard drive and Middle drive in Condition column of Device clock specs • Updated FRO-16K to FRO16K and updated temperature from 105 to 125 • Added content in LPUART section • Updated speed in LPSPI master mode timing • Updated Part Number format • Removed the content in ADC electrical specifications • Updated the values in ADC electrical specifications

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Rev. No.	Date	Substantial Changes
		• Added Note after Typical-value conditions table • Updated pinout table • Unified package name through out to show package first and then pincount
3	Jan 2024	• Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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