Initial Release

High Speed Quad MOSFET Driver

Features

- 6ns rise and fall time
- 2A peak output source/sink current
- 1.2V to 5V input CMOS compatible
- ±5V to ±12V supply voltage operation
- Smart Logic threshold
- Low jitter design
- Quad matched channels
- Drives two N and two P-channel MOSFETs
- Outputs can swing below ground
- Built-in level translator for negative gate bias
- User-defined damping for return-to-zero application
- Low inductance quad flat no-lead package
- Thermally-enhanced package

Applications

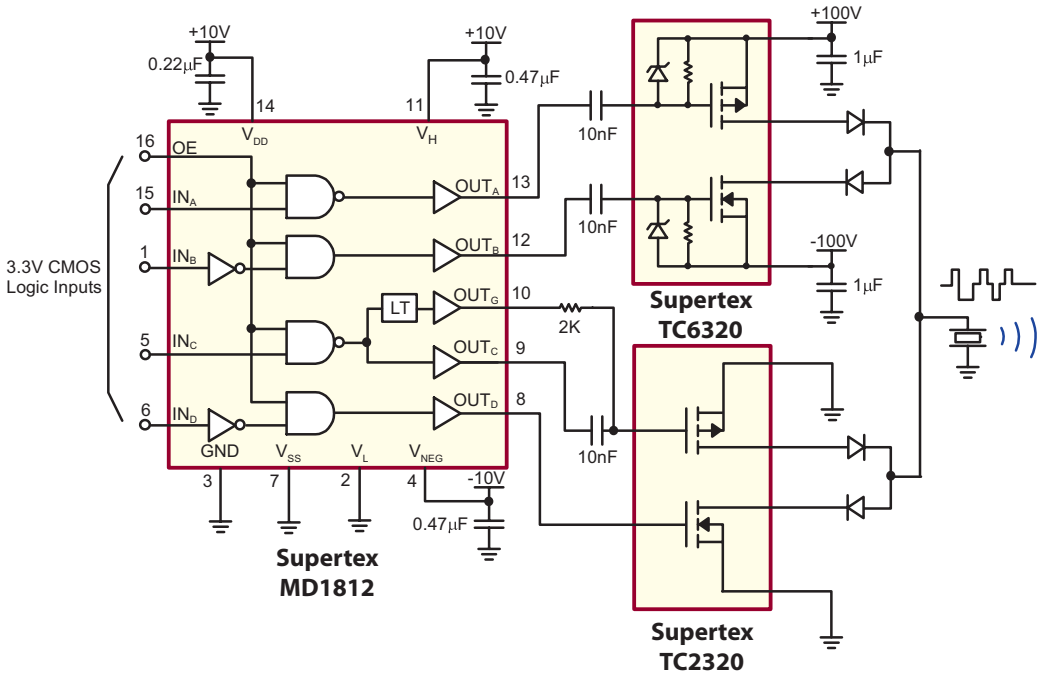
- Ultrasound PN code transmitter
- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Nondestructive evaluation
- High speed level translator
- High voltage bipolar pulser

General Description

The Supertex MD1812 is a high-speed quad MOSFET driver. It is designed to drive two N and two P-channel high voltage DMOS FETs for medical ultrasound applications but may be used in any application that needs a high output current for a capacitive load. The input stage of the MD1812 is a high-speed level translator that is able to operate from logic input signals of 1.2 to 5.0 volt amplitude. An adaptive threshold circuit is used to set the level translator threshold to the average of the input logic 0 and logic 1 levels. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation. The output stage of the MD1812 has separate power connections enabling the output signal L and H levels to be chosen independently from the driver supply voltages.

As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V and –5V, and the output L and H levels may be varied anywhere over the range of –5V to +5V. The output stage is capable of peak currents of up to ±2 amps, depending on the supply voltages used and load capacitance. The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Secondly, when OE is low, the outputs are disabled, with the A and C outputs high and the B and D outputs low. This assists in properly pre-charging the coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS. A built-in level shifter provides P-MOS gate negative bias drive. This enables the user-defined damping control to generate return-to-zero bipolar output pulses.

Typical Application Circuit



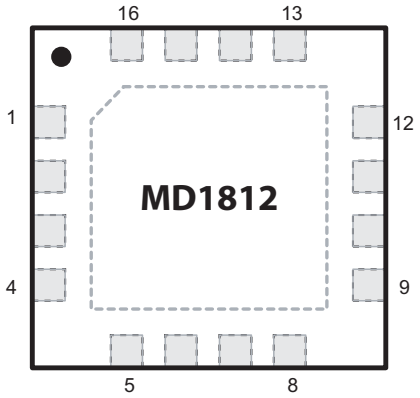
NR031706

Device	Package Option
	16-lead 4x4x0.9 QFN
MD1812	MD1812K6-G

-G indicates package is RoHS compliant ('Green')

16-Lead QFN (K6) Package

16-Lead QFN (K6) Pin Configuration



Top View

Pin Description

Pin #	Function	Description
1	IN_B	Logic input. Controls OUT_B when OE is high.
2	V_L	Supply voltage for N-channel output stage.
3	GND	Device ground.
4	V_{NEG}	Supply voltage the auxiliary gate drive.
5	IN_C	Logic input. Controls OUT_C when OE is high.
6	IN_D	Logic input. Controls OUT_D when OE is high.
7	V_{SS}	Supply voltage for low-side analog, level shifter, and gate drive circuit.
8	OUT_D	Output driver.
9	OUT_C	Output driver.
10	OUT_G	Auxiliary output driver.
11	V_H	Supply voltage for P-channel output stage
12	OUT_B	Output driver.
13	OUT_A	Output driver.
14	V_{DD}	Supply voltage for high-side analog, level shifter, and gate drive circuit.
15	IN_A	Logic input. Controls OUT_A when OE is high.
16	OE	Output enable logic input.

Note: Thermal pad and pin #4, V_{NEG} must be connected externally.

Absolute Maximum Ratings

Parameter	Value
V_{DD}-V_{SS}, Logic Supply Voltage	-0.5V to +13.5V
V_H, Output High Supply Voltage	V_L-0.5V to V_{DD}+0.5V
V_L, Output Low Supply Voltage	V_{SS}-0.5V to V_H+0.5V
Vss, Low Side Supply Voltage	-7V to +0.5V
V_{NEG}-V_{SS}, Negative Supply Voltage	V_{SS}-13.5V to V_{SS}+0.5V
Logic Input Levels	V_{SS}-0.5V to V_{SS}+7V
Maximum Junction Temperature	+125°C
Storage Temperature	-65°C to 150°C
Soldering Temperature	235°C
Package Power Dissipation	2.2W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

DC Electrical Characteristics

($V_H = V_{DD}$ = 12V, $V_L = V_{SS}$ = GND = 0V, V_{NEG} = -12V, V_{OE} = 3.3V, T_J = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD} - V_{SS}	Logic supply voltage	4.5	-	13	V	---
V_{SS}	Low side supply voltage	-5.5	-	0	V	---
V_H	Output high supply voltage	V_{SS}+2	-	V_{DD}	V	---
V_L	Output low supply voltage	V_{SS}	-	V_{DD}-2	V	---
V_{NEG}	Negative supply voltage	-13	-	V_{SS}-2	V	May connect to V_{SS} if OUT_G not used
I_{DDQ}	V_{DD} quiescent current	-	1.5	-	mA	No input transitions, OE = 1
I_{HQ}	V_H quiescent current	-	-	10	µA	
I_{NEGQ}	V_{NEG} quiescent current	-	-	10	µA	
I_{DD}	V_{DD} average current	-	7.0	-	mA	One channel on at 5.0Mhz, No load
I_H	V_H average current	-	22	-	mA	
I_{NEG}	V_{NEG} average current	-	1.5	-	mA	
V_{IH}	Input logic voltage high	V_{OE}-0.3	-	5	V	For logic inputs IN_A, IN_B, IN_C, and IN_D
V_{IL}	Input logic voltage low	0	-	0.3	V	
I_{IH}	Input logic current high	-	-	1.0	µA	
I_{IL}	Input logic current low	-	-	1.0	µA	
V_{IH}	OE Input logic voltage high	1.2	-	5	V	For logic input OE
V_{IL}	OE Input logic voltage low	0	-	0.3	V	
R_{IN}	Input logic impedance to GND	12	20	30	KΩ	
C_{IN}	Logic input capacitance	-	5	10	pF	---

Outputs

($V_H = V_{DD}$ = 12V, $V_L = V_{SS}$ = GND = 0V, V_{NEG} = -12V, V_{OE} = 3.3V, T_J = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	-	12.5	Ω	I_{SINK} = 50mA
R_{SOURCE}	Output source resistance	-	-	12.5	Ω	I_{SOURCE} = 50mA
I_{SINK}	Peak output sink current	-	2.0	-	A	---
I_{SOURCE}	Peak output source current	-	2.0	-	A	---

AC Electrical Characteristics

($V_H = V_{DD}$ = 12V, $V_L = V_{SS}$ = GND = 0V, V_{NEG} = -12V, V_{OE} = 3.3V, T_J = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{irf}	Input or OE rise & fall time	-	-	10	ns	Logic input edge speed requirement
t_{PLH}	Propagation delay when output is from low to high	-	7	-	ns	C_{LOAD} = 1000pF, see timing diagram Input signal rise/fall time 2ns
t_{PHL}	Propagation delay when output is from high to low	-	7	-	ns	
t_{POE}	Propagation delay OE to output	-	9	-	ns	
t_{PCG}	Propagation delay IN_C to OUT_G	-	28	-	ns	
t_r	Output rise time	-	6	-	ns	
t_f	Output fall time	-	6	-	ns	
$\lvert t_r - t_f \rvert$	Rise and fall time matching	-	1.0	-	ns	for each channel
$\lvert t_{PLH} - t_{PHL} \rvert$	Propagation low to high and high to low matching	-	1.0	-	ns	
Δt_{dm}	Propagation delay matching	-	±2.0	-	ns	Device to device delay match

Logic Truth Table

Logic Inputs			Output		
OE	IN_A	IN_B	OUT_A		OUT_B
H	L	L	V_H		V_H
H	L	H	V_H		V_L
H	H	L	V_L		V_H
H	H	H	V_L		V_L
L	X	X	V_H		V_L
OE	IN_C	IN_D	OUT_C	OUT_G	OUT_D
H	L	L	V_H	V_{SS}	V_H
H	L	H	V_H	V_{SS}	V_L
H	H	L	V_L	V_{NEG}	V_H
H	H	H	V_L	V_{NEG}	V_L
L	X	X	V_H	V_{SS}	V_L

Application Information

For proper operation of the MD1812, low inductance bypass capacitors should be used on the various supply pins. The GND pin should be connected to the logic ground. The IN_A, IN_B, IN_C, IN_D and OE pins should be connected to a logic source with a swing of GND to V_{CC}, where V_{CC} is 1.2 to 5.0 volts. When input logic(s) is high, output(s) will swing to V_L, and when input(s) logic is low, output(s) will swing to V_H. All inputs must be kept low until the device is powered up. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1812 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the V_{SS} and V_L pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connection V_{DD} should have a ceramic bypass capacitor to the ground plane, with short leads and decoupling components to prevent resonance in the power leads.

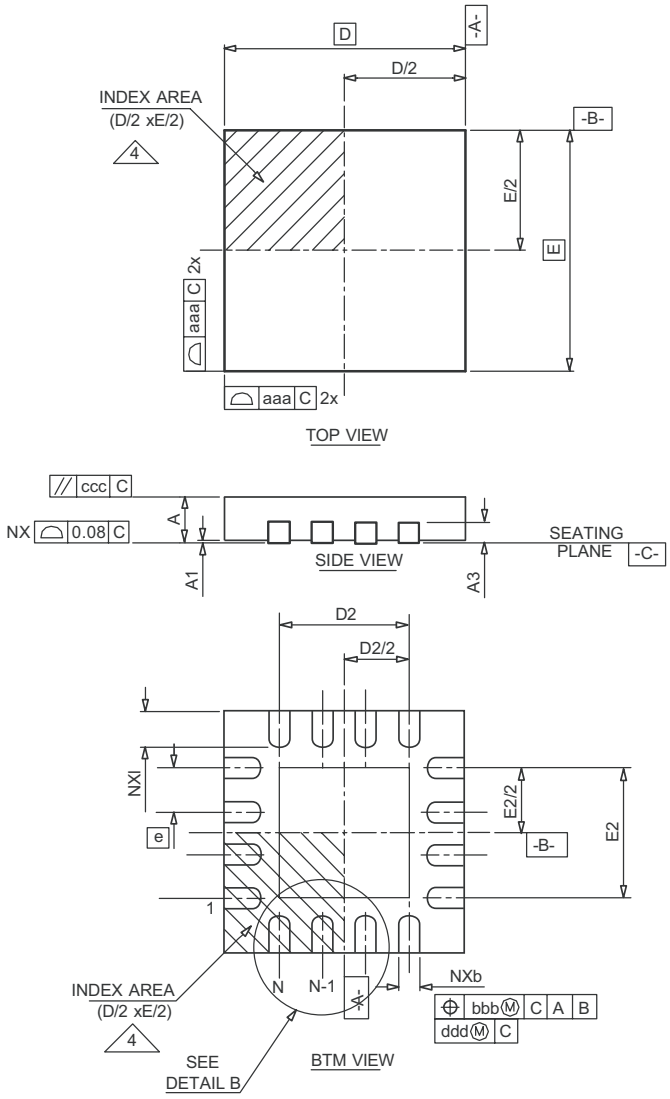
Output drivers, OUT_A and OUT_C, drive the gate of an external P-channel MOSFET, while output drivers OUT_B and OUT_D drive the gate of an external N-channel MOSFET, and they all swing from V_H to V_L. The auxiliary output drive, OUT_G, swings from V_{SS} to V_{NEG}, and drives the gate of an external P-channel MOSFET via a 2KΩ series resistor.

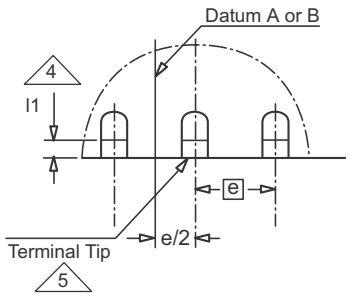
The voltages of V_H and V_L decide the output signal levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths, current loop area, and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistance in series with the output signal to obtain better waveform transitions at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

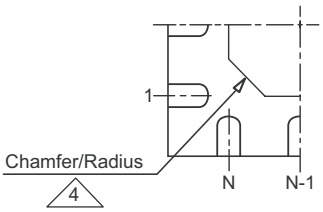
The OE pin sets the threshold level of logic for inputs (V_{OE} + V_{GND}) / 2. When OE is low, OUT_A and OUT_C are at V_H. OUT_B and OUT_D are at V_L. Auxiliary output OUT_G, is at V_{SS}, regardless of the inputs IN_A or IN_B.

Pay particular attention that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V, even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that a circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry. Best timing performance is obtained for OUT_C when the voltage of (V_{SS}-V_{NEG}) = (V_H-V_L).

16-Lead QFN Package Outline (K6)







Symbol	Height Dimensions		
	Min	Nom	Max
D BSC		4.0	
E BSC		4.0	
e		0.65	
D2	2.0	2.15	2.25
E2	2.0	2.15	2.25
b	0.25	0.30	0.35
l	0.45	0.55	0.65
A	0.80	0.90	1.0
A1	0.00	0.02	0.05
A3	---	0.20 ref	---
L1	0.03	---	0.15
Issue	A		

Tolerance of Form & Position	
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
Issue	A

Bottom ID Dimensions			
AA	BB	CC	DD
.344	.344	.181	.181

Notes:

1. *Dimensioning and tolerancing conform to ASME Y14.5m - 1994.*
2. *All dimensions are in millimeters, all angles are in degrees (°).*
3. *The terminal #1 identifier and terminal numbering convention shall conform to JEDEC publication 95, SPP-002. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.*
4. *Depending on the method of lead termination at the edge of the package, pull back (L1) may be present. L minus L1 to be equal to or greater than 0.33mm.*
5. *Dimension B applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension B should not be measured in that radius area.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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