5-A Peak, High Frequency, Dual Low-Side Driver

1 DESCRIPTION

The MD18624 high-frequency gate driver is designed to drive both low-side N-Channel MOSFETs with maximum control flexibility of independent inputs.

Each channel can source and sink 5A peak current along with rail-to-rail output capability. 7ns/6ns rise and fall time with 2.2nF load decrease the switching loss of MOSFET.

MD18624 has 11ns rising and falling propagation delay which allows the systems operating at high frequency with less delay matching variations. These delays are very suited for applications requiring dual-gate drivers with critical timing, such as synchronous rectifiers. When connecting two channels in parallel to increase current-drive capability, intelligent stack detection circuit is implemented to add extra 5nsdead-time between the two channels to avoid shoot through current without adding external series resistor.

The inputs can handle -10V to 20V PWM, which increases robustness against ringing from gate transformer and/or parasitic inductance of long routing traces. The input PINs thresholds are fixed and independent of the VDD supply voltage.

The MD18624 is offered in DFN-8 and SOP-8 packages

2 TYPICAL APPLICATIONS

- Power Supplies for Telecom, Datacom, and 48V to 72V Battery Powered Systems
- Switch-Mode Power Supplies
- Motor Control, Solar Power

3 FEATURES

- Two Independent Gate-Drive channels with Independent Inputs
- 5-A Source and Sink Output Peak Currents
- 7ns/6ns Rise and Fall Time with 2.2nF Load
- Fast Propagation Delay (11ns Typical)
- Excellent Propagation Delay Matching (1ns Typical)
- Intelligent stack detection to support Channel A paralleled with Channel B
- Input Pins Can Tolerate -10V to +26V, and are Independent of Supply Voltage Range
- TTL Compatible Inputs
- 4.5V to 26V VDD Operating Range, 28V ABS MAX
- Symmetrical Undervoltage Lockout for Channel A and Channel B
- Industry-standard-compatible Pinout
- Available in both DFN-8 and SOP-8 Packages
- Specified from -40°C to 140°C

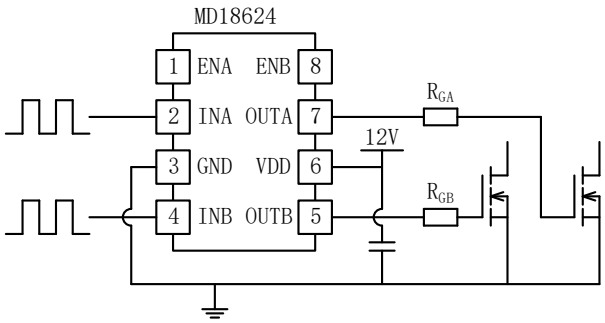
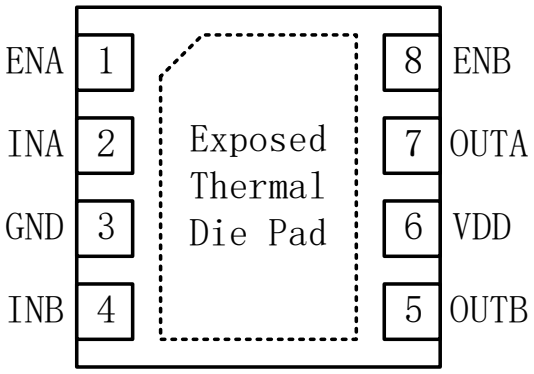
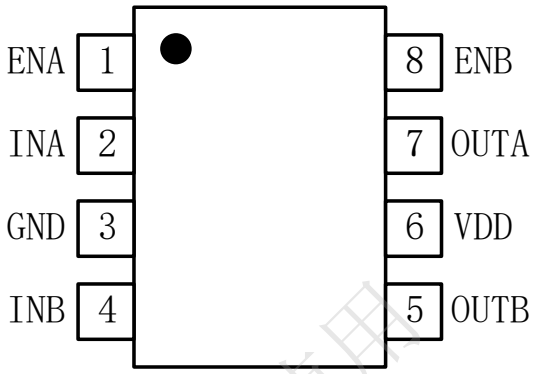


Figure 1. Functional Block Diagram

4 PACKAGE REFERENCE AND PIN FUNCTIONS



DFN-8



SOP-8

Pin #	Name	Description
1	ENA	Enable input for Channel A: ENA biased LOW Disables Channel A output regardless of INA state, ENA biased HIGH or floating Enables Channel A output
2	INA	Input of Channel A
3	GND	Negative supply for the device that is generally grounded. All signals of the device are referenced to this ground
4	INB	Input of Channel B
5	OUTB	Output of Channel B
6	VDD	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the device as possible
7	OUTA	Output of Channel A
8	ENB	Enable input for Channel B: ENB biased LOW Disables Channel B output regardless of INB state, ENB biased HIGH or floating Enables Channel B output

5 ABSOLUTE MAXIMUM RATINGS (1)

VDD.....-0.3V to +28V
INA ,INB, ENA, ENB .....–10V to +28V
OUTA, OUTB DC.....–0.3V to VDD+0.3V
Repetitive pulse(2) .....–2V to VDD+0.3V
Output continuous source/sink current.....0.3A

Continuous Power Dissipation (TA = +25°C) (3)
Junction Temperature ..... 150°C
Lead Temperature (Solder) ..... 260°C
Storage Temperature ..... –65°C to +150°C

6 Recommend Operation Conditions (4)

VDD.... .....4.5V to 26V
INA ,INB, ENA, ENB.....-5V to 26V
Maximum Junction Temp. (T_J).....+140°C

7 Thermal Resistance (5) ϑ_{JA} ϑ_{JC}

DFN-8.....64.0 37.8 °C/W
SOP-8.....TBD TBD °C/W

Notes:

(1) Exceeding these ratings may cause permanent damage to the device

(2) Repetitive pulse ≤100ns. Verified at bench characterization

(3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

(4) The device is not guaranteed to function outside of its operating conditions.

(5) Measured on JEDEC, 1S0P PCB.

8 ESD RATINGS

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

9 Electrical Characteristics

VDD=12V, T_A=T_J=-40°C to 140°C, 1uF capacitor from V_{DD} to GND. unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
VDD Start current	$I_{DD(off)}$	VDD = 3.4V INA = INB = 3.4V	20.7	38.7	56.6	uA
		VDD = 3.4V INA = INB = GND	20.8	38.6	56.4	uA
INPUTS(INA, INB)						
Input voltage rising threshold	V_{ITH}		1.94	2.14	2.34	V
Input voltage falling threshold	V_{ITL}		1.08	1.23	1.38	V
Input voltage hysteresis	V_{ITHYS}		0.74	0.91	1.08	V
INPUTS(ENA, ENB)						
Enable voltage rising threshold	V_{ETH}		1.94	2.14	2.34	V
Enable voltage falling threshold	V_{ETL}		1.08	1.23	1.38	V
Enable voltage hysteresis	V_{ETHYS}		0.74	0.91	1.08	V
UNDERVOLTAGE LOCKOUT						
VDD rising threshold	V_{DDR}		3.95	4.24	4.46	V
VDD falling threshold	V_{DDF}		3.66	3.93	4.14	V
VDD threshold hysteresis	V_{DDHYS}		0.21	0.31	0.41	V
OUTPUTS(OUTA, OUTB)						
Sink/Source peak current	I_{SNK} /I_{SRC}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		±5		A
High output voltage	V_{OH}	I_{OUT} = -10mA			0.02	V
Low output voltage	V_{OL}	I_{OUT} = 10mA			0.016	V
Output pullup resistance	R_{OH}	I_{OUT} = -10mA	0.5	1	2	Ω
Output pulldown resistance	R_{OL}	I_{OUT} = 10mA	0.4	0.8	1.6	Ω
PROPAGATION DELAYS						
Inx(A/B) turn-on propagation delay	T_{D1}	C_{LOAD}=2.2nF, 5V input pulse	5	11	20	ns
Inx(A/B) turn-off propagation delay	T_{D2}	C_{LOAD}=2.2nF, 5V input pulse	5	11	20	ns
Enx(A/B) turn-on propagation delay	T_{D3}	C_{LOAD}=2.2nF, 5V enable pulse	5	11	20	ns
Enx(A/B) turn-off propagation delay	T_{D4}	C_{LOAD}=2.2nF, 5V enable pulse	5	11	20	ns
Delay matching between 2 channels	t_M	INA = INB, OUTA and OUTB at 50% transition point		1	4	ns
OUTPUT RISE AND FALL TIME						
Rise time	t_R	C_{LOAD}=2.2nF, from 10% to 90%		7.6	19	ns
Fall time	t_F			6.2	11	ns
MISCELLANEOUS						
Minimum input pulse width that changes the output				10	20	ns

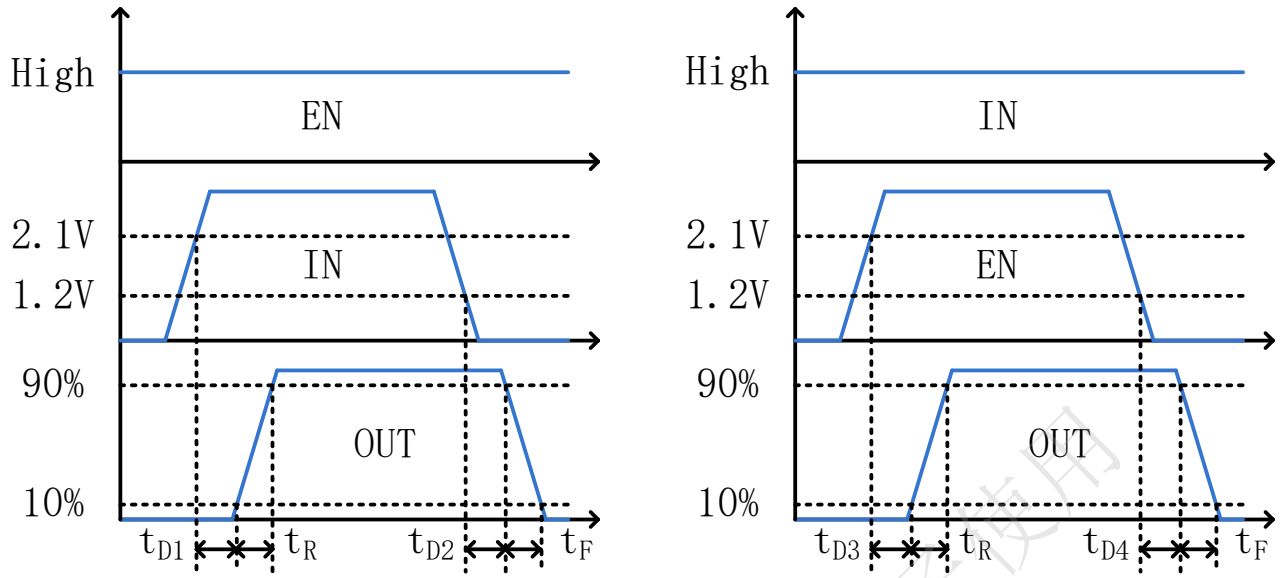


Figure 2. Timing Diagram

10 TYPICAL CHARACTERISTICS

VDD=3.4V, C_{L_OUTA}= C_{L_OUTB}=470pF

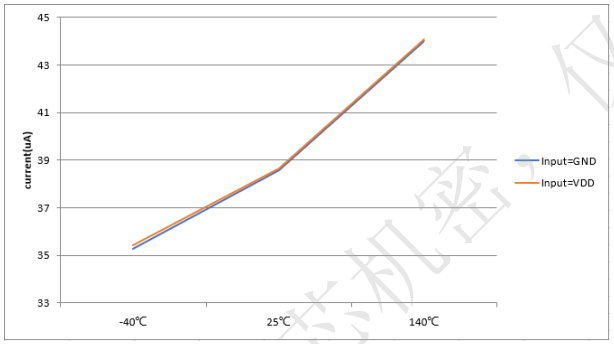


Figure 3. Start-Up Current vs Temperature

VDD=12V, f_{sw}=500kHz, C_{L_OUTA}= C_{L_OUTB}=470pF

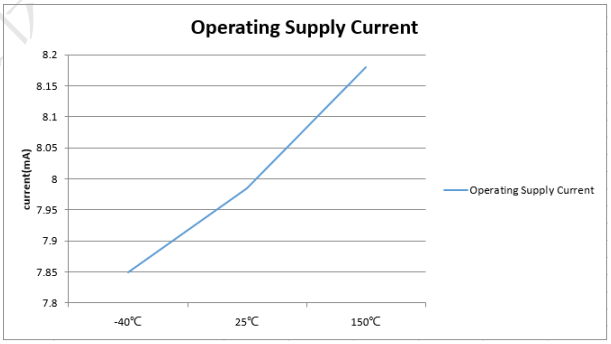


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

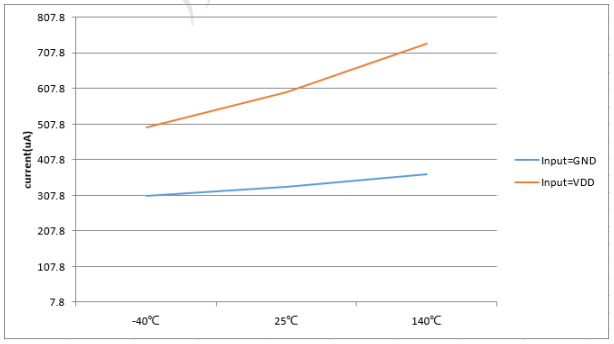


Figure 5. Supply Current vs Temperature (Outputs in DC ON/OFF Condition)

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

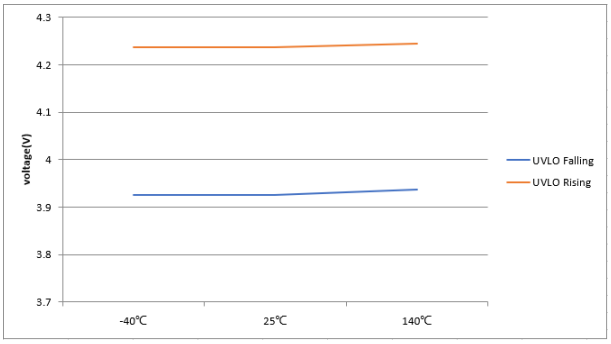


Figure 6. UVLO Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

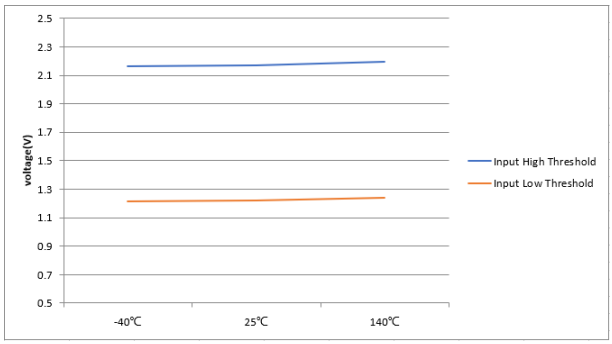


Figure 7. Input Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

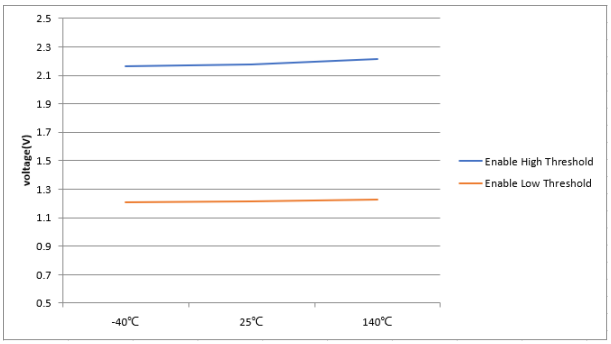


Figure 8. Enable Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

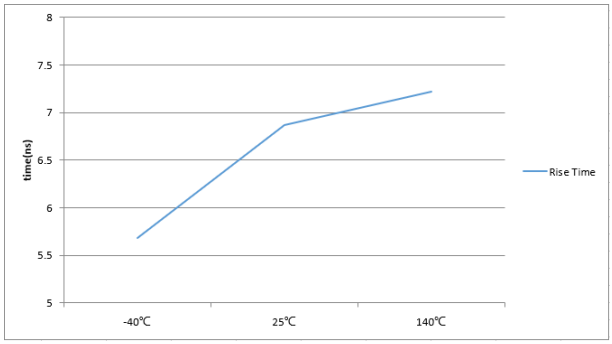


Figure 9. Rise Time vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

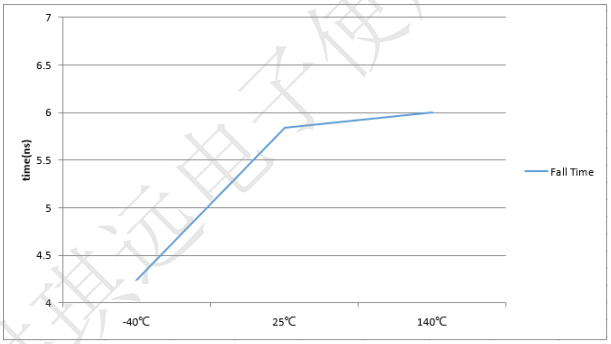


Figure 10. Fall Time vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

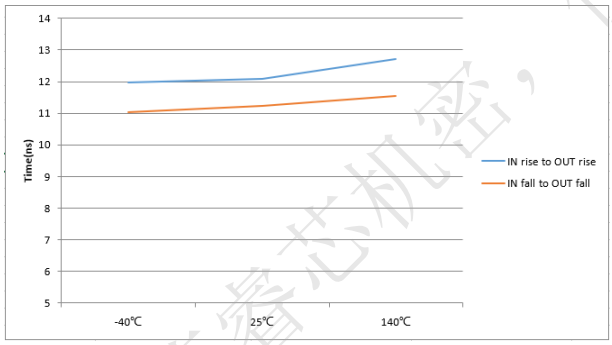


Figure 11. Input to Output Propagation Delay vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

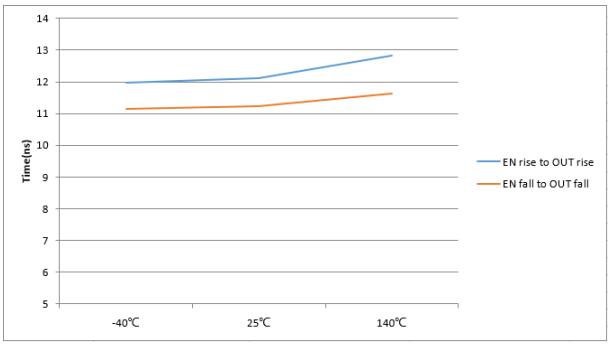
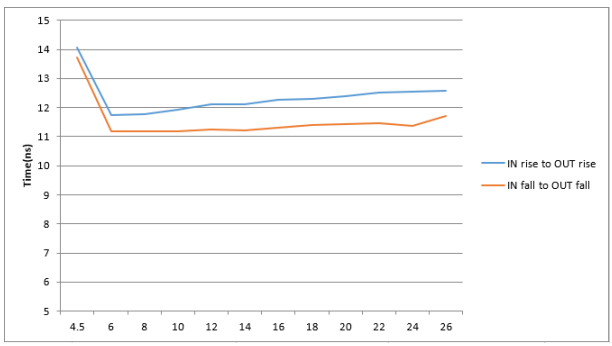


Figure 12. Enable to Output Propagation Delay vs Temperature

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF



25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

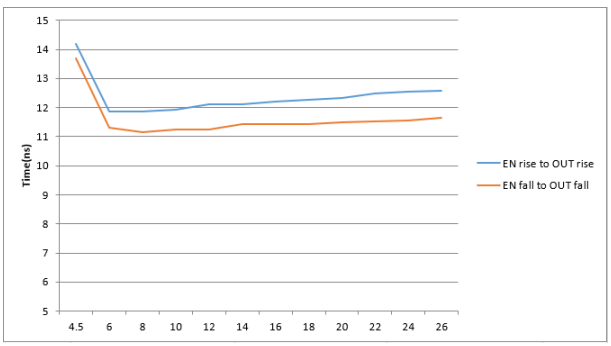


Figure 13. Input Propagation Delays vs VDD Voltage

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

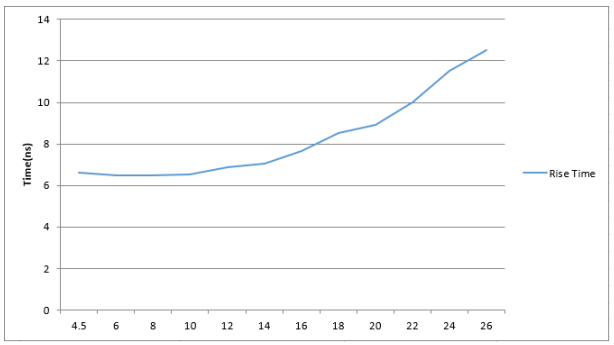


Figure 15. Rise time vs VDD Voltage

Figure 14. Enable Propagation Delays vs VDD Voltage

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

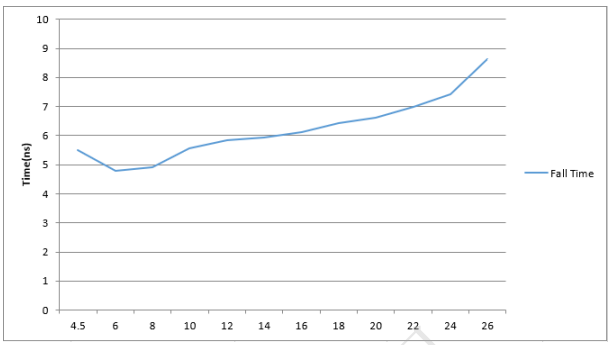


Figure 16. Fall time vs Temperature

11 BLOCK DIAGRAM

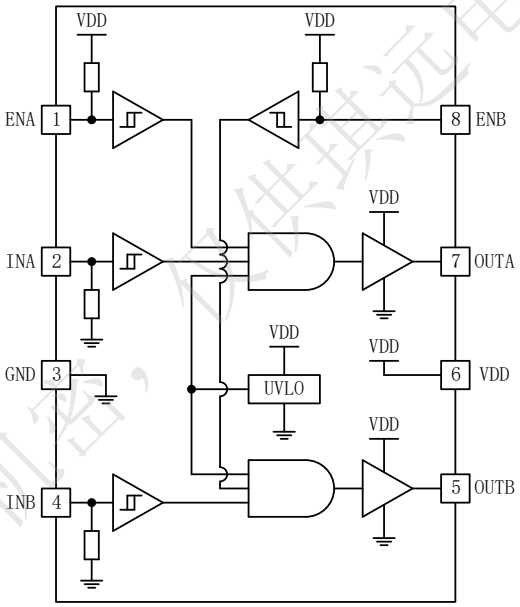


Figure 17. Functional Block Diagram

12 OPERATION

12.1 Overview

MD18624 is a dual-channel non-invertible high-speed low-side driver with supporting up to 26V wide supply. Each channel can source and sink 5A peak current along with the minimum propagation delay 11ns from input to output. The 1ns delay matching and 7ns switching time support higher switching frequency and driving capability. The ability to handle -10V DC input increase the noise immunity of driver input stage. The 26V rail-to-tail outputs can drive both MOSFET and IGBT.

12.2 Functional Modes

MD18624 operates in normal mode and UVLO mode. In the normal mode, the output state is dependent on states of the input pins. See as below:

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	X(1)	X(1)	L	L
X(1)	X(1)	L	L	L	L
X(1)	X(1)	L	H	L	H
X(1)	X(1)	H	L	H	L
X(1)	X(1)	H	H	H	H

Notes:

(1) X = Floating condition

12.3 VDD power supply and Undervoltage Lockout(UVLO)

MD18624 operates with the supply voltage from 4.5V to 26V. This feature make MD18624 has the ability to drive both MOSFET and IGBT. For the best performance, VDD bypass capacitor(1uF to 10uF) in parallel are recommended to supply energy for switching. Using a decoupling cap(0.1uF as usual) to prevent noise problems.

MD18624 has internal UVLO protection feature on the VDD supply circuit blocks. When VDD is rising and the voltage is still below UVLO threshold, this function keeps the outputs 'LOW', regardless of the status of the inputs. The UVLO is typically 4.2V with 0.3V hysteresis. This prevents VDD noise and dropping.

For example, at power up, MD18624 output remains 'LOW' until the VDD voltage reaches the UVLO threshold if ENA and ENB is 'High' or floating. The OUTPUT rise along with VDD until steady state VDD is reached.

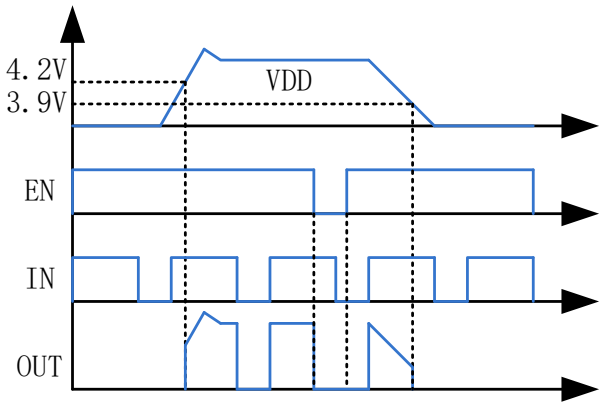


Figure 18. MD18624 operation sequence

12.4 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices especially for certain applications such as synchronous rectification where the driver outputs disable in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

MD18624 provide independent enable pins(ENx) for exclusive control of each driver channel operation. when ENx pins are driven 'HIGH' the driver is enabled and when ENx pins are driven 'LOW' the drivers are disabled. The enable pins are based on a TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V and 5-V MCU.

The ENx pins are internally pulled up to V_{DD} using pullup resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed.

12.5 Input Function

The input pins of MD18624 gate-driver device is based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.2 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices.

The INx pins are internally pulled down to GND using pulldown resistors as a result of which the outputs of the device are disabled in the default state. This feature is used to keep OUTx 'LOW' when VDD supply voltage rise.

12.6 Output Stage

The MD18624 device output stage features the pull up structure with P-MOS and the pull down structure with N-MOS. P-MOS provides the pull up capability when Input is 'HIGH', and the R_{OH} parameter (see **ELECTRICAL CHARACTERISTICS**) is a DC measurement which is representative of the on-resistance of the P-Channel device. N-MOS provides the pull down capability when Input is 'LOW', the R_{OL} parameter (see **ELECTRICAL CHARACTERISTICS**) is a DC measurement which is representative of the on-resistance of the N-Channel device.

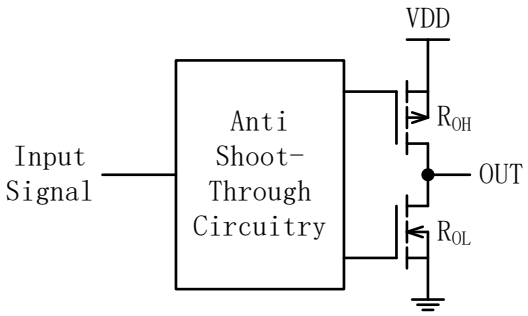


Figure 19. MD18624 Gate Driver Output Structure

Each output stage in MD18624 can supply 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

The MD18624 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven

complementary to each other. This situation is due to the extremely low drop-out offered by the MOS output stage of MD18624, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

12.7 Output Parallel Capability

The MD18624 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be paralleled when the driven power device required higher driving capability. For example, in the secondary of hard switching full bridge converter, there are two or more power MOSFETs in parallel to support high current output capability. The parallel power MOSFETs are preferred to be driven by a common gate control signal. By using MD18624, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. To support the parallel output, intelligent stack detection is implement. When two channels are connected together, internal circuit will recognize this parallel application and add extra 5ns dead-time to avoid shoot through.

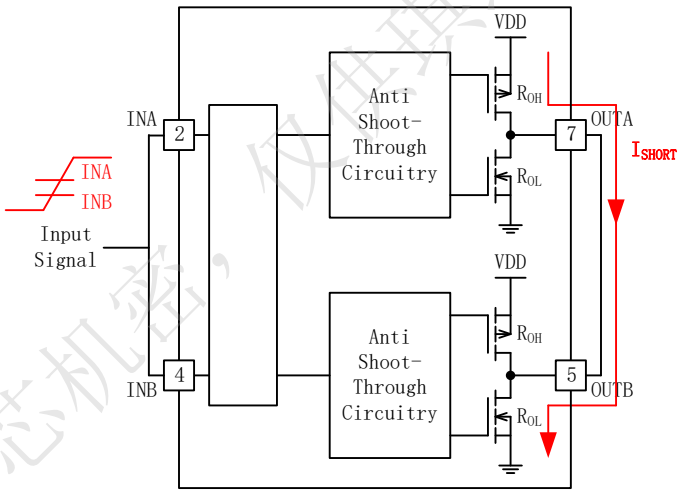


Figure 20. MD18624 Parallel Output Structure

Due to the rising and falling threshold mismatch between INA and INB, shoot through current conduction as shown in Figure 17 when directly connecting OUTA and OUTB pins. To avoid the shoot through current, intelligent stack detection is implemented. Extra 5ns dead-time is added between the two channels to cancel the delay between the two channels when slow dv/dt input signals are employed. No extra dead-time is added when the two channels parallel are not detected, so has no influence to propagation delay under normal operation. With the benefit of the intelligent stack detection circuit, MD18624 can support slow input signal slew rate (<20V/us) without external gate resistor in series with OUTA and OUTB, so wider application range and lower BOM count is obtained.

CH1: IN **CH2: OUT**

Single output driving waveform

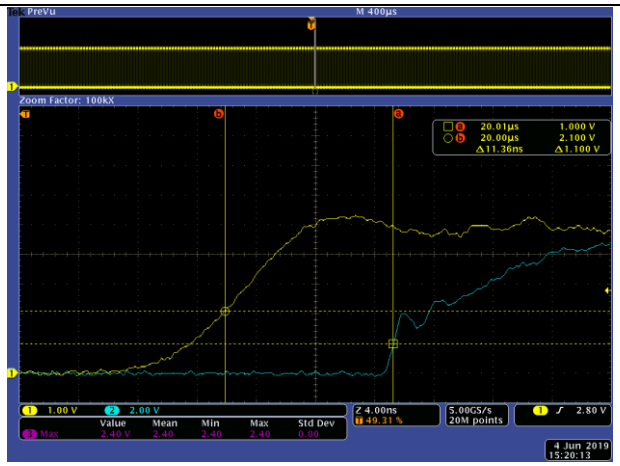


Figure 21. Turn-on propagation delay

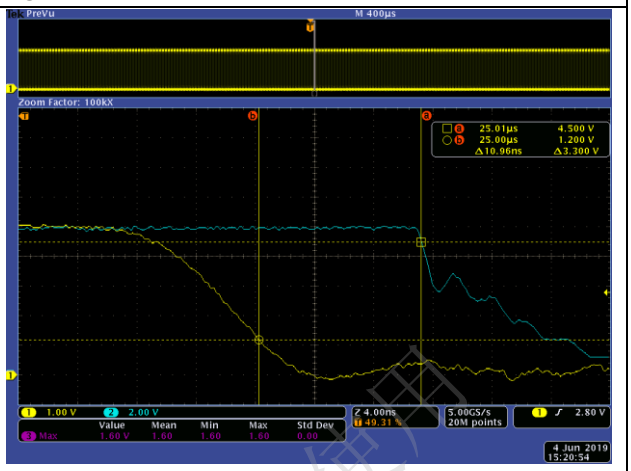


Figure 22. Turn-off propagation delay

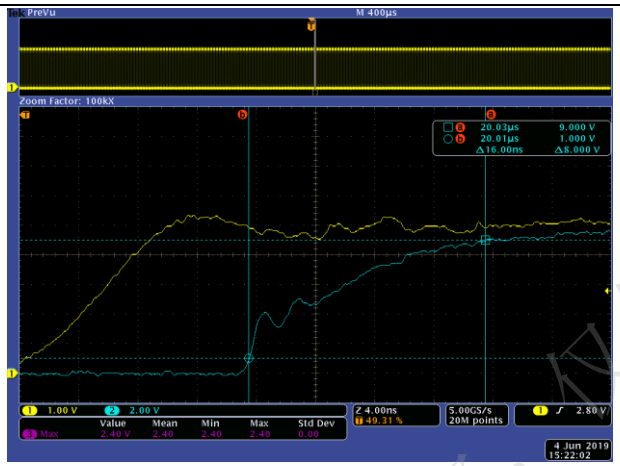


Figure 23. Rise time

Figure 24. Fall time

Dual outputs in parallel driving waveform

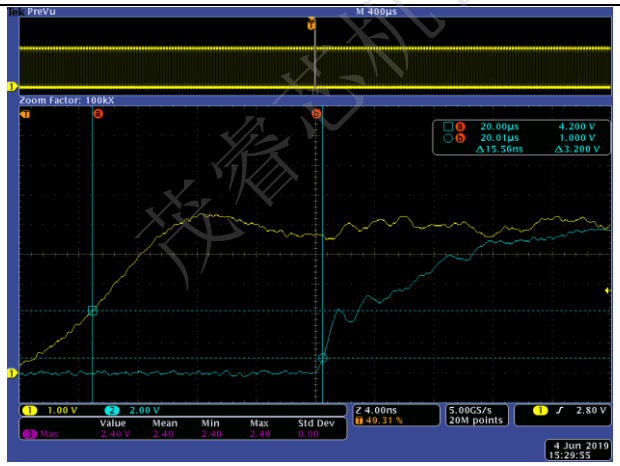


Figure 25. Turn-on propagation delay

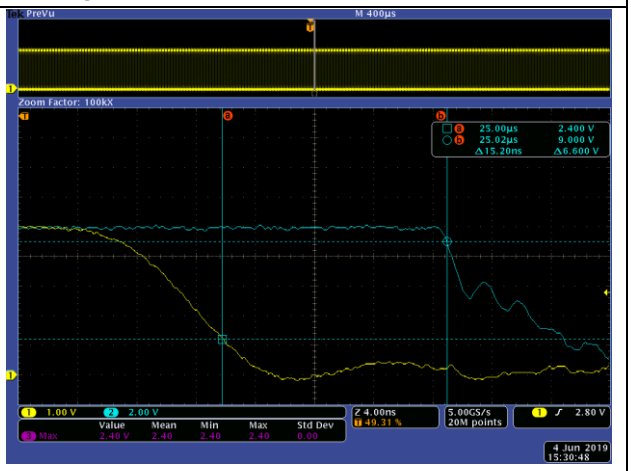


Figure 26. Turn-off propagation delay

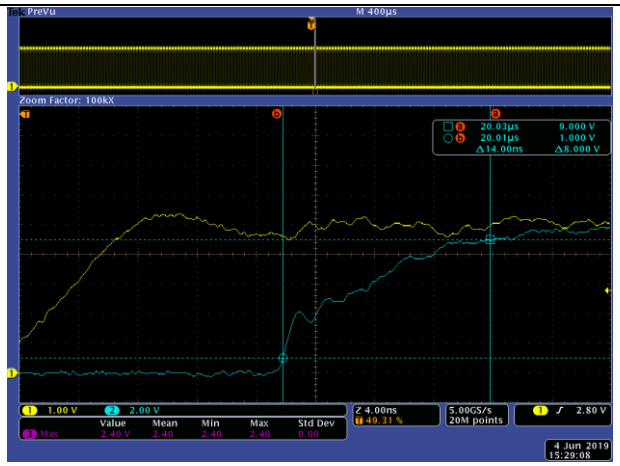


Figure 27. Rise time

Figure 28. Fall time

13 APPLICATION AND IMPLEMENTATION

13.1 Typical Application

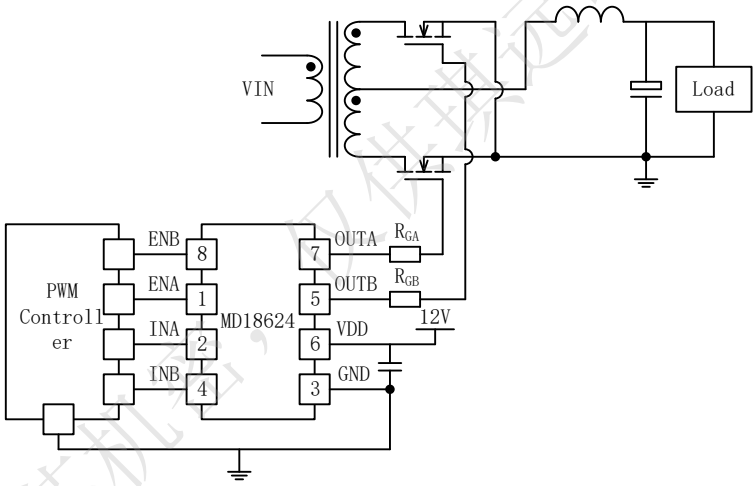


Figure 29. Synchronous Rectification Application

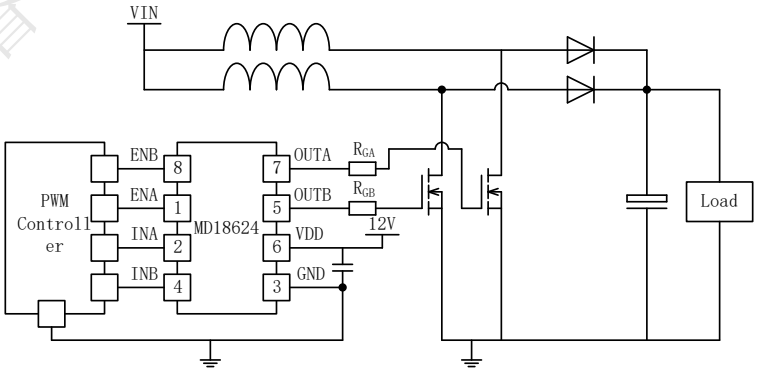


Figure 30. PFC Application

13.2 Driver Power Dissipation

Generally, the power dissipated in the MD18624 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The MD18624 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G = \frac{1}{2} \times C_{LOAD} \times V_{DD}^2 \quad (1)$$

where

C_{LOAD} is load capacitor

V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 2.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} \quad (2)$$

where

f_{sw} is the switching frequency

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the Equation 3 to provide Equation 4 for power:

$$Q_G = C_{LOAD} \times V_{DD} \quad (3)$$

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_g \times V_{DD} \times f_{SW} \quad (4)$$

To decrease the stress of MOSFET, adding a gate resistor between output of MD18624 and gate of MOSFET, and the power loss of resistor is given by Equation 5.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OL}}{R_{OL}+R_{GATE}} + \frac{R_{OH}}{R_{OH}+R_{GATE}}\right) \quad (5)$$

14 Layout

14.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

(1) Locate the driver close to the MOSFETs.

(2) Locate the VDD-VSS capacitors close to the driver.

(3) Connect the VSS pin to thermal pad and use the thermal pad as GND. The GND trace from MD18624 does directly to the source of the MOSFET, but not be in the high current path of MOSFET source current.

(4) For system using multiple drivers, the decoupling capacitors need to be located at VDD-VSS for each driver.
(5) Avoid placing VDD, INA, INB, ENA, ENB trace close to OUTA, OUTB signals or any other high dV/dT traces that can induce significant noise into the high impedance leads.
(6) Use wide trace for INA, INB, ENA and ENB to decrease the influence of switching ringing made by parasitic inductance.
(7) For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.

14.2 Layout Example

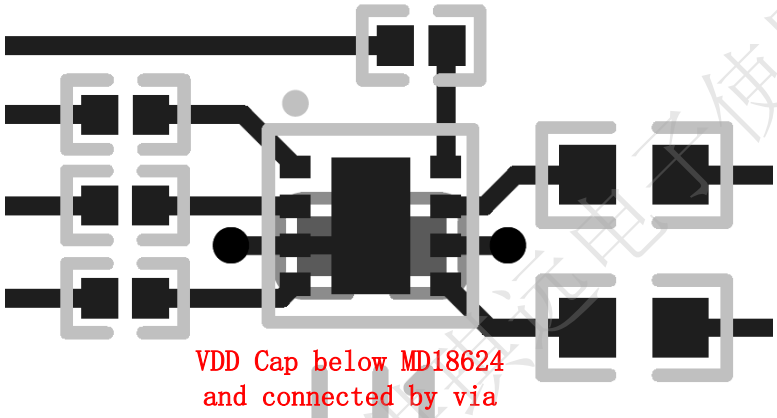


Figure 31. MD18624 PCB Layout Example

14.3 Package size

14.3.1 DFN-8 Package

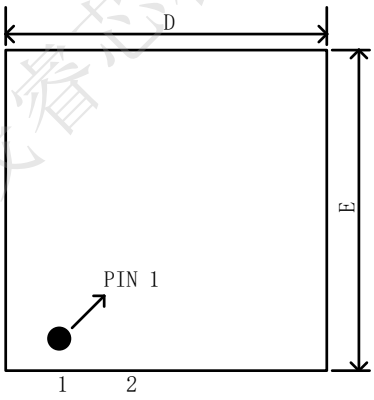


Figure 32. MD18624 Top View

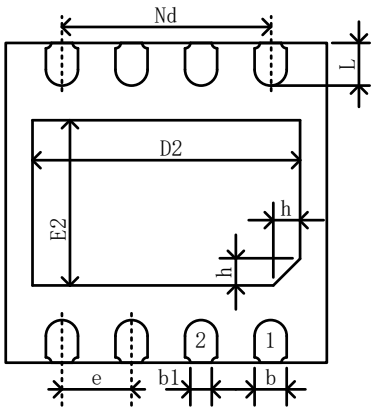


Figure 33. MD18624 Bottom View

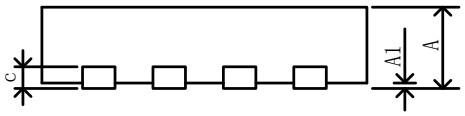


Figure 34. MD18624 Side View

SYMBOL	Millimeter		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1		0.2REF	
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e		0.65BSC	
Nd		1.95BSC	
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30

14.3.2 SOP-8 Package

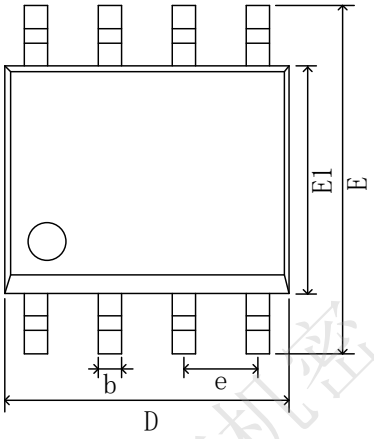


Figure 35. MD18624 Top View

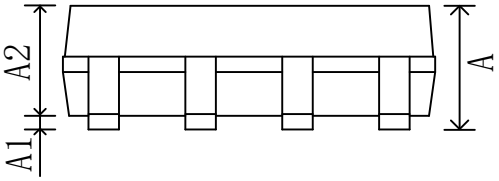


Figure 36. MD18624 Side View

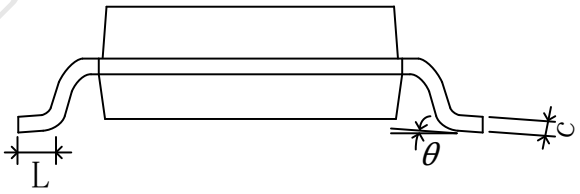


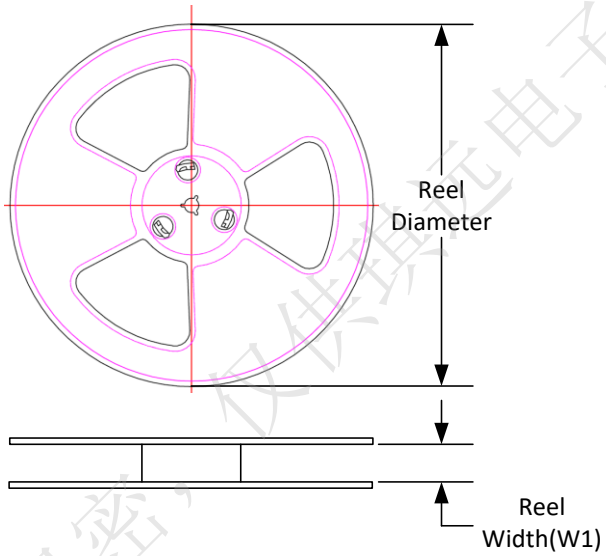
Figure 37. MD18624 Side View

SYMBOL	Millimeter	
	MIN	NOM
A	1.450	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510

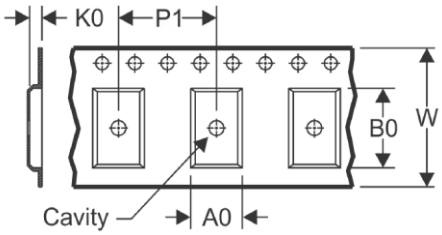
c	0.170	0.250
D	4.700	5.100
E	5.800	6.200
E1	3.800	4.000
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

15 REEL AND TAPE INFORMATION

REEL DIMENSIONS

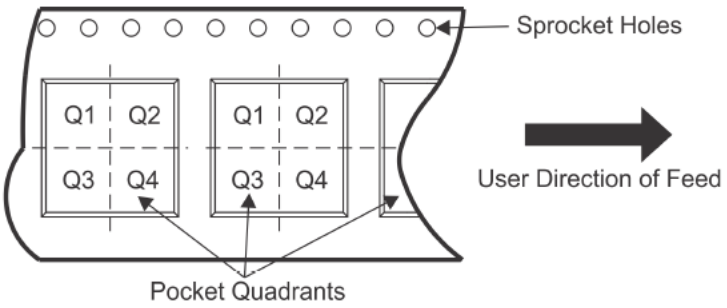


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION TAPE



Device	Package Type	Package Drawing	Pins	Quantities	Reel Diameter (mm)	Reel Width W1(mm)
MD18624DFN	DFN	DFN	8	3000	332	12.5
A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
4.0	3.3	1.1	8.0	12.0	Q1	

16 TAPE AND REEL BOX DIMENSIONS