MD231G SPECIFICATION

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0 Version History

Data	Version	Description of change	Author
2012-08-08	01.00	Origin	Changchun Zhu

1 Introduction

This document describes the hardware interface of the MD231G GSM/GPRS module which can be integrated with a wide range of applications. This document can help you quickly understand MD231G interface specifications, electrical and mechanical details. With the help of this document and other MD231G application notes, user guide, you can use MD231G module to design and set-up mobile applications quickly.

1.1. Related documents

[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.05:	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE –DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[3]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module –Mobile Equipment (SIM – ME) interface
[4]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[5]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[6]	GSM 11.10	Digital cellular telecommunications system (Phase 2)； Mobile Station (MS) conformance specification； Part 1: Conformance specification
[7]	GSM 07.10	Digital Cellular telecommunications system (Phase 2+); Terminal Equipment to Mobile Station multiplexer protocol, verion 7.2.0 Release 1998
[8]	GSM 07.10 V7.1.0	Digital cellular telecommunications system (Phase 2+);Terminal Equipment to Mobile Station (TE-MS)multiplexer protocol
[9]	GSM 07.07 V7.5.0	AT command set for GSM Mobile Equipment
[10]	CMT 11092011	OPENAT_MD231G_V3.2.0_USER_MANUAL_EN
[11]	CMT 02102012	MD231G_AT_DOCUMENT_20120210
[12]	CMT 09102006	CMT Wirless Phone feature

2. Product concept

Designed for global market, MD231G is a Dual-band GSM/GPRS/EDGE-Rx engine that works on frequencies EGSM 900 MHz/DCS 1800 MHz or GSM850/PCS1900 MHz. MD231G provides GPRS/EDGE-Rx class 12 capability. And MD231G also include a high performance signal-chip GPS solution which is able to achieve the industry's highest level of sensitivity, accuracy and Time-to-Firt-Fix(TTFF) with the lowest power consummation.

With a tiny configuration of 27.4*30.8*3.0 (mm), MD231G can fit almost all the space requirement in your application, such as Smart phone, PDA phone and wireless phone. The physical link to the interface board is 88 soldering pins.

The MD231G module is designed with power saving technique, the current consumption to as low as 3-4mA in Sleep mode (depends on network condition).

2.1. MD231G features at a glance

Feature	**Implementation**
Power supply	Single supply voltage 3.4V – 4.2V, typical: 3.8V
Power saving	Typical power consumption in Sleep mode to 3-4mA depends on network condition
Frequency bands	MD231G Dual band: EGSM 900/ DCS 1800 or GSM850/PCS 1900.
Transmit power	Class 4 (2W) at EGSM900 Class 1 (1W) at DCS1800 and PCS 1900
GPRS/EDGE-Rx connectivity	GPRS/EDGE-Rx class 12
Temperature range	Normal operation: -40°C to +85°C
SMS	MT, MO, CB, Text and PDU mode SMS storage: SIM card Support transmission of SMS alternatively over CSD or GPRS. User can choose preferred mode.
FAX	Group 3 Class 1
SIM interface	Supported SIM card: 1.8V/3V
External antenna	Connected via antenna pad
Phonebook management	Supported phonebook types: SM, FD, LD, RC, ON, MC.
SIM Application Toolkit	Supports SAT class 3, GSM 11.14 Release 97
Real time clock	Implemented
Timer function	Programmable via AT command
Physical characteristics	Size: 27.4*30.8*3.0 Weight: 8g
Firmware upgrade	Firmware upgradeable over serial interface

3. Hardware Interface

3.1. Module Interface

The 88 pins described in detail in following chapters:
Power supply
UART
Analog audio interfaces
SPI interface
I2C
GSM Antenna
GPS Antenna
BT Antenna
SIM interface
Keyboard interface
LCD interface
Touch Panel
SD/MMC Card
RTC backup battery
Camera
GPIO and External Interrupt
ADC
USB
Charger Detect

3.2. Pin description

Table 1: Pin description

Item	Name	Function	Aux 0	Aux1	Aux2	PD/PU	Power Domain
1	GPIO0	GPIO0	SPI_MOSI0	U3RXD	PWM	PD	DVDD28
2	GND	Ground					
3	ANT_GPS	Antenna of GPS singal					
4	GND	Ground					
5	NLD8	Parallel LCD data8	GPIO33	DAIPCMIN	EINT6	PD	DVDD18_EMI

6	LPTE	parallel display interface tearing effect	GPIO50	CLKO4		PD	DVDD18_EMI
7	SPKPO	Speaker positive output					
8	SPKNO	Speaker negative output					
9	MIC_PO	Microphone 0 input(Positive)					
10	MIC_NO	Microphone 0 input(Negative)					
11	XMIC	Microphone 1 input()					
12	AU_OUTO_P	Voice handset output(Positive)					
13	AU_OUTO_N	Voice handset output(Negative)					
14	MP3_OUTL	Aoudio head phone output(R channel)					
15	MP3_OUTR	Aoudio head phone output(L channel)					
16	VCHG_DET	Voltage of Charger detect					
17	USB_DM	D- data input/output					
18	USB_DP	D+ data input/output					
19	SIM_RST	SIM card reset output					
20	SIM_DATA	SIM data input/outputs					
21	SIM_CLK	SiM card clock output					
22	VSIM	LDO output for SIM					
23	KCOL6	Keypad column6	GPIO4	U1RXD	MCDA2	PD	DVDD28
24	KROW3	Keypad row3	GPIO15	DAISYNC	LSAODA11	PD	DVDD28
25	KCOL7	Keypad column7	GPIO3	EDICK	LSAODA10	PD	DVDD28
26	KROW2	Keypad row2	GPIO16	LSCKO	LSDIO	PD	DVDD28
27	KROWO	Keypad row0	GPIO18	LSDIO	LSCKO	PD	DVDD28

28	KCOL3	Keypad column3	GPIO7	DAIPCMIN		PD	DVDD28
29	KCOL2	Keypad column2	GPIO8	DAICLK		PD	DVDD28
30	KROW1	Keypad row1	GPIO17	U1CTS	DAIRST	PD	DVDD28
31	KROW7	Keypad row7	GPIO11	EINT3	EDIDAT	PD	DVDD28
32	SPIMOSI	Data singal from master output to slave input	GPIO9	KCOL1		PD	DVDD28
33	SDA	I2C data	GPIO2	SPICS0		PD	DVDD28
34	SCL	I2C colck	GPIO1	SPISCK0		PD	DVDD28
35	NC	reserved					
36	VIO28	LDO output of 2.8V					
37	LPCE_B	Parallel display interface chip select output	GPIO45	LSCE0B1		PU	DVDD18_EMI
38	LPRSTB	Parallel display inerface reset signal	GPIO51	EINT8	LSCK4	PD	DVDD18_EMI
39	LWR_B	Parallel display interface write strobe	GPIO42			PD	DVDD18_EMI
40	LRD_B	Parallel display interface read strobe	GPIO43			PD	DVDD18_EMI
41	LPA0	Parallel display interface address output	GPIO44			PD	DVDD18_EMI
42	NLD7	Parallel LCD data7	GPIO34	LPTE1		PD	DVDD18_EMI
43	NLD6	Parallel LCD data6	GPIO35			PD	DVDD18_EMI
44	NLD5	Parallel LCD data5	GPIO36			PD	DVDD18_EMI
45	NLD4	Parallel LCD data4	GPIO37			PD	DVDD18_EMI
46	NLD3	Parallel LCD data3	GPIO38	LSDI3		PD	DVDD18_EMI
47	NLD2	Parallel LCD data2	GPIO39	LSDA02		PD	DVDD18_EMI
48	NLD1	Parallel LCD data1	GPIO40	LSA0DA13		PD	DVDD18_EMI

49	**NLD0**	Parallel LCD data0	GPIO41	LSCK2		PD	DVDD18_EMI
50	**UTXD1**	UART1 transmit data	GPIO26	U3CTS	LSDA01	\	DVDD28
51	**URXD1**	UART1 receive data	GPIO25	EINT11	LSDAI1	PU	DVDD28
52	**ANT_BT**	Antenna of Bluetooth					
53	**CMPCLK**	CMOS sensor master clock output	GPIO64	CMCSK		PD	DVDD28
54	**CMMCLK**	CMOS sensor master clock output	GPIO63			PD	DVDD28
55	**CMPDN**	CMOS sensor power down control	GPIO62	LSCE0B2	U3TXD	\	DVDD28
56	**CMVSYNC**	CMOS sensor vertical reference signal input	GPIO61	SDA		PD	DVDD28
57	**CMRST**	CMOS sensor reset signal output	GPIO65			PD	DVDD28
58	**CMDAT7**	CMOS sensor data input 7	GPIO59	U3CTS	PWM	PD	DVDD28
59	**CMDAT6**	CMOS sensor data input 6	GPIO58	LSDA04	DAISYNC	PD	DVDD28
60	**CMDAT5**	CMOS sensor data input 5	GPIO57	LSCK5	DAIPCMOUT	PD	DVDD28
61	**CMDAT4**	CMOS sensor data input 4	GPIO56	LSA0DA15	DAICLK	PD	DVDD28
62	**CMDAT3**	CMOS sensor data input 3	GPIO55	LRSTB	DAIPCMIN	PD	DVDD28
63	**CMDAT2**	CMOS sensor data input 2	GPIO54	SCL		PD	DVDD28
64	**CMDAT1**	CMOS sensor data input 1	GPIO53	CMCSD1		PD	DVDD28
65	**CMDAT0**	CMOS sensor data input 0	GPIO52	CMCSD0		PD	DVDD28
66	**CMHSYNC**	CMOS sensor horizontal reference signal input	GPIO60	EINT9	U3RXD	PD	DVDD28
67	**UTXD2**	UART2 transmit data	GPIO24	U3TXD	CLKO7	PD	DVDD28

68	URXD2	UART2 receive data	GPIO23	LSCE0B0	U1RTS	PD	DVDD28
69	GND	Ground					
70	ANT_GSM	Antenna of GSM					
71	GND	Ground					
72	PWR_KEY	PWR key					
73	ADC4	Auxiliarey ADC input					
74	YP	Touch panel Y-asis poisitive input					AVDD28_ABB
75	XP	Touch panel X-asis poisitive input					AVDD28_ABB
76	XM	Touch panel X-asis negative input					AVDD28_ABB
77	YM	Touch panel Y-asis negative input					AVDD28_ABB
78	VBACKUP	Voltage of RTC					
79	VBAT	Power supply of Battery					
80	VBAT	Power supply of Battery					
81	MCCLK	SD serial clock/memory stick serial clock	GPIO30			PD	DVDD33_MSDC
82	MCDA0	SD serial data IO/memory stick serial clock	GPIO31			PD	DVDD33_MSDC
83	MCCM0	SD serial command output/memory stick serial clock	GPIO32			PD	DVDD33_MSDC
84	MCINS	SD card detect input	GPIO29	EINT5	LPTE1	PD	DVDD18_EMI
85	EINT0	External intrrupt0	GPIO66	EDIDAT		PD	DVDD28
86	SPI_MISO	Data singal from slave output to master input	GPIO19	LRSTB	DAIRST	PD	DVDD28
87	SPI_SCK	Bit serial clock	GPIO20			PD	DVDD28
88	SPI_CS	Low-active chip select singal	GPIOI22			PD	DVDD28

Notice: 1.DVVDD(2.7V-2.9V) 2.DVDD33_MSDC(3.0V-3.6V) 3. AVDD28_ABB (2.7V-2.9V)

3.3. Operating modes

The following table summarizes the various operating modes, each operating modes is referred to in the following chapters.

Table 2：Overview of operating modes

Mode	Function	
Normal operation	GSM/GPRS Sleep	Module will automatically go into Sleep mode if there is no air link activation and no hardware interrupt (such as GPIO interrupt or data on serial port). In this case, the current consumption of module will reduce to the minim. During sleep mode, the module can still receive paging message.
	GSM IDLE	Module has registered to the GSM network, and the module is ready to send and receive.
	GSM TALK	CSD connection is going on between two subscribers. In this case, the power consumption depends on network condition and settings such as DTX off/on, FR/EFR/HR, hopping sequences.
	GPRS IDLE	Module is ready for GPRS data transfer, but no data is currently sent or received. In this case, power consumption depends on network settings and GPRS configuration (e.g. multi-slot settings).
	GPRS DATA	There is GPRS data in transfer (PPP or TCP or UDP). In this case, power consumption is related with network settings (e.g. power control level), uplink / downlink data rates and GPRS configuration (e.g. used multi-slot settings).
POWER DOWN	The power management ASIC disconnects the power supply from the base band part of the module, only the power supply for the RTC is remained. Software is not active. The serial interfaces are not accessible.	
Alarm mode	RTC alert function launches this restricted operation while the module is in POWER DOWN mode. MD231G will not be registered to GSM network and only parts of AT commands can be available.	

3.4. Power supply

The power supply must be able to provide sufficient current up to 2A.

For the VBAT input, a local bypass capacitor is recommended. A capacitor (above 100μF, low ESR) is recommended. Multi-layer ceramic chip (MLCC) capacitors can provide the best combination of low ESR and small size but may not be cost effective. A lower cost choice may be a 100 μF tantalum capacitor (low ESR) with a small (1 μF to 10μF) ceramic in parallel, which is illustrated as following figure. And the capacitors should put as closer

as possible to the MD231G VBAT (RF) pins. A voltage regulator diode should been add between the Vbat and Gnd, and the BZV55C5V1 of Philips could been used. The following figure is the recommended circuit.

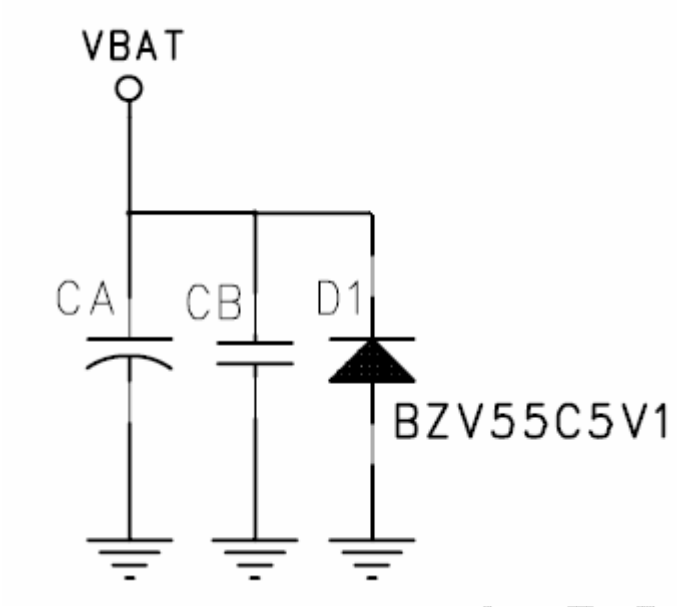


Figure 1：VBAT input

Table3: Power supply pins on the half-circle connector

Num	Name	Function	I/O	Min (V)	Type (V)	Max (V)	Note
79,80	VBAT	Power Supply	Input	3.3	4.2	4.6	Please make sure that the input voltage will never drops below 3.3V even in a transmit burst during which the current consumption may rise up to 2A.
2,4,69,71	GND	GND	GND				

Minimizing power losses

Please pay special attention to the supply power when you are designing your applications. Please make sure that the input voltage will never drops below 3.3V even in a transmit burst during which the current consumption may rise up to 2A. If the power voltage drops below 3.3V, the module may be switched off. You should also take the resistance of the power supply lines on the host board or of battery pack into account.

3.5. Power up and power down scenarios

3.5.1. Turn on MD231G

MD231G can be turned on by following two ways:

- Via PWRKEY pin: You can turn on the MD231G to normal operating mode by driving the PWRKEY to a low level voltage for 1500ms;
- Via RTC interrupt: starts ALARM modes;
- For some application system, we can connect the “PWRKEY” to “GND” so that the module will be turn on as soon as the 3.8V power supply to the module. But, if “PWRKEY” linked to “GND”, other keypad pin could not work. Here is a circuit to make the module power on automatically. If the module power on, the GPIO which is PD will output high level, on consequence, the “PWR_KEY” will be high level so that other keypad pin could work.

3.5.2. Turn off MD231G

MD231G can be truned off by following two ways:

- Driving the PWRKEY to a low level for 1500ms when module working
- Use “AT + CKPD=”P”, 50” command to turn off MD231G module.

3.5.3. System reset of MD231G

The pin 35 RESETB is the output signal of MD231G, It could be used for reset the chipset such as the WIFI,ATV.

3.5.4. Power saving

The module could enter into sleep mode to save power through use the at command **"AT+ESLP=1".**

3.6. UART

MD231G provides 2 UARTs with hardware flow control and speed up to 921600 bps. The UARTs provide full duplex serial communication channels between the module and external devices.
Serial Port can be used for CSD FAX, GPRS service and send AT command of controlling module. Serial port supports the communication rate as following:
1200, 2400, 4800, 9600 (Default), 19200, 38400, 57600, 115200
The serial port
The follow table is the pin definition of UART.

Table4: UART interface of the MD231G

Pin	Name	Function	Pin	Name	Function
50	TXD1	UART1-Transmit Data	51	RXD1	UART-Receive Data
67	TXD2	UART2-Transmit Data	68	RXD2	UART2-Receive Data

Notice: **CTS1&RTS1 also is the Aux function of Pin Kow1 and RXD2, if these two pins have been used , you could not use the CTS and RTS function.**

The reference design of standard serial port level witching circuit is as follow figure:

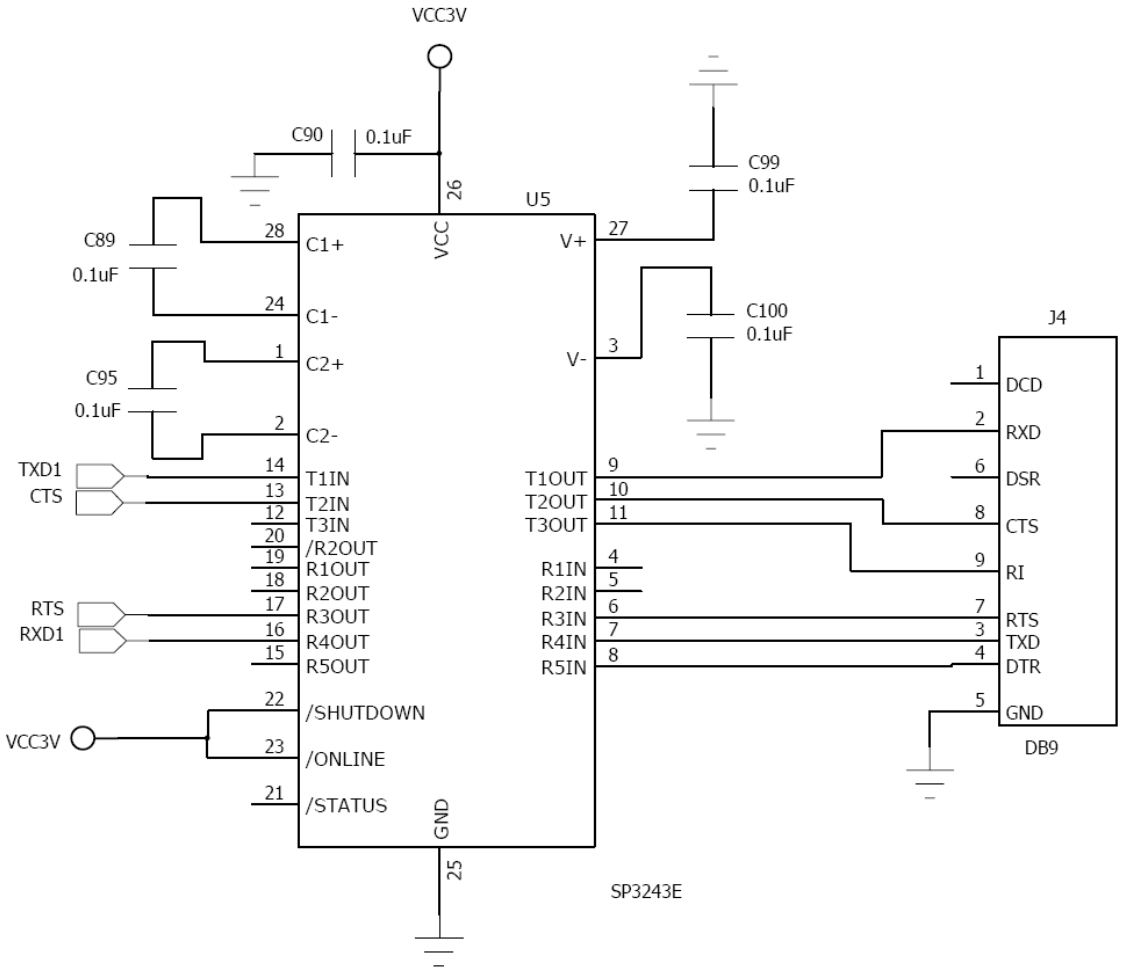


Figure2 The reference diagram of standard serial port level switching circuit

3.7. Audio interfaces

The module provides two audio channels:
EAR and MIC, used for microphone and receiver;
AUXI and AU_MOUT, used for line in and line out;
The audio should be far away from the radio part to reduce TD noise from radio.
The audio pins definitions are as follow table:

Table5: Audio interface of the MD231G

Pin	Name	Function	Pin	Name	Function
9	MICP0	Microphone amplifier positive input(+) output	10	MICN0	Microphone amplifier negative input(-) output
12	AU_OUT0_P	Earphone positive output(+)	13	AU_OUT0_N	Earphone negative output(-)
15	MP3_OUTR	Audio analog output right channel	14	MP3_OUTL	Audio analog output left channel
11	XMICP	Audio 1 chanel			
8	SPK_N	Audio amplifier negative output	7	SPK_P	Audio amplifier positive output

It is suggested that you adopt following matching circuit in order to satisfy speaker effect.

The difference audio signals have to be layout according to difference signal layout rules. If you want to adopt an amplifier circuit for audio, we commend National company's LM4890. But you can select it according to your needs.

The audio reference design as follow chart:

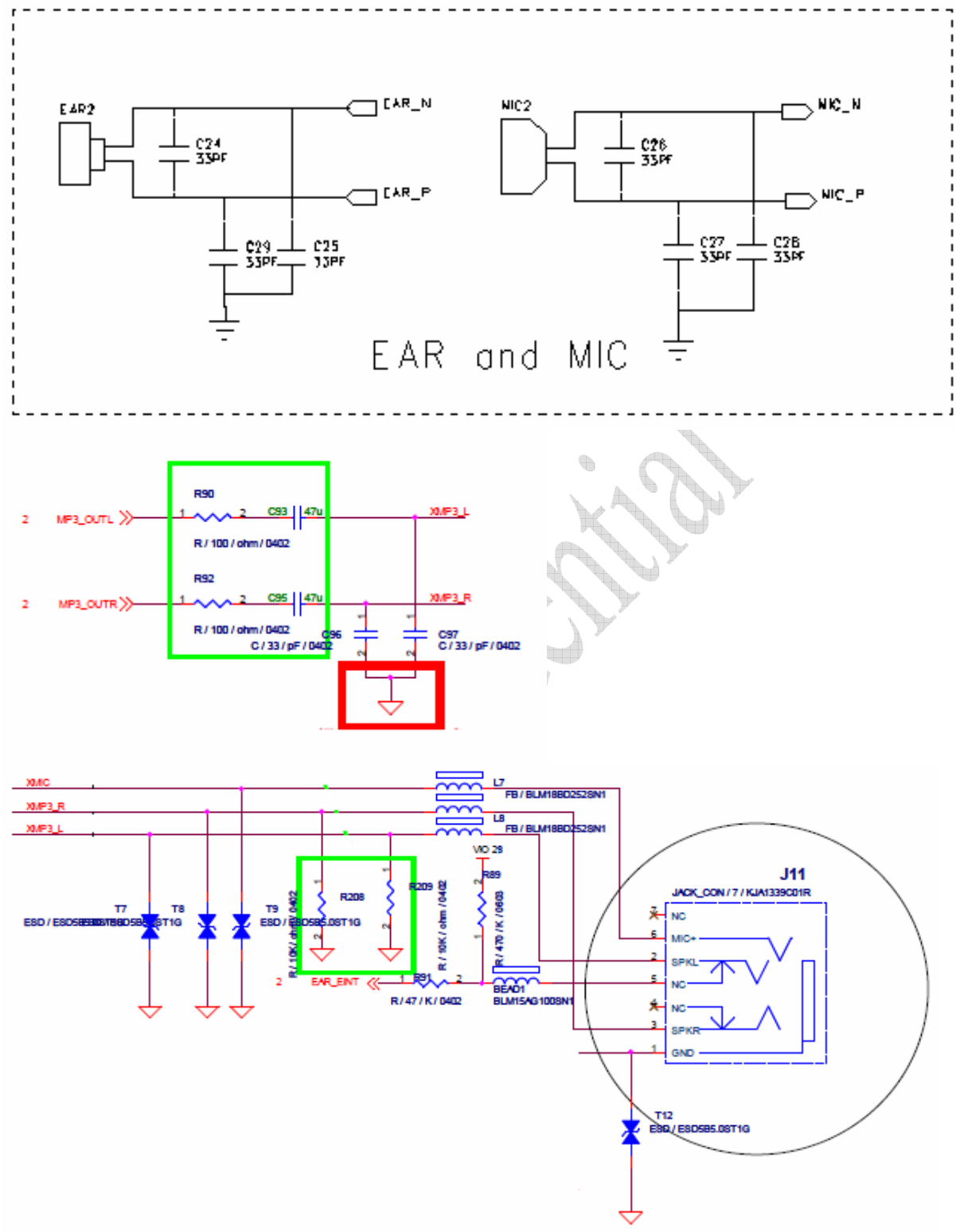


Figure3 The reference design of audio

The microphone bias electric circuit was designed in MD231G. The MIC_BIAS DC characteristics see the table 6.

Table 6：MIC_BIAS DC Characteristics

Parameter	Minimum	Typical	Maximum	Units
Microphone Bias Voltage (MIC_BIAS)		1.9		V
Source Current			2	mA

All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio are also provided. The audio stereo path facilitates CD-quality playback and voice playback through a headset.
MD231G has a built-in high fidelity calss AB audio power amplifier. It is capable of delivering 0.85 watt of power to an 8 ohm BTL load with less than 10% distortion.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	RMS power@1% THD	8Ω load, VBAT = 4.2V		850		mW
	THD + N	1kHz, Po = 600mWrms, 4.2V		0.1		%
	PSRR	20Hz ~ 1kHz, diff. mode	60	85		dB
	Shutdown current	SPK_EN = SPK_OUTSTG_EN = 0		1		μA
	Quiescent power supply current	VBAT = 4.2V, no input		4		mA
	Gain adjustment	Audio speaker mode		6/12		dB
	Gain adjustment	Voice receiver mode		-6		dB
	Gain adjustment steps	Audio speaker mode		6		dB

3.8. SPI Interface

The MD231G supply a SPI master interface for peripheral management including digital TV chips.

Table 7：Pin mapping of SPI interfaces

Pin	Name	Function	Pin	Name	Function
32	SPI_MOSI	Data singal from master output to slave input	86	SPI_MISO	Data singal from slave output to master input
87	SPI_SCK	Bit serial clock	88	SPI_CS	Low-active chip select singal

3.9. I2C

I2C is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

Table8: I2C interface of the MD231G

Pin	Name	Function
33	SDA	I2C data
34	SCL	I2C colck

3.10. GSM Antenna

The RF interface has an impedance of 50Ω. The antenna cable can be soldered to the pad. Pay attention, the line between the MD231G antenna pin and antenna connection should be thick and short. It is better to use filter circuit to fit 50 ohms.

Table9: RF output power：

Frequency	Max	Min
GSM850	33dBm±2dB	5dBm±5dB
E-GSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB

Table10: Module RF receive sensitivity：

Frequency	Receive sensitivity
GSM850	<-106dBm
E-GSM900	<-106dBm
DCS1800	<-104dBm
PCS1900	<-104dBm

Table11: MD231G receive/transmit frequency

Frequency	Receive	Transmit
GSM850	869~894MHz	824-849MHz
E-GSM900	925~960MHz	800-915MHz
DCS1800	1710~1785 MHz	1805~1800 MHz
PCS1900	1850~1910 MHz	1930~1990 MHz

According to the application, should use GSM900/DCS1800 Dual-band antenna or GSM850/PCS1900 Dual-band antenna.

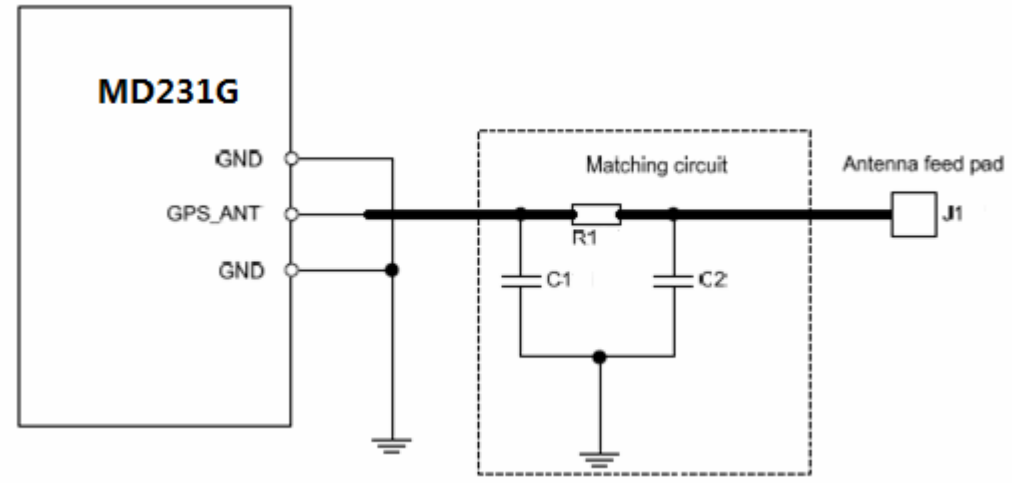
3.11.GPS Antenna

The MD231G include a high-performance singal-chip GPS solution which includes on-chip CMOS RF and digital baseband. It supports up to 210 PRN channels. With 66 serch channels and 22 simultaneous tracking channels, it acquires and tracks satellites in the shortest time even at indoor signal levels. I also supports various location and navigation applications, including autonomous GPS, SBAS ranging(WAAS, EGNOS, GAGAN, and MSAS), QZSS, DGPS(RTCM) and AGPS. It also has the excellent

low-power consumption characteristic (acquisition 24mW, track 17mW).
The RF interface has an impedance of 50Ω. To suit the physical design of individual applications, MD231G offers GPS_ANT pad.

2	GND	Ground
3	ANT_GPS	Antenna of GPS singal
4	GND	Ground

The customer's main board under the GPS_ANT pad should be copper keep out.
To minimize the loss on the RF cable, it need be very careful to choose RF cable. SIMCom recommend the insertion loss should be meet following requirements:
 GPS < 1dB
The customer's GPS antenna also can be located in the customer's main board and connect to module's GPS_ANT pad through microstrip line or other type RF trace which impendence must be controlled in 50Ω.



In this figure, the components R1, C1 and C2 is used for antenna matching, the components' value only can be got after the antenna tuning. Usually, matching components' value is provided by antenna vendor, the default value of R1 is 0Ω, and users need to reserve the place of C1 and C2 without soldering. The traces in bold type should be treated as 50Ω impedance controlled line in PCB layout.

GPS Antenna Choice Consideration

To obtain excellent GPS reception performance, a good antenna will always be required. The antenna is the most critical item for successful GPS reception in a weak signal environment. Proper choice and placement of the antenna will ensure that satellites at all elevations can be seen, and therefore, accurate fix measurements are obtained. Most customers contract with antenna design houses to properly measure the radiation pattern of the final mounted configuration in a plastic housing with associated components near the antenna. Linear antennas are becoming more popular, and the gain is reasonable, since a smaller ground plane can be used.
User can consider following factors as:
 Choose a linear antenna with a reasonably uniform hemispherical gain pattern of >-4dBi.
 Use of an antenna with lower gain then this will give less than desirable results. Please note that a RHCP antenna with a gain of 3dBi, equates to a linear polarized antenna of 0dBi.
 Proper ground plane sizing is a critical consideration for small GPS antennas.
 Proper placement of the GPS antenna should always be the FIRST consideration in integrating the MD231G GPS Module.
If the customer's design will allow for a ceramic RHCP patch antenna with an appropriately sized ground plane, and the patch is normally oriented towards the sky, then

that particular solution usually works the best. Note that if the patch antenna ground plane is less than 60x60mm, then compromises to the beam width and gain pattern could result. Usually the gain becomes very directional, and looses several dB of performance. Since results can vary, measuring the antenna radiation pattern in the final housing in an appropriate anechoic chamber is required. Some customers do not have the size availability to implement a patch antenna approach. In that instance, use of a Linear Polarized (LP) antenna is the next best alternative. There are new ceramic LP antennas on the market that exhibit reasonable gain characteristics once properly mounted in the housing, and when matched to an appropriate sized ground. Generally the ground plane requirements are smaller for a LP antenna when compared to a patch, but once again, proper testing in an anechoic chamber is a mandatory requirement. These ceramic elements will need to be located near the end of the ground plane, and will require several millimeters of clearance between the closest component. It is important to note that use of a LP antenna will result in a minimum of 3dB of gain loss when compared to a RHCP antenna at a defined elevation. This is due to the right hand gain rule of antenna propagation.
Use of PIFA antenna is another LP possibility, but the PIFA usually exhibits a considerable amount of gain nulls, or "holes" in the radiation pattern. This will be undesirable for obtaining a low circular error probability (CEP), since the antenna may not allow the receiver to capture the desired satellite at the ideal orientation due to these noted gain nulls. Once again, careful testing in an appropriate anechoic chamber is required.
If the customer's design is for automotive applications, then an active antenna can be used and located on top of the car in order for guarantee the best signal quality. GPS antenna choice should be based on the designing product and other conditions.
For detailed Antenna designing consideration, please refer to related antenna vendor's design recommendation. The antenna vendor will offer further technical support and tune their antenna characteristic to achieve successful GPS reception performance depending on the customer's design.

The GPS performance of MD231G

Search CH		**66CH**
Sensitivity (dBm)	**Tracking**	**-165**
	Acquisition	**-148(cold)/-163(hot)**
TTFF (SEC)	**Cold**	**32**
	Warm	**30**
	Hot	**1**
Position（m）	**2DRMS**	**10**
Power Consumption	**Tracking (Ma)**	**24**
	Acquisition (mA)	**40**
	Backup (uA)	**2**

3.12.BT Antenna

Only need add a BT antenna, you could use the BT of MD231G. The module contains a fully Bluetooth RF transceiver. The BT fully compliant with Bluetooth specification 3.0 + EDR and has the excellent interference rejection performance -95 dBm sensitivity

52	ANT_BT	Antenna of Bluetooth

3.13. SIM card interface

The MD231G contains a dedicated smart card interface to allow the MCU access to the SIM card. The SIM interface supports the functionality of the GSM Phase 1 specification and also supports the functionality of the new GSM Phase 2+ specification for FAST 64 kbps SIM (intended for use with a SIM application Tool-kit).
The SIM card interface circuitry of PMU meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband chipset to the SIM supply (Vsim). The bi-directional data bus is internal pull high with 10kohm resistor.
All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV of human body mode ESD. In order to ensure proper ESD protection, careful board layout is required.
The interface of SIM is as follow table：

Tbale12: The SIM pins on the Module

Num	Name	Function
20	SIM_IO	SIM card data output and input
21	SIM_CLK	SIM card clock output
19	SIM_RST	SIM card RESET output
22	VRSIM	Power supply for SIM card

Table 13: SIM Interface Electrical Specifications

SIM Voltage					
Output voltage (V_SIM)	Register VSIM_SEL=L	1.71	1.8	1.89	V
	Register VSIM_SEL=H	2.82	3.0	3.18	V
Output current (Isim_max)			20		mA
Line regulation				4	mV
Load regulation				15	mV

Parameter	**Conditions**	**Min.**	**Typical**	**Max.**	**Unit**

Interface to 3 V SIM Card					
Volrst	I = 20 µA			0.4	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.4	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
Interface to 1.8 V SIM Card					
Volrst	I = 20 µA			0.2*VSIM	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.2*VSIM	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
SIM Card Interface Timing					
SIO pull-up resistance to VSIM		8	10	12	kΩ
SRST, SIO rise/fall times	VSIM = 3, 1.8 V, load with 30 pF			1	µs
SCLK rise/fall times	VSIM = 3 V, CLK load with 30 pF			18	ns
	VSIM = 1.8 V, CLK load with 30 pF			50	ns
SCLK frequency	CLK load with 30 pF	5			MHz
SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%
SCLK propagation delay			30	50	ns

Following is a reference circuit about SIM interface. We recommend a Electrostatic discharge device ST (www.st.com) ESDA6V1W5 or ONSEMI (www.onsemi.com) SMF05C for "ESD ANTI".

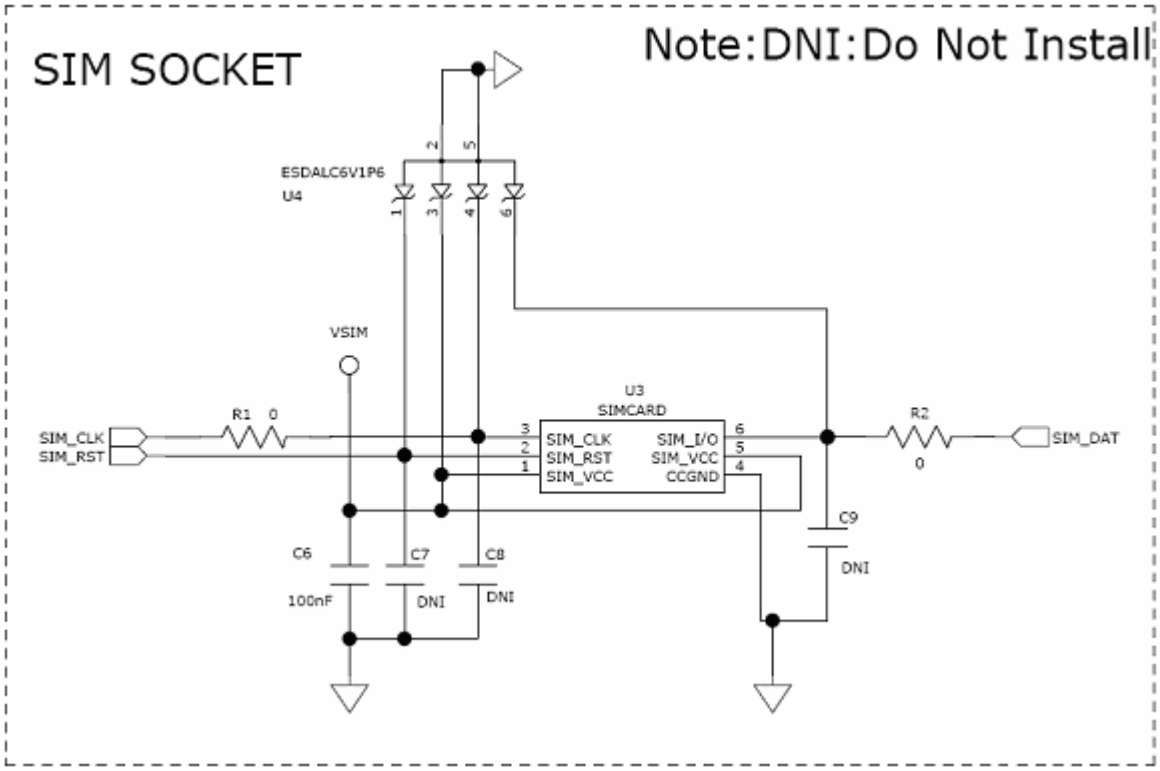


Figure4 The reference design of SIM Socket

3.14. Keypad Interface

The keypad can be divided into two parts: one is the keypad interface including 5 columns and 5 rows with one dedicated power-key, as shown in **Fig. 5.** the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 5 x 5 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed or released. This keypad can detect one or two key-pressed simultaneously with any combination. Since the key press detection depends on the HIGH or LOW level of the external keypad interface, if keys are pressed at the same time and there exists a key that is on the same column and the same row with the other keys, the pressed key cannot be correctly decoded. For example, if there are three key presses: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) are detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern retrieve the wrong information.

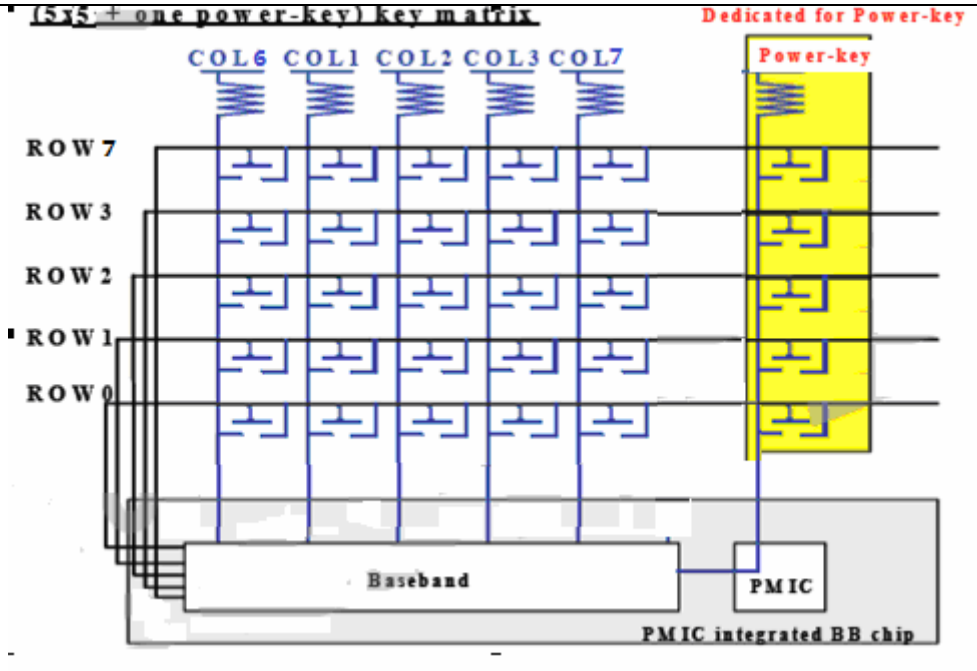


Figure5 The Typical Keypad Interface Circuit

3.15. LCD Interface

MD231G contains a versatile LCD controller which is optimized for multimedia applications. This controller supports many types of LCD modules and contains a rich feature set to enhance the functionality. These features are:

- Up to 480 x 320 resolution
- The internal frame buffer supports 8bpp indexed color, RGB565,RGB888,ARGB8888,PARGB8888 and YUYV422 format
- Supports 8-bpp (RGB332), 12-bpp (RGB444), 16-bpp (RGB565), 18-bit (RGB666) and 24-bit (RGB808) color depths
- 4 Layers Overlay with individual vertical and horizontal size, vertical and horizontal offset, source key, opacity and display rotation control(90°,180°, 270°, mirror and mirror then 90°, 180° and 270°)

For parallel LCD modules, this special LCD controller can reuse external memory interface or use dedicated 8/9-bit parallel interface to access them and 8080 type interface is supported. It can transfer the display data from the internal SRAM or external SRAM/Flash Memory to the off-chip LCD modules.

For serial LCD modules, this interface performs parallel to serial conversion and supports 8,9,16,18,24 and 32 bit interface. The serial interface may use four pins – LSCE#, LSDA, LSCK and LSA0 or three pins –LSCE#, LSDA, LSCK to enter commands and data. In 3 wire mode, an extra bit representing the LSA0 pin is transferred before the MSB of each transaction.

Figure 6 shows the timing diagram of this serial interface. When the block is idle, LSCK is forced LOW and LSCE# is forced HIGH. Once the data register contains data and the interface is enabled, LSCE# is pulled LOW and remain LOW for the duration of the transmission.

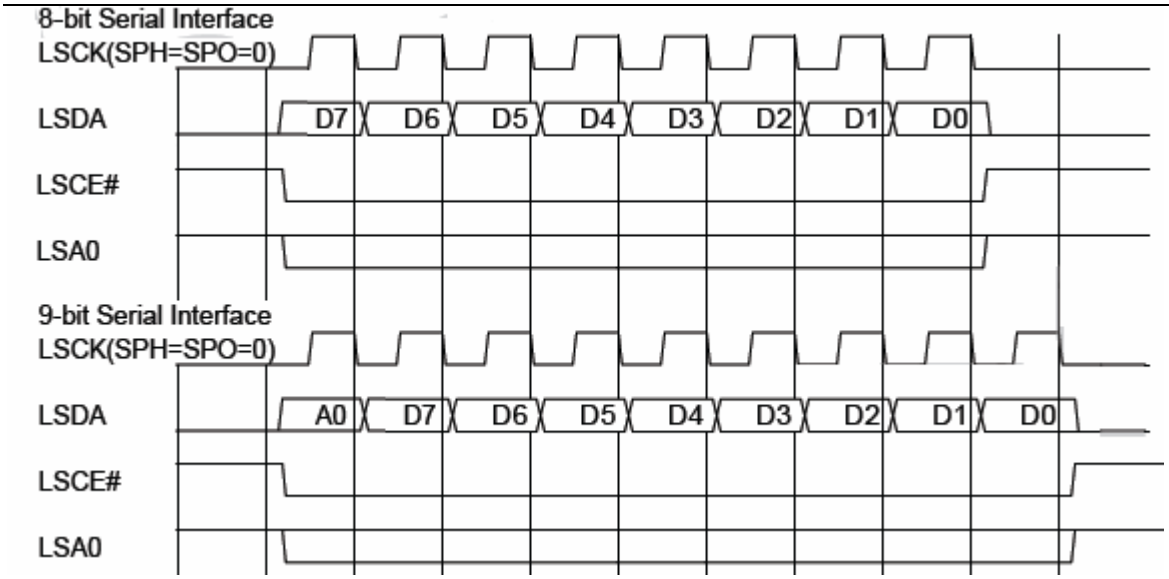


Figure 6 LCD Interface Transfer Timing Diagram

Tbale14: The LCD pins on the Module

Num	Name	Function
40	LRD_B	Parallel display interface Read Signal
39	LWR_B	Parallel display interface Write Signal
41	LPA0	Parallel display interface address output
37	LPCE0B	Parallel display interface chip select 0 output Serial display interface LSCE0
49	LCD_D0	Parallel display interface Data0 Serial display interface LSCK
48	LCD_D1	Parallel display interface Data1 Serial display interface LSA0
47	LCD_D2	Parallel display interface Data2 Serial display interface LSDA
46	LCD_D3	Parallel display interface Data3 Serial display interface LSDI
45	LCD_D4	Parallel display interface Data4
44	LCD_D5	Parallel display interface Data5
43	LCD_D6	Parallel display interface Data6
42	LCD_D7	Parallel display interface Data7
38	LRSTB	Parallel display interface Reset Signal
6	LPTE	Parallel display interface
5	LCD_D8	Parallel display interface Data7

3.16. Touch Panel

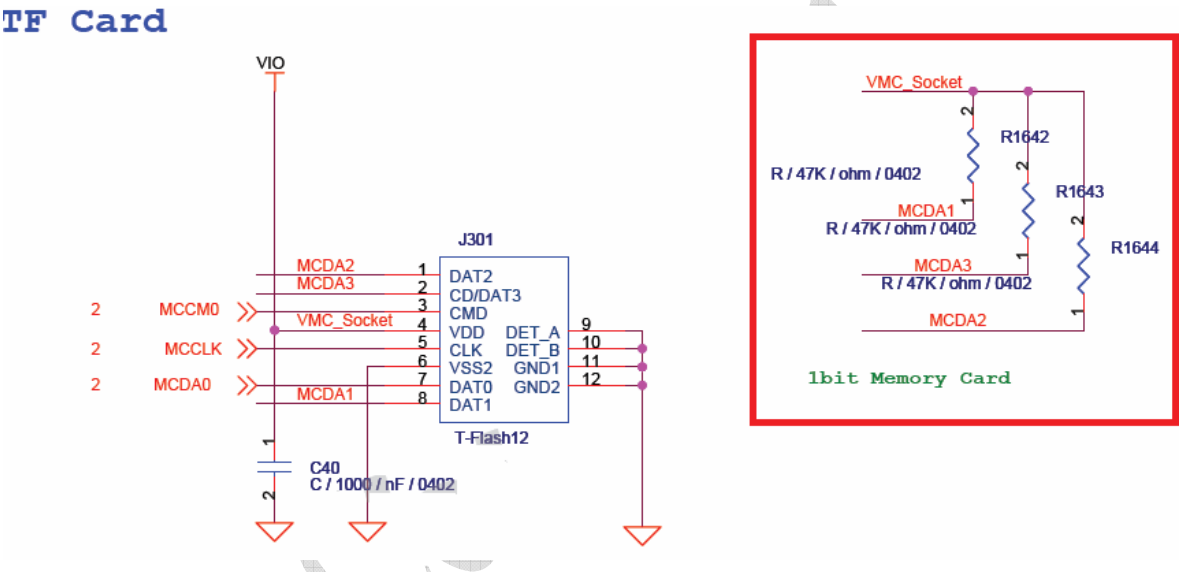
The Module of MD231G has a four lines R type touch panel. XM, YM, XP, YP.

74	**YP**	Touch panel Y-asis poisitive input
75	**XP**	Touch panel X-asis poisitive input
76	**XM**	Touch panel X-asis negative input
77	**YM**	Touch panel Y-asis negative input

3.17.SD/MMC Memory Card

The MD231G fully supports the SD memory Card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 as well as the MultiMediaCard (MMC) bus protocol as defined in MMC system specification version 4.1. Since SD Memory Card bus protocol is backward compatible to MMC bus protocol, the MD231G is capable of working well as the host on MMC bus under control of proper firmware. Hereafter, the MD231G is also abbreviated as SD/MMC controller.

Num	Name	Function
81	MCCLK	SD Serial Clock/Memory Stick Serial Clock
82	MCDA0	SD Serial Data IO 0/Memory Stick Serial Data IO
83	MCCM0	SD Command Output/Memory Stick Bus State Output
84	MCINS	SD Card Detect Input



MD231G also support 4bit mode, then KCOL7 use as MCDA1, KCOL6 use as MCDA2, and KROW7 use as MCDA3. For 4bit mode, R1642,R1643,R1644 should be NC.

3.18. RTC backup

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768KHz oscillator with an independent power supply. When the module is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor is used through the pin68 of VBACKUP. Figure 7 give the example diagram of the two ways. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g., 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

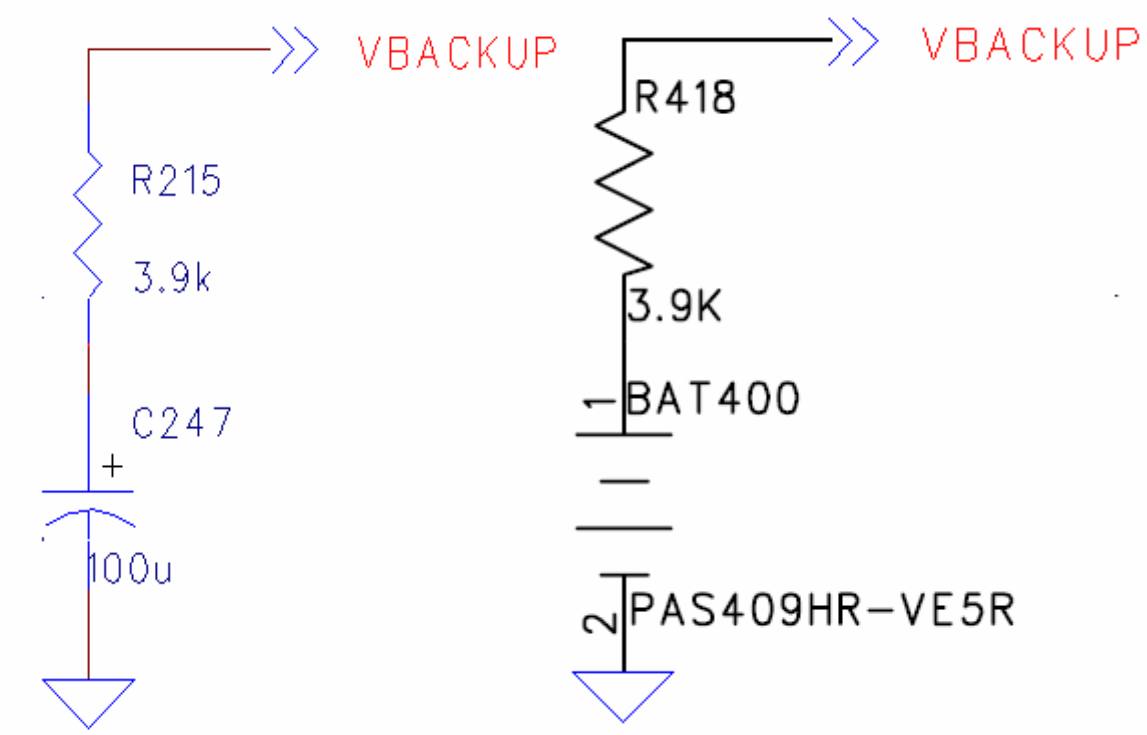


Figure7 The RTC battery diagram for the module

3.19. CAMERA

The camera of MD231G support YUV422 format image input and capable of processing image of size up to 0.3M pixels(Mediatek serial interface) and 2M pixels(w/o compression).

33	SDA	I2C data
34	SCL	I2C colck
53	CMPCLK	CMOS sensor master clock output
54	CMMCLK	CMOS sensor master clock output
55	CMPDN	CMOS sensor power down control
56	CMVSYNC	CMOS sensor vertical reference signal input
57	CMRST	CMOS sensor reset signal output
58	CMDAT7	CMOS sensor data input 7

59	CMDAT6	CMOS sensor data input 6
60	CMDAT5	CMOS sensor data input 5
61	CMDAT4	CMOS sensor data input 4
62	CMDAT3	CMOS sensor data input 3
63	CMDAT2	CMOS sensor data input 2
64	CMDAT1	CMOS sensor data input 1
65	CMDAT0	CMOS sensor data input 0
66	CMHSYNC	CMOS sensor horizontal reference signal input

***Important Notice: The CMPDN and CMRST are also used as system configure pin, so when used as IO, don't pull them high or low.**

3.20.GPIO and External Interrupt

MD231G module has several IO pins which are configurable according to customer's requirement. We can do custom software for users.

The external interrupts can be used for different kind of applications, mainly for event detections: detection of hand free connection, detection of hood opening, detection of battery charger connection.

Since the external event may be unstable in a certain period, a de-bounce mechanism is introduced to ensure the functionality. The circuitry is mainly used to verify that the input signal remains stable for a programmable number of periods of the clock. When this condition is satisfied, for the appearance or the disappearance of the input, the output of the de-bounce logic changes to the desired state. Note that, because it uses the 32 KHz slow clock for performing the de-bounce process, the parameter of de-bounce period and de-bounce enable takes effect no sooner than one 32 KHz clock cycle (~31.25us) after the software program sets them. However, the polarities of EINTs are clocked with the system clock. Any changes to them take effect immediately.

The ENT pins can be configurable to "EDGE/LEVEL" according to the external signal.

3.21.ADC

MD231G provides one auxiliary ADC (General purpose analog to digital converter.) as voltage input pin, which can be used to detect the values of some external items such as voltage、temperature etc. For module application, user can use AT command "AT+CADC#" to read the voltage value added on ADC pin.

The functional specifications of the auxiliary ADC are listed in the following table.

Table 19 The Functional specification of Auxiliary ADC

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FC	Clock Rate	0.1	1.0833	5	MHz
FS	Sampling Rate @ N-Bit			5/(N+1)	MSPS
	Input Swing	1.0		AVDD	V
T	Operating Temperature	-40		85	℃
	Current Consumption Power-up Power-Down		300 1		μA μA

3.22. USB

The usb of MD231G provides a USB function interface which complies with Universal Serial Bus Specification Rev 1.1. The USB device controller supports only full-speed (12Mbps) operation. It can make use of this widely available USB interface to transmit/receive data with USB hosts, typically PC/laptop.

3.23. Charger detect

Although the MD231G don't integrated the charge function, but the pin16 could be used to detect the charger input. When the voltage of this pin is above the VBAT, the module also could into charge power on mode.

Symbol	Descripton	condition	Min	Type	Max	Unit
	Charger detect-on range	PD	4.3		7	V

3.24. Digital Pin Electrical Characteristics

Important: Please take care of the power domin of MD251P/Q IO pins, not correct level voltage will damage the module.

About the digital pin electrical characteristics of MD231G, please reference the table 20.

Table 20: Module digital electrical characteristics

Name	Reset		Power Domain
	I/O	PD/PU	
SPI_MOSI	I	PD	DVDD28
NLD8	I	PD	DVDD18_EMI

LPTE	I	PD	DVDD18_EMI
KCOL6	I	PD	DVDD28
KROW3	I	PD	DVDD28
KCOL7	I	PD	DVDD28
KROW2	I	PD	DVDD28
KROW0	O	PU	DVDD28
KCOL3	I	PD	DVDD28
KCOL2	I	PD	DVDD28
KROW1	I	PD	DVDD28
KROW7	I	PD	DVDD28
KCOL1	I	PD	DVDD28
SDA	I	PD	DVDD28
SCL	I	PD	DVDD28
LPCE_B	O	\	DVDD18_EMI
LPRSTB	I	PD	DVDD18_EMI
LWR_B	I	PD	DVDD18_EMI
LRD_B	I	PD	DVDD18_EMI
LPA0	I	PD	DVDD18_EMI
NLD7	I	PD	DVDD18_EMI
NLD6	I	PD	DVDD18_EMI
NLD5	I	PD	DVDD18_EMI
NLD4	I	PD	DVDD18_EMI
NLD3	I	PD	DVDD18_EMI
NLD2	I	PD	DVDD18_EMI
NLD1	I	PD	DVDD18_EMI
NLD0	I	PD	DVDD18_EMI
UTXD1	O	\	DVDD28
URXD1	I	PU	DVDD28
CMPCLK	I	PD	DVDD28
CMMCLK	I	PD	DVDD28
CMPDN	I	\	DVDD28
CMVSYNC	I	PD	DVDD28

CMRST	I	PD	DVDD28
CMDAT7	I	PD	DVDD28
CMDAT6	I	PD	DVDD28
CMDAT5	I	PD	DVDD28
CMDAT4	I	PD	DVDD28
CMDAT3	I	PD	DVDD28
CMDAT2	I	PD	DVDD28
CMDAT1	I	PD	DVDD28
CMDAT0	I	PD	DVDD28
CMHSYNC	I	PD	DVDD28
UTXD2	I	PD	DVDD28
URXD2	I	PD	DVDD28
MCCLK	I	PD	DVDD33_MSDC
MCDA0	I	PD	DVDD33_MSDC
MCCM0	I	PD	DVDD33_MSDC
MCINS	I	PD	DVDD18_EMI
EINT0	I	PD	DVDD28
SPI_MISO	I	PD	DVDD28
SPI_SCK	I	PD	DVDD28
SPI_CS	I	PD	DVDD28

About the digital IO LDO (VIO) is a regulator that could source 100mA (max) with 2.8V output voltage. It supplies the baseband circuitry of the Module. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO. Table21 show the electrical characteristics of VIO.

Table 21 VIO electrical characteristics

VBAT = 3.4 V ~ 4.6 V, minimum loads applied on all outputs, unless other noted. Typical values are at TA = 25 °C.

Parameter	Conditions	Min.	Typical	Max.	Unit
Digital IO Voltage					
Output voltage (V_IO)		2.7	2.8	2.9	V
Output current (Iio_max)			**20**		mA
Line regulation				5	mV
Load regulation				30	mV

3.25. Module sleep mode control

Our Module support two ways to control module enter sleep mode or not:

1) Hardware control method: **DSR** is used for hardware sleep mode control.
   LOW Level: disable module enter sleep mode;
   HIGH Level: enable module enter sleep mode.
2) Software control method: AT command "AT+ESLP"
   "AT+ESLP=0": disable module enter sleep mode;
   "AT+ESLP=1": enable module enter sleep mode.

NOTE1: Module default software value is disable enter sleep mode.
NOTE2: If module enter sleep mode, the AT command can not be sent to module normally.

3.26.Behaviors of the RING indication line

MD231G: One IO (through software define) could be used for Ring indication when network event. The working state of this pin is listed in following table:

Table 23: The Behaviors of the RING line

State	RI respond
Standby	High
Voice calling	Change low, then: 1) Change to high when establish calling. 2) Sender hang up, change to high.
SMS	When receive SMS, The ring will change to LOW and hold LOW level at least 200 ms, then change to HIGH.

3.27.Network status indication LED lamp

MD231G: One IO pin (through software define) could be used to drive a network status indication LED lamp. The working state of this pin is listed in following table:

Table 23: Working state of network status indication LED pin

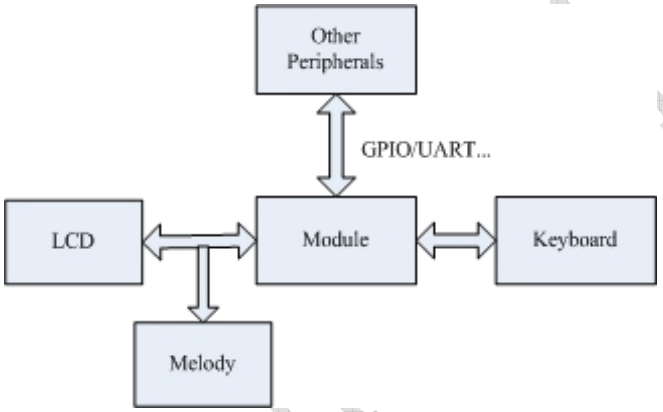
State	Module function
Off	Module is not running
64ms On/800ms Off	Module does not find the network
64ms On/3000ms Off	Module find the network
64ms On/300ms Off	GPRS communication

4. Software application

The module can be used in master mode and slave mode.

4.1. Master mode (such as application for fixed wireless phone)

In master mode, the module acted as main board of mobile terminal. The LCD or melody processor can be connected to the module via data and address bus. Users can control the module via keyboard and the application software can be customized according to requirement.



Please get schematic information from chap 6.2.
Please get detail information from refer[10]

4.2. Slave mode (standard GSM/GPRS module application)

In slave mode, the module communicated with master MCU via UART interface using AT commands.
Please get schematic information from chap 6.1.

4.2.1. AT command

Please get detail information from refer[11]

4.2.2. The hyper terminal configure method

User can control the MD231G module using hyper terminal to send AT Command. The configuration in hyper terminal:
Bits per second： 115200 (depends on SW)

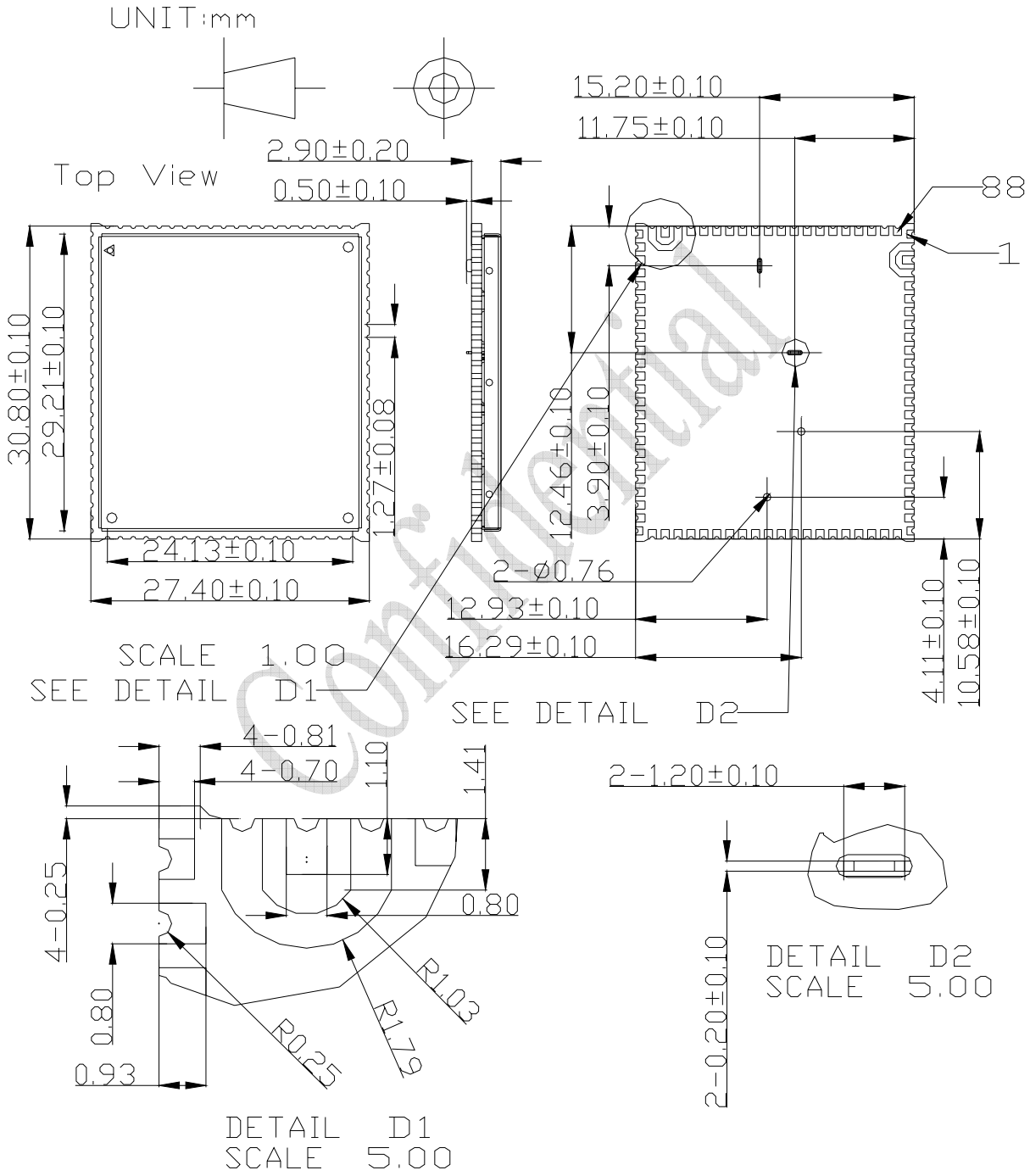
Data bits: 8
Parity: None
Stop bits: 1
Flow control: None

4.2.3. TCP/IP protocol

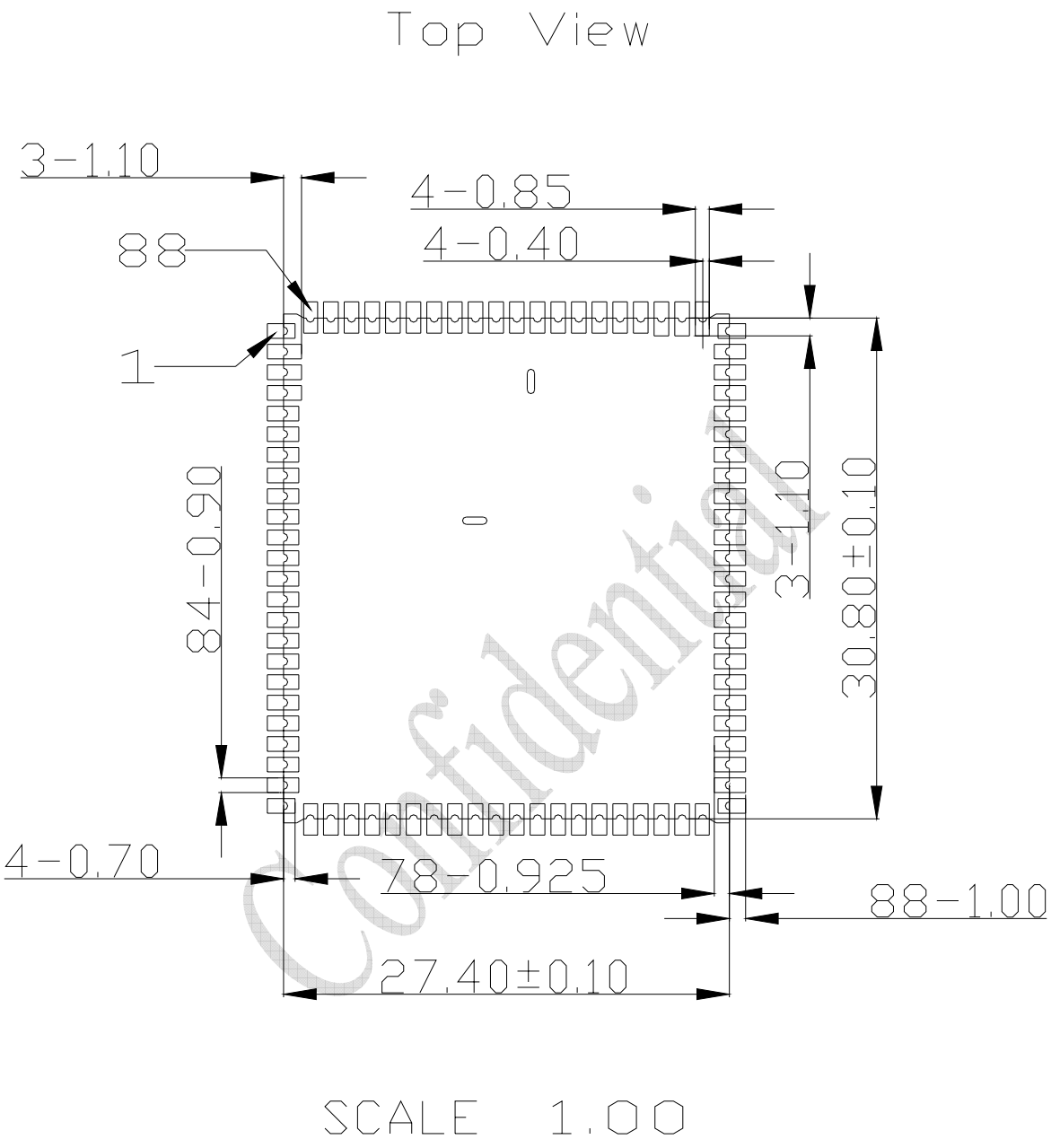
The module can support TCP/IP protocol. Please get detail information from reference [11].

5. Mechanics

5.1. PACKAGE DIMENSIONS

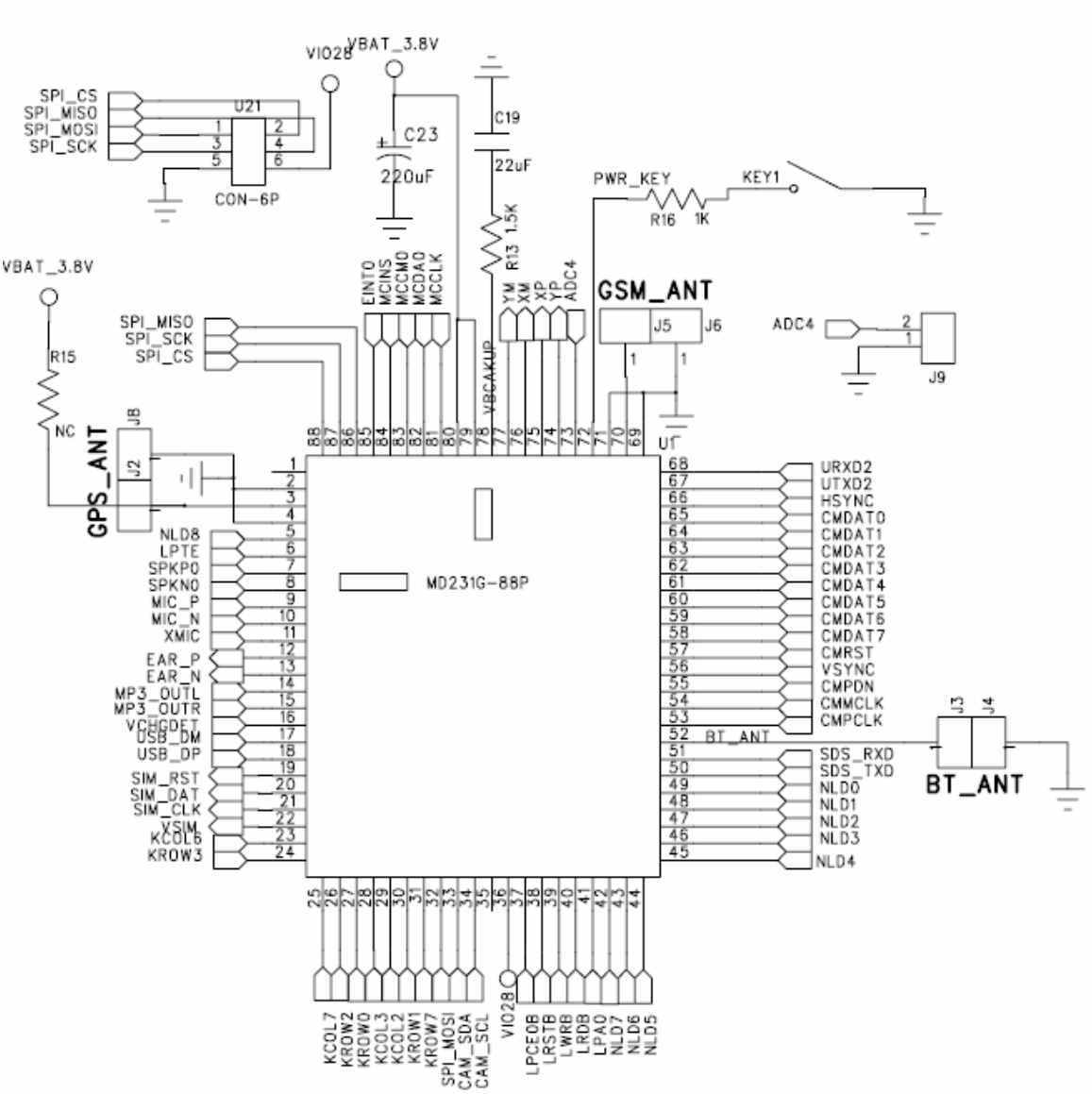


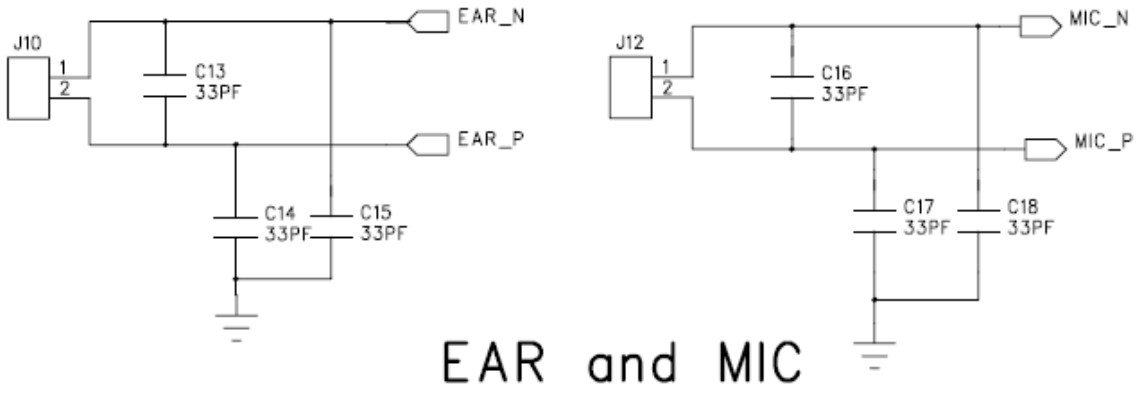
5.2. SOLDERING FOOTPRINT



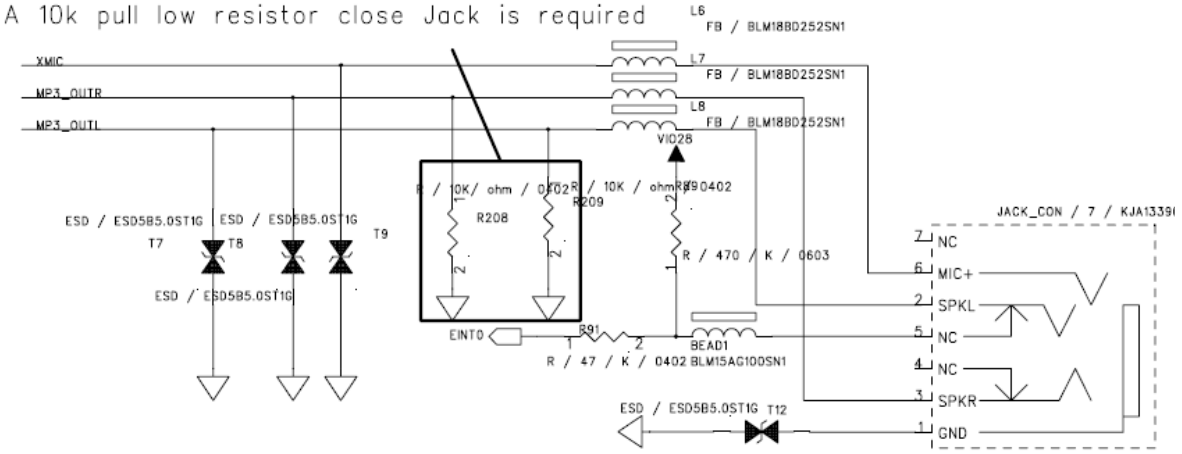
6. Interface board Reference EVB

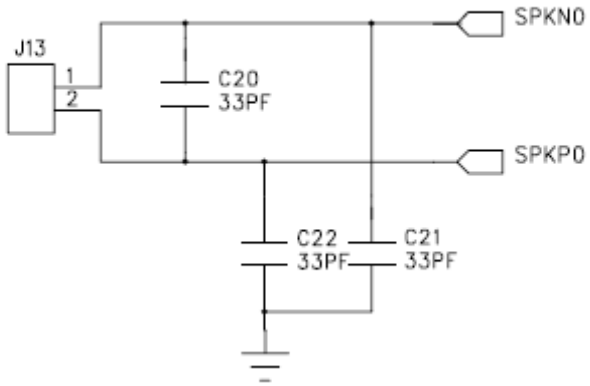
6.1 Standard GSM/GPRS module

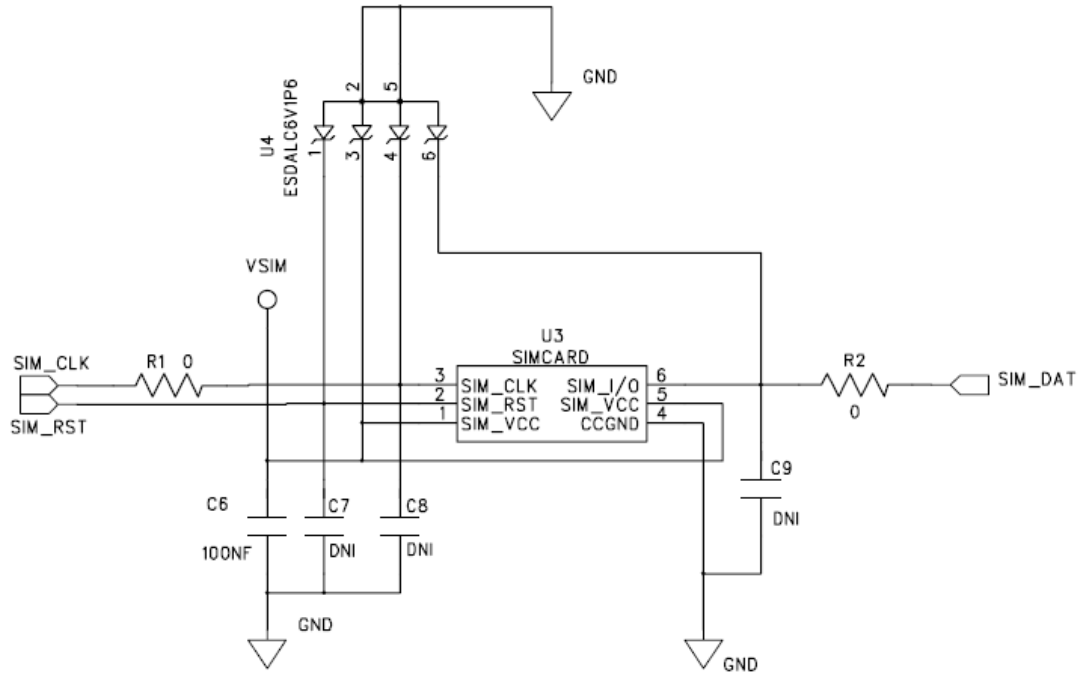



J10
1
2
C13
33PF
EAR_N
EAR_P
C14
33PF
C15
33PF
J12
1
2
C16
33PF
MIC_N
MIC_P
C17
33PF
C18
33PF

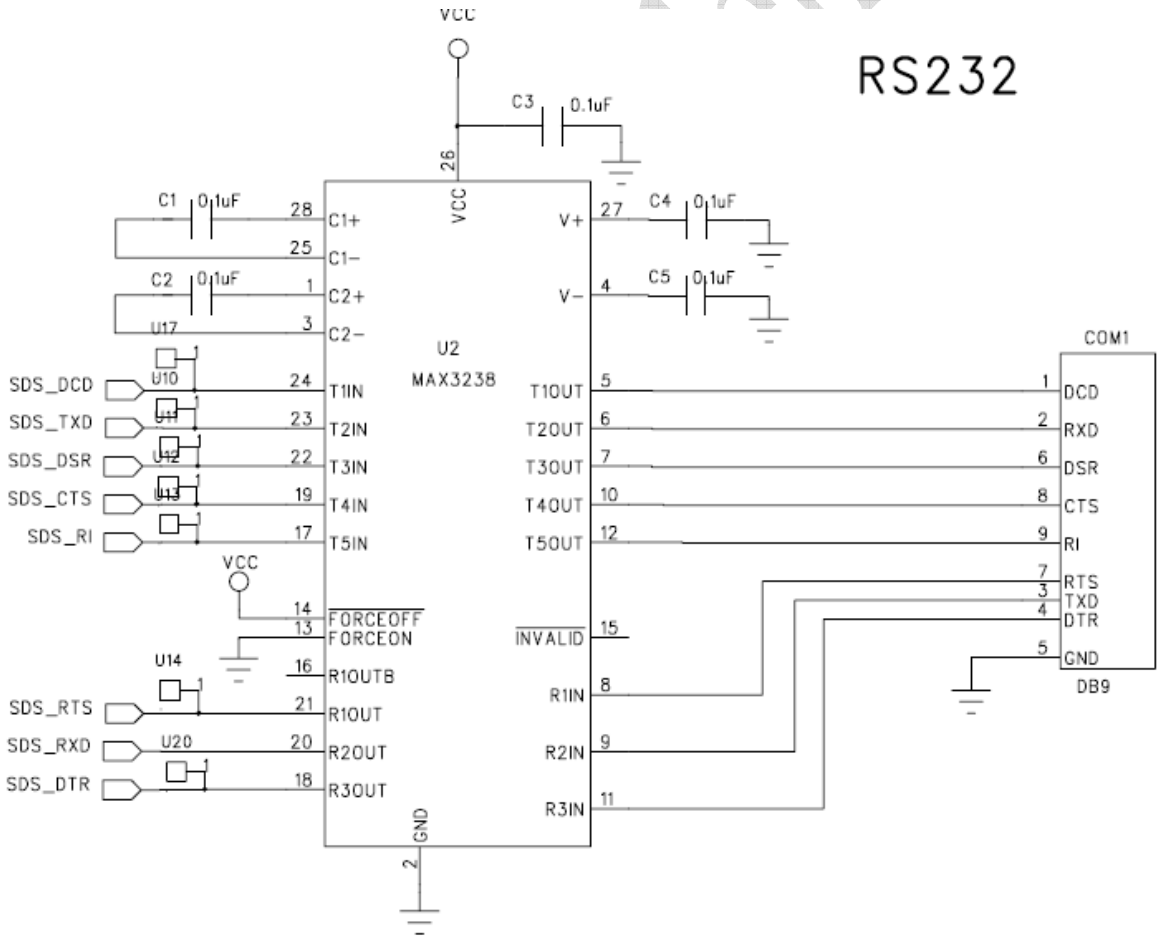
EAR and MIC


A 10k pull low resistor close Jack is required
L6
FB / BLM18BD252SN1
L7
FB / BLM18BD252SN1
L8
FB / BLM18BD252SN1
XMIC
MP3_OUTR
MP3_OUTL
VIO28
R / 10K/ ohm / 0402
R208
R / 10K / ohm / 0402
R209
R / 470 / K / 0603
ESD / ESD5B5.0ST1G
T7
T8
T9
ESD / ESD5B5.0ST1G
ESD / ESD5B5.0ST1G
EINT0
R91
R / 47 / K / 0402
BEAD1
BLM15AG100SN1
JACK_CON / 7 / KJA13391
7 NC
6 MIC+
2 SPKL
5 NC
4 NC
3 SPKR
1 GND
ESD / ESD5B5.0ST1G
T12


J13
1
2
C20
33PF
SPKN0
SPKP0
C22
33PF
C21
33PF

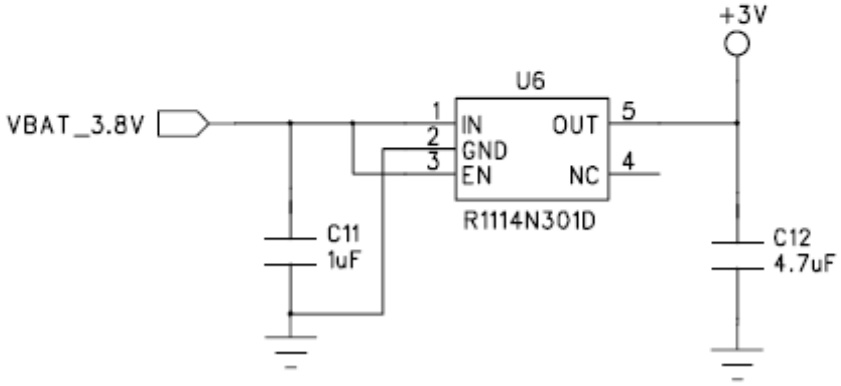


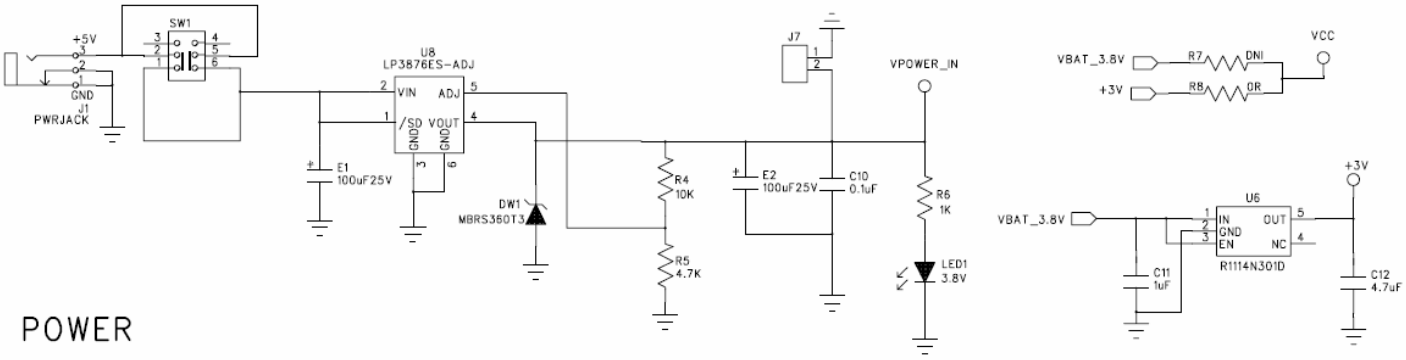
SIM SOCKET



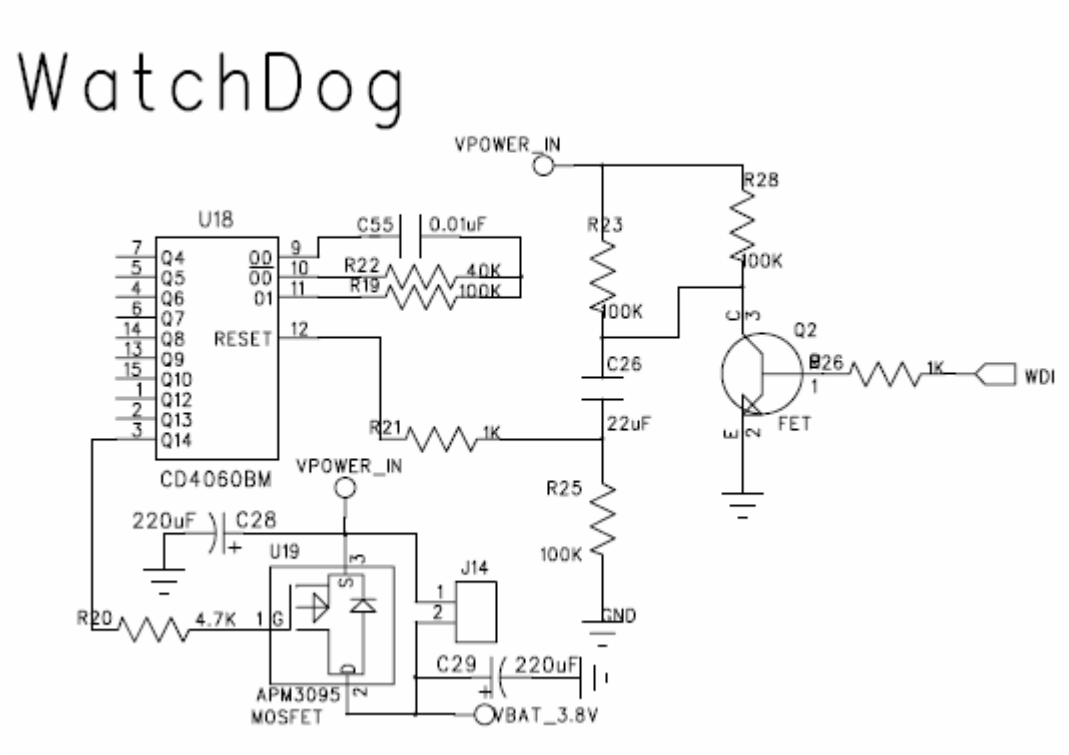
RS232

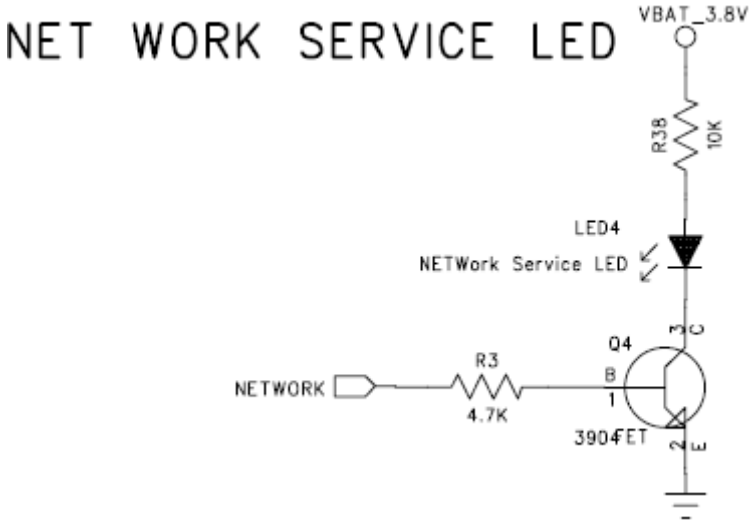

VCC
VBAT_3.8V
R7
DNI
+3V
R8
0R

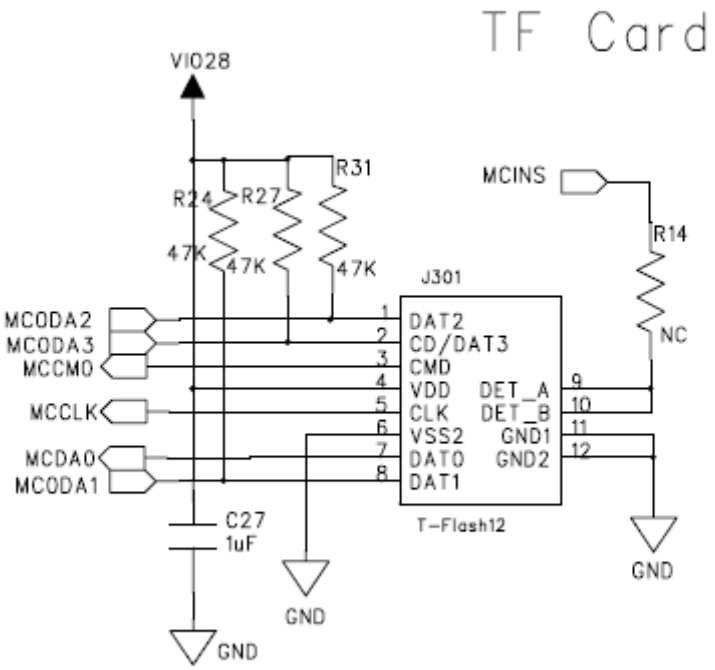

+3V
U6
VBAT_3.8V
1
IN
OUT
5
2
GND
3
EN
NC
4
R1114N301D
C11
1uF
C12
4.7uF

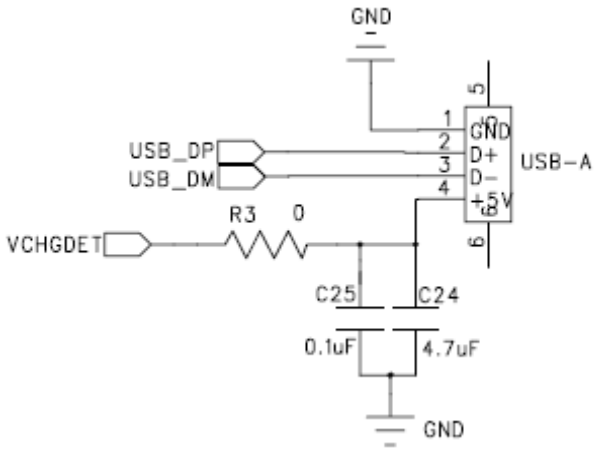

SW1
+5V
GND
J1
PWRJACK
U8
LP3876ES-ADJ
VIN
ADJ
/SD
VOUT
GNDS
GND
E1
100uF25V
DW1
MBRS360T3
R4
10K
R5
4.7K
J7
VPOWER_IN
E2
100uF25V
C10
0.1uF
R6
1K
LED1
3.8V
VBAT_3.8V
R7
DNI
VCC
+3V
R8
0R
U6
IN
OUT
GND
EN
NC
R1114N301D
C11
1uF
C12
4.7uF

POWER


WatchDog
VPOWER_IN
R28
100K
U18
C55
0.01uF
R23
100K
R22
40K
R19
100K
Q2
C26
R26
1K
WDI
RESET
22uF
R21
1K
FET
CD4060BM
VPOWER_IN
R25
100K
220uF
C28
U19
J14
R20
4.7K
GND
C29
220uF
APM3095
MOSFET
VBAT_3.8V


NET WORK SERVICE LED
VBAT_3.8V
R38
10K
LED4
NETWork Service LED
Q4
R3
NETWORK
4.7K
3904FET


TF Card
VIO28
R31
R24
R27
47K
47K
47K
MCINS
R14
NC
J301
MCDA2
MCDA3
MCCM0
MCCLK
MCDA0
MCDA1
DAT2
CD/DAT3
CMD
VDD
CLK
VSS2
DAT0
DAT1
DET_A
DET_B
GND1
GND2
T-Flash12
C27
1uF
GND
GND
GND


GND
USB_DP
USB_DM
GND
D+
D-
+5V
USB-A
R3 0
VCHGDET
C25
C24
0.1uF
4.7uF
GND

7. PCB Check List

7.1 The PCB Trace Design Flow Sequence:

1. Place all the ground vias on the component relevant pads
2. Route the VBAT trace to Module
3. Route the VIO net
4. Route the RF striplines and micro-striplines
5. Route the audio traces
6. Route the digital traces

7.2 The PCB Layout check point

Power Supply

1. All power supply filters should be put near the relevant components. And the order is the smallest capacitance is the nearest.
2. The power supply traces, such as VBAT, Vcharge, should be wide and short. The Capacitors for Vbat_RF should be placed near Power Pin.
3. The voltage of V_BAT is often changing from time to time. So it is better to keep other power supply lines far away from V_BAT, such as V_IO, V_SIM…
4. The width of VBAT should not be less then 80mil.

Antenna(GSM&GPS)

1. The line of Antenna should be **short** to make the insert loss lower and routed as RF line strictly to keep **50ohm** matching.
2. It's better to put the antenna pad on the edge of the PCB.

Audio

1. EAR+ and EAR-, MIC+ and MIC-, LINE_I+ and LINE_I-, LINE_O+ and LINE_O- should be parallel and symmetry, respectively.
2. High speed lines should not go below these audio lines.

SIM

1. SIM test is very sensitive. While PCB layout, the SIM trace, such as V_SIM, SIM_DATA, SIM_RST, SIM_CLK should be kept clean. And reserve a R-C filter location at the side of SIM socket for above lines respectively.

2. It's better to put the SIM socket near the Module.

USB

1. USB D+ and USBD- should be parallel and symmetry, respectively and should been strictly to keep **90ohm** matching.

2. USB line should be protected below and both side by GND.

Camera

1. CMMCLK and CMPCLK should be protect by GND

2. Camera signals route together is better.

Memory Card

1. MCCLK signal line should protect by GND

2. Memory card signals are better to route toghter.

LCM

1. LWR_B should be protected by GND

2. It's better to route LCM signals together and protected by GND.

ESD Protect

1. ESD component should be put close to the related connector / jack.

2. Some pins of Module also should have ESD components, especially the pin of SIM card, TF-Card and USB.

Ground

1. The more GND Via, the better! Make sure enough GND Via to the Ground.

2. If possible, the ground layer should not be divided. Keep at least one ground layer completed.

3. Distinguish the digital GND pin and analog GND pin for IA chip and make different GND plane for them respectively.

Others

- The Keypad lines should not been routed up the antenna, especially the key_return lines.

- Components of Microphone input circuit should be put as symmetry as possible.

- The RF traces should be carefully calculated.

- CLK_OUT signal line should protect by GND.