Preliminary

OKI Semiconductor

This version: Jun. 1998

MD56V62800A

4-Bank × 2,097,152-Word × 8-Bit SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The MD56V62800A is a 4-bank × 2,097,152-word × 8-bit synchronous dynamic RAM, fabricated in Oki's CMOS silicon-gate process technology. The device operates at 3.3 V. The inputs and outputs are LVTTL compatible.

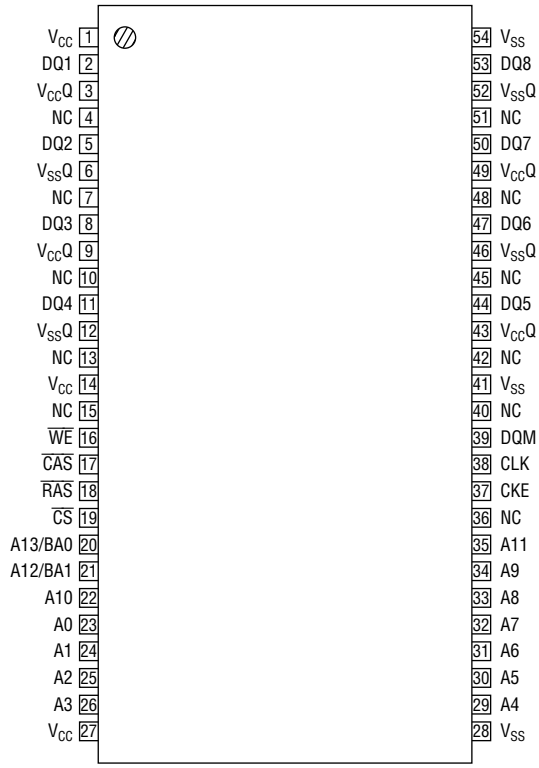
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4-bank × 2,097,152-word × 8-bit configuration
- 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible
- Refresh : 4096 cycles/64 ms
- Programmable data transfer mode
  – $\overline{\text{CAS}}$ latency (1, 2, 3)
  – Burst length (1, 2, 4, 8, full page)
  – Data scramble (sequential, interleave)
- Burst read single bit write capability
- CBR auto-refresh, Self-refresh capability
- Package:
  54-pin 400 mil plastic TSOP (Type II) (TSOPII54-P-400-0.80-K) (Product : MD56V62800A-xxTA)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Max. Frequency	Access Time (Max.)	
		t_{AC2}	t_{AC3}
MD56V62800A-8	125 MHz	10 ns	6 ns
MD56V62800A-10	100 MHz	9 ns	9 ns

PIN CONFIGURATION (TOP VIEW)



54-Pin Plastic TSOP (II)
(K Type)

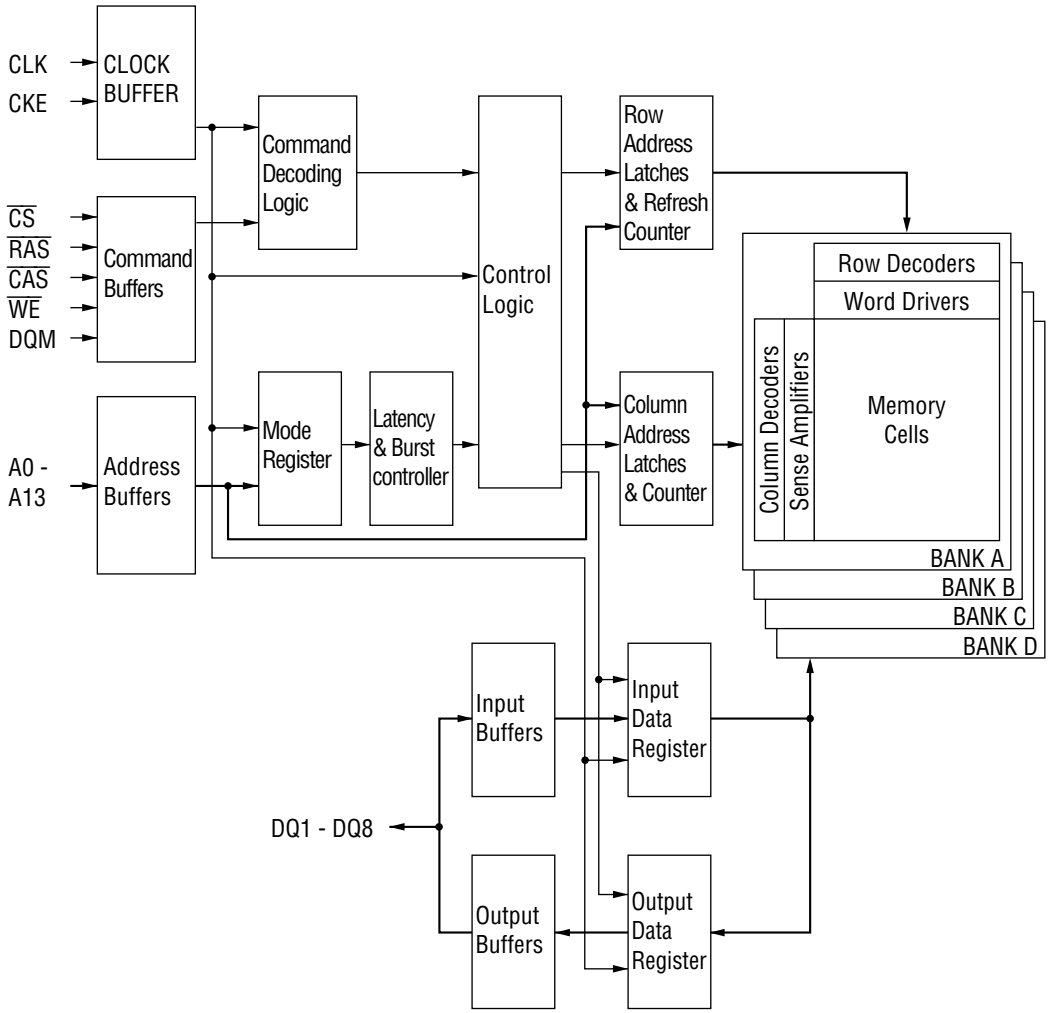
Pin Name	Function	Pin Name	Function
CLK	System Clock	DQM	Data Input/Output Mask
$\overline{CS}$	Chip Select	DQi	Data Input/Output
CKE	Clock Enable	V_{CC}	Power Supply (3.3 V)
A0 - A11	Address	V_{SS}	Ground (0 V)
A12, A13	Bank Select Address	$V_{CC}Q$	Data Output Power Supply (3.3 V)
$\overline{RAS}$	Row Address Strobe	$V_{SS}Q$	Data Output Ground (0 V)
$\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Write Enable		

Note: The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}Q$ pin.
The same GND voltage level must be provided to every V_{SS} pin and $V_{SS}Q$ pin.

PIN DESCRIPTION

CLK	Fetches all inputs at the "H" edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE and DQM.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 – RA11 Column address: CA0 – CA8
A12, A13 (BA1, BA0)	Bank Access pins. These pins are dedicated to select one of 4 banks.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
DQM	Masks the read data of two clocks later when DQM is set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM is set "H" at the "H" edge of the clock signal.
DQi	Data inputs/outputs are multiplexed on the same pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Voltages referenced to V_{SS})

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to V_{CC} + 0.5	V
V_{CC} Supply Voltage	V_{CC}, $V_{CC}Q$	–0.5 to 4.6	V
Storage Temperature	T_{stg}	–55 to 150	°C
Power Dissipation	P_D*	1	W
Short Circuit Current	I_{OS}	50	mA
Operating Temperature	T_{opr}	0 to 70	°C

*: Ta = 25°C

Recommended Operating Conditions

(Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}, $V_{CC}Q$	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 2.0	V
Input Low Voltage	V_{IL}	V_{CC} – 2.0	—	0.8	V

Capacitance

(V_{CC} = 3.3 V, V_{bias} = 1.4 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	C_{CLK}	2.5	4	pF
Input Capacitance (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, A0 - A13)	C_{IN}	2.5	5	pF
Input/Output Capacitance (DQ1 - DQ8)	C_{OUT}	4	6.5	pF

DC Characteristics

Parameter	Symbol	Condition			Version				Unit	Note
		Bank	CKE	Others	-8		-10			
					Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	—	—	I_{OH} = –2 mA	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	—	—	I_{OL} = 2 mA	—	0.4	—	0.4	V	
Input Leakage Current	I_{LI}	—	—	—	–5	5	–5	5	µA	
Output Leakage Current	I_{LO}	—	—	—	–5	5	–5	5	µA	
Average Power Supply Current (Operating)	$I_{CC}1$	One Bank Active	CKE ≥ V_{IH}	t_{CC} = min t_{RC} = min No Burst	—	125	—	115	mA	1, 2
	$I_{CC}1D$	Both Banks Active	CKE ≥ V_{IH}	t_{CC} = min t_{RC} = min t_{RRD} = min No Burst	—	175	—	165	mA	1, 2
Power Supply Current (Stand by)	$I_{CC}2$	Both Banks Precharge	CKE ≥ V_{IH}	t_{CC} = min	—	30	—	30	mA	3
Average Power Supply Current (Clock Suspension)	$I_{CC}3S$	Both Banks Active	CKE ≤ V_{IL}	t_{CC} = min	—	6	—	6	mA	2
Average Power Supply Current (Active Stand by)	$I_{CC}3$	One Bank Active	CKE ≥ V_{IH}, $\overline{CS}$ ≥ V_{IH}	t_{CC} = min	—	60	—	50	mA	3
Power Supply Current (Burst)	$I_{CC}4$	Both Banks Active	CKE ≥ V_{IH}	t_{CC} = min	—	165	—	155	mA	1, 2
Power Supply Current (Auto-Refresh)	$I_{CC}5$	One Bank Active	CKE ≥ V_{IH}	t_{CC} = min t_{RC} = min	—	185	—	185	mA	2
Average Power Supply Current (Self-Refresh)	$I_{CC}6$	Both Banks Precharge	CKE ≤ 0.2 V	t_{CC} = min	—	2	—	2	mA	
Average Power Supply Current (Power down)	$I_{CC}7$	Both Banks Precharge	CKE ≤ V_{IL}	t_{CC} = min	—	2	—	2	mA	

Notes: 1. Measured with outputs open.
2. The address and data can be changed once or left unchanged during one cycle.
3. The address and data can be changed once or left unchanged during two cycles.

Mode Set Address Keys

Write Burst Length		$\overline{CAS}$ Latency				Burst Type		Burst Length				
A9	Write Burst Length	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Burst Write	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single Bit Write	0	0	1	1	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

Notes: 1. A7, A8, A10, A11, A12 and A13 should stay "L" during mode set cycle.
2. When A9 = 1, a burst length for write operation is always 1 regardless of the burst lengths set by A0, A1 and A2.

POWER ON SEQUENCE

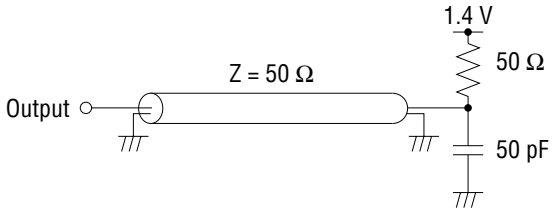
1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 µs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply a CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

AC Characteristics

Note 1, 2

Parameter		Symbol	MD56V62800A-8		MD56V62800A-10		Unit	Note
			Min.	Max.	Min.	Max.		
Clock Cycles Time	CL = 3	t_{CC}	8	—	10	—	ns	
	CL = 2		12	—	15	—	ns	
	CL = 1		24	—	30	—	ns	
Access Time from Clock	CL = 3	t_{AC}	—	6	—	9	ns	3, 4
	CL = 2		—	10	—	9	ns	3, 4
	CL = 1		—	22	—	27	ns	3, 4
Clock "H" Pulse Time		t_{CH}	3	—	3	—	ns	
Clock "L" Pulse Time		t_{CL}	3	—	3	—	ns	
Input Setup Time		t_{SI}	2	—	3	—	ns	
Input Hold Time		t_{HI}	1	—	1	—	ns	
Output Low Impedance Time from Clock		t_{OLZ}	3	—	3	—	ns	
Output High Impedance Time from Clock		t_{OHZ}	—	8	—	8	ns	
Output Hold from Clock		t_{OH}	3	—	3	—	ns	3
$\overline{RAS}$ Cycle Time		t_{RC}	80	—	90	—	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	30	—	30	—	ns	
$\overline{RAS}$ Active Time		t_{RAS}	50	100,000	60	100,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	—	30	—	ns	
Write Recovery Time		t_{WR}	8	—	10	—	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		t_{RRD}	16	—	20	—	ns	
Refresh Time		t_{REF}	—	64	—	64	ms	
Power-down Exit Set-up Time		t_{PDE}	t_{SI} + 1 CLK	—	t_{SI} + 1 CLK	—	ns	
Input Level Transition Time		t_T	—	3	—	3	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Min.)		l_{CCD}	1		1		Cycle	
Clock Disable Time from CKE		l_{CKE}	1		1		Cycle	
Data Output High Impedance Time from DQM		l_{DOZ}	2		2		Cycle	
Data Input Mask Time from DQM		l_{DOD}	0		0		Cycle	
Data Input Time from Write Command		l_{DWD}	0		0		Cycle	
Data Output High Impedance Time from Precharge Command	CL = 3	l_{ROH}	3		3		Cycle	
	CL = 2		2		2		Cycle	
	CL = 1		1		1		Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)		l_{MRD}	3		3		Cycle	
Write Command Input Time from Output		l_{OWD}	2		2		Cycle	

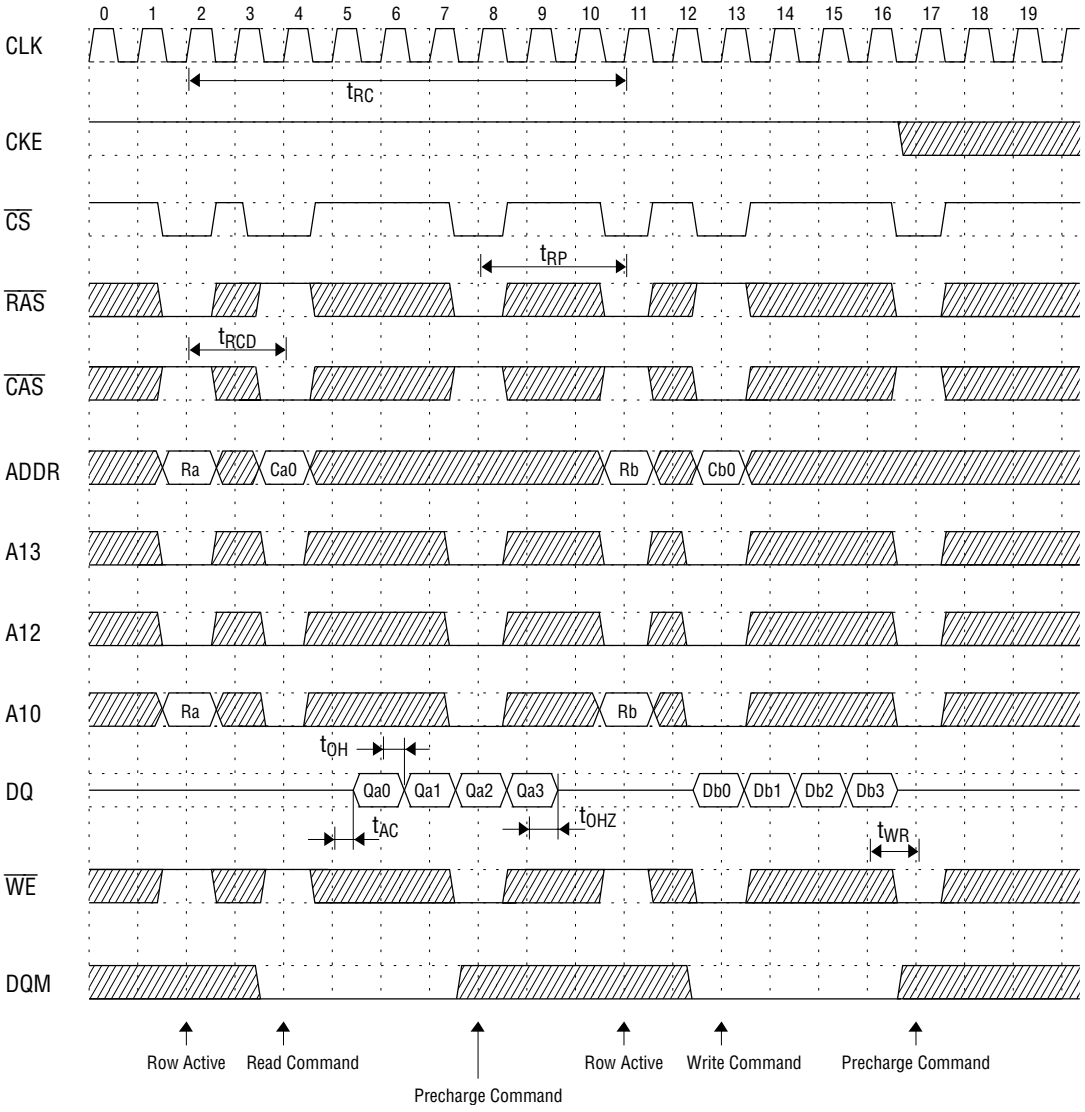
Notes : 1. AC measurements assume that t_T = 1 ns.
2. The reference level for timing of input signals is 1.4 V.
3. Output load.



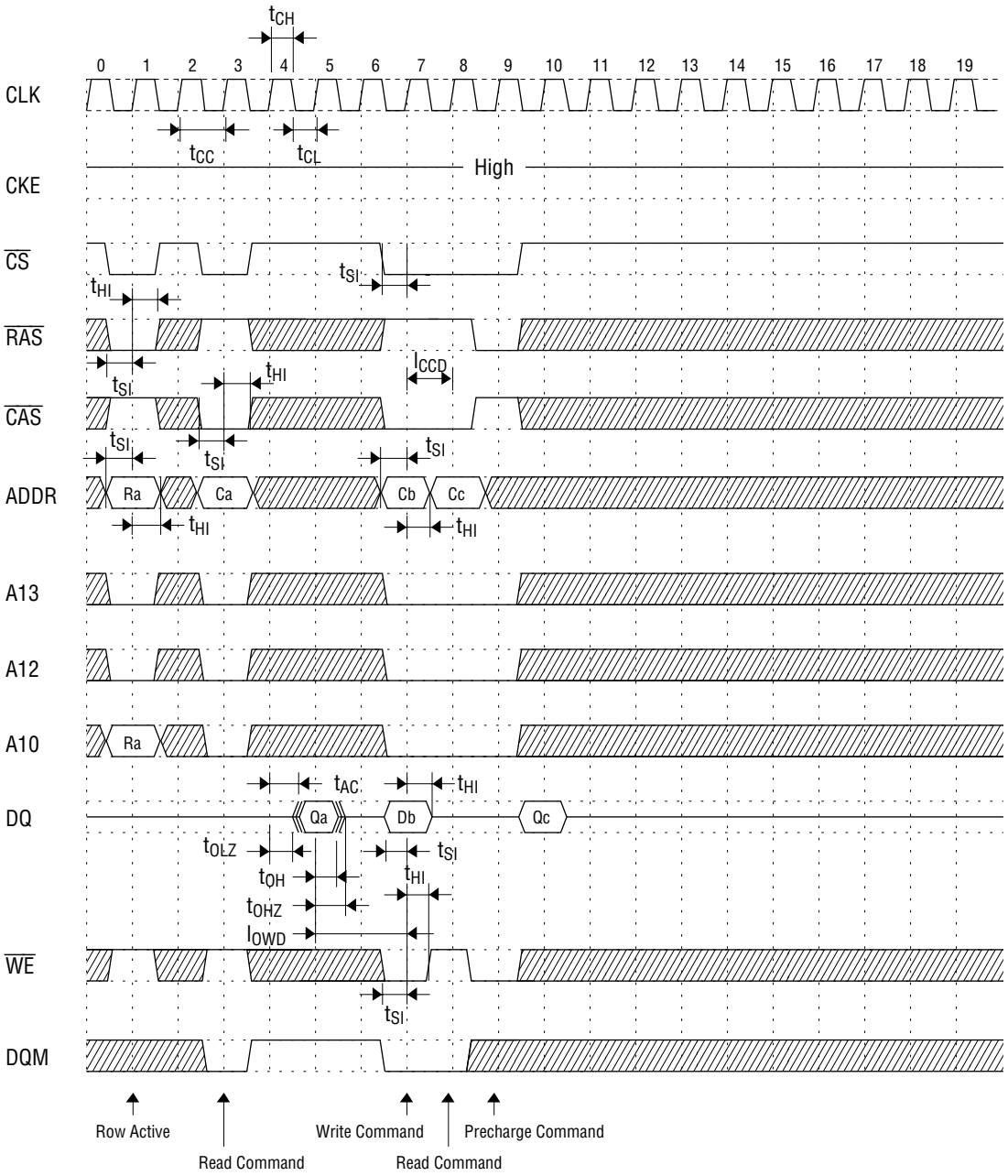
4. The access time is defined at 1.4 V.
5. If t_T is longer than 1 ns, then the reference level for timing of input signals is V_{IH} and V_{IL}.

TIMING WAVEFORM

Read & Write Cycle (Same Bank) @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Single Bit Read-Write-Read Cycle (Same Page) @ $\overline{CAS}$ Latency = 2, Burst Length = 4



***Notes:** 1. When $\overline{CS}$ is set "High" at a clock transition from "Low" to "High", all inputs except CKE and DQM are invalid.

2. When issuing an active, read or write command, the bank is selected by A12 and A13.

A12	A13	Active, read or write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

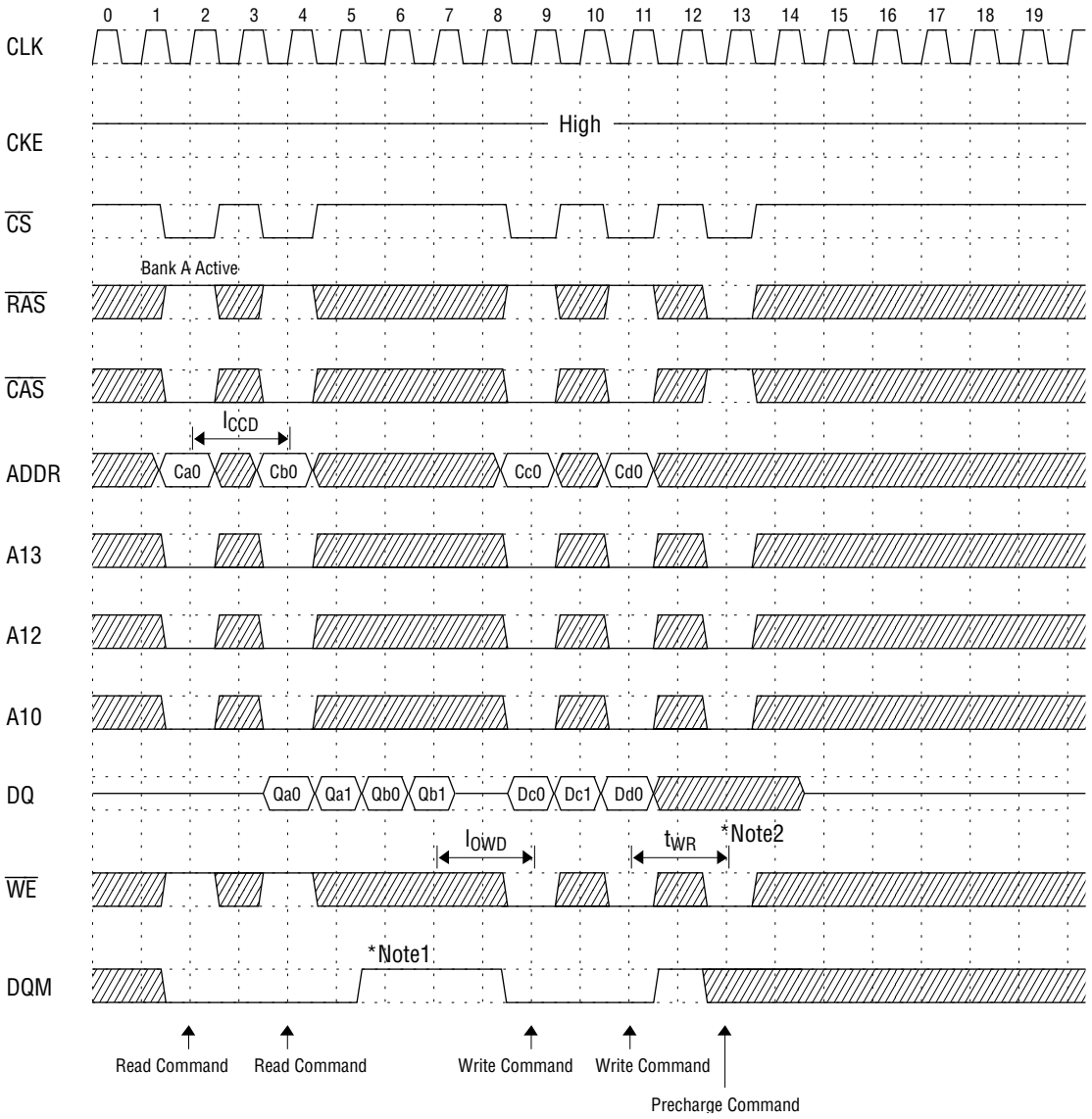
A10	A12	A13	Operation
0	0	0	After the end of burst, bank A holds the idle status.
1	0	0	After the end of burst, bank A is precharged automatically.
0	0	1	After the end of burst, bank B holds the idle status.
1	0	1	After the end of burst, bank B is precharged automatically.
0	1	0	After the end of burst, bank C holds the idle status.
1	1	0	After the end of burst, bank C is precharged automatically.
0	1	1	After the end of burst, bank D holds the idle status.
1	1	1	After the end of burst, bank D is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A10, A12 and A13 inputs.

A10	A12	A13	Operation
0	0	0	Bank A is precharged.
0	0	1	Bank B is precharged.
0	1	0	Bank C is precharged.
0	1	1	Bank D is precharged.
1	X	X	All banks are precharged.

5. The input data and the write command are latched by the same clock (Write latency = 0).
6. The output is forced to high impedance by (1 CLK + t_{OHZ}) after DQM entry.

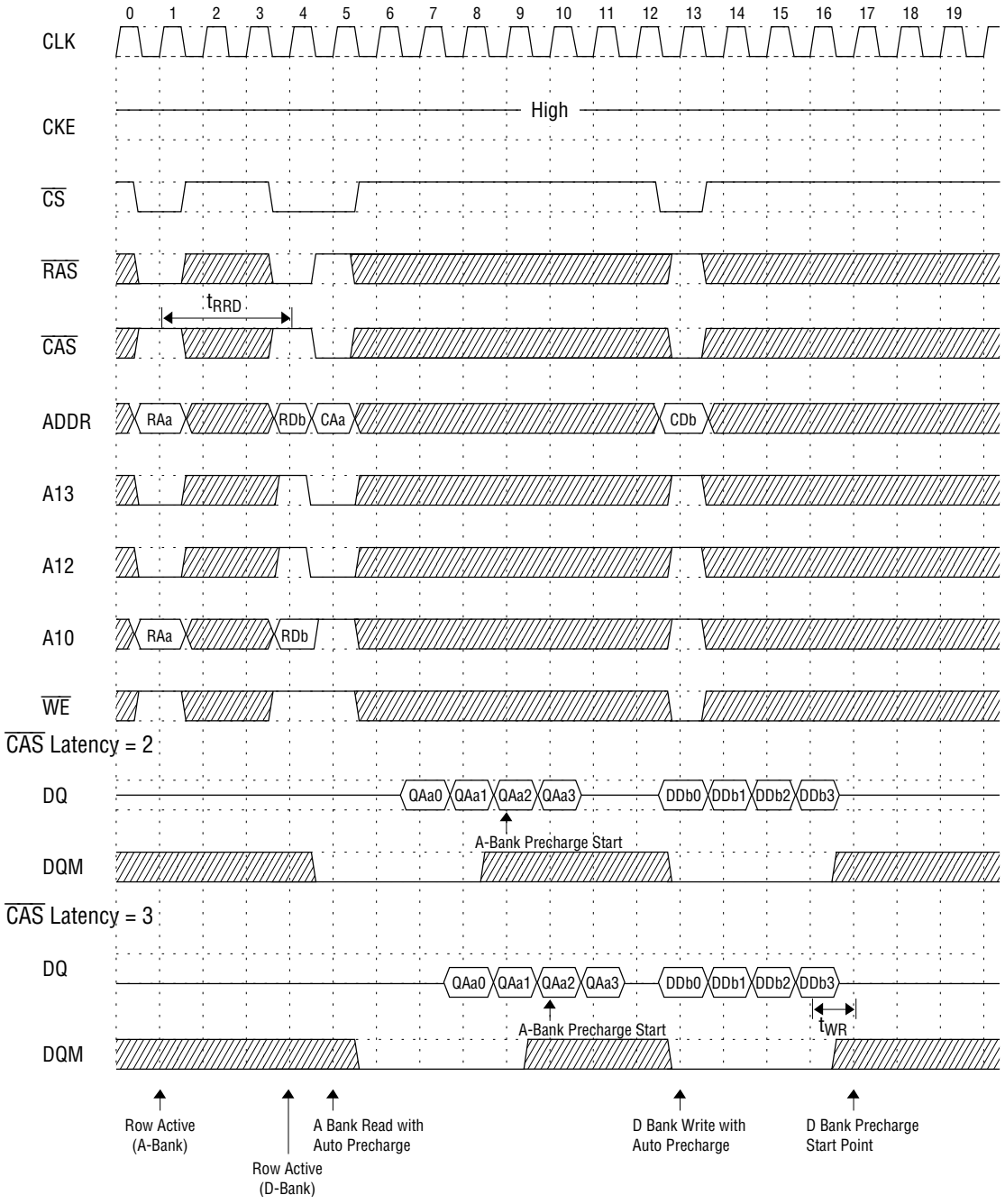
Page Read & Write Cycle (Same Bank) @ $\overline{CAS}$ Latency = 2, Burst Length = 4



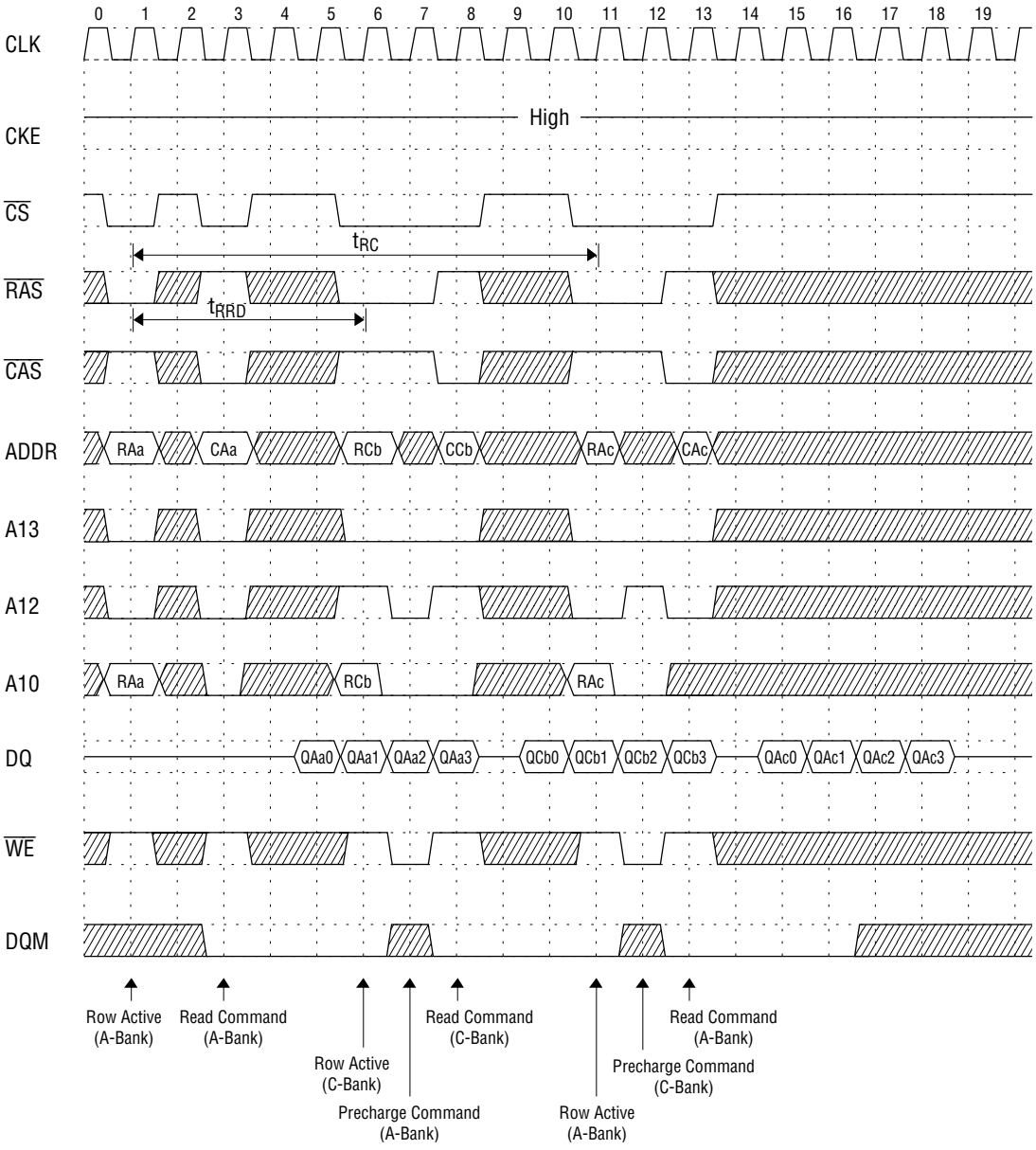
***Notes:**

1. To write data before a burst read ends, DQM should be asserted three cycles prior to the write command to avoid bus contention.
2. To assert row precharge before a burst write ends, wait t_{WR} after the last write data input. Input data during the precharge input cycle will be masked internally.

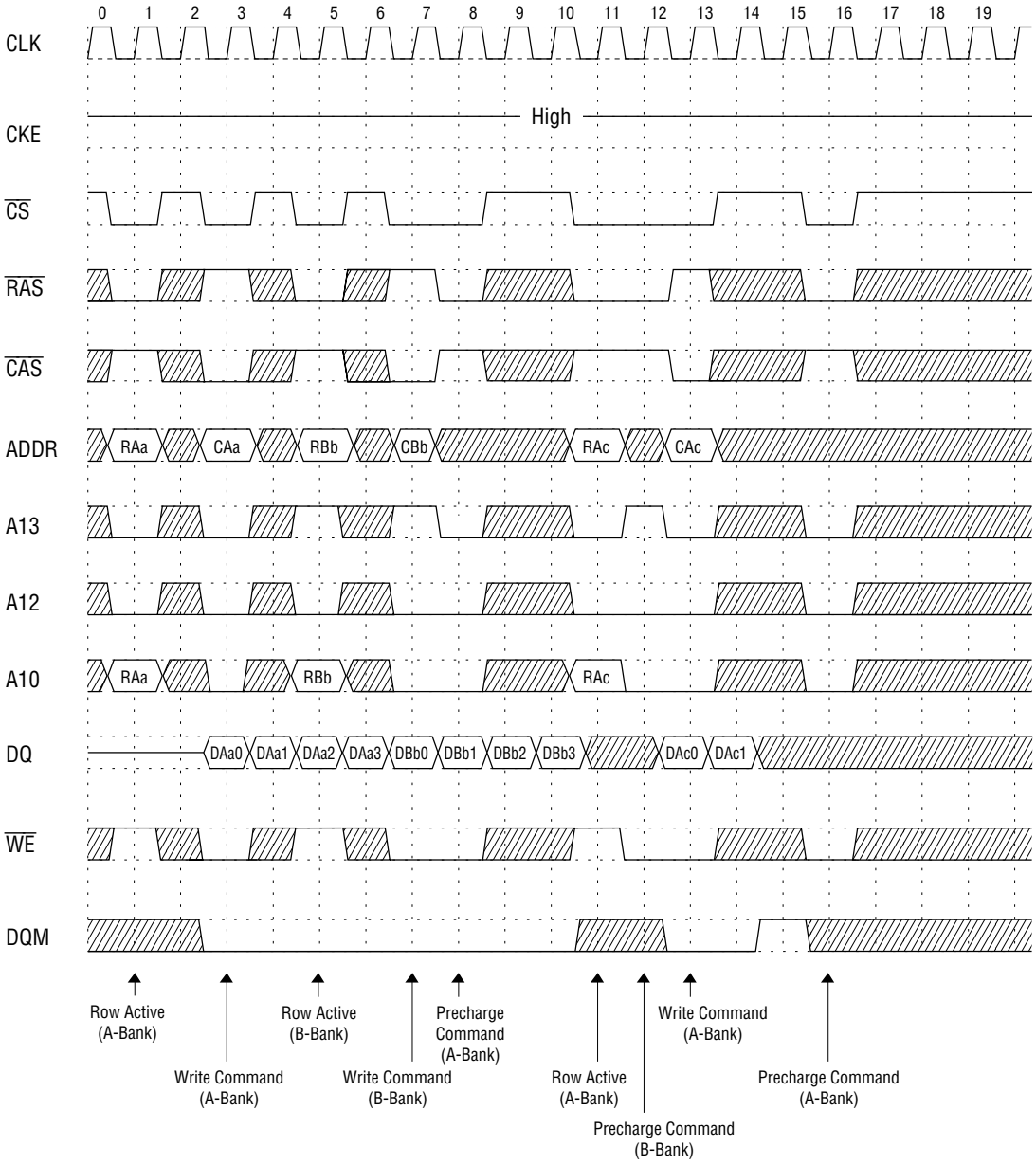
Read & Write Cycle with Auto Precharge @ Burst Length = 4



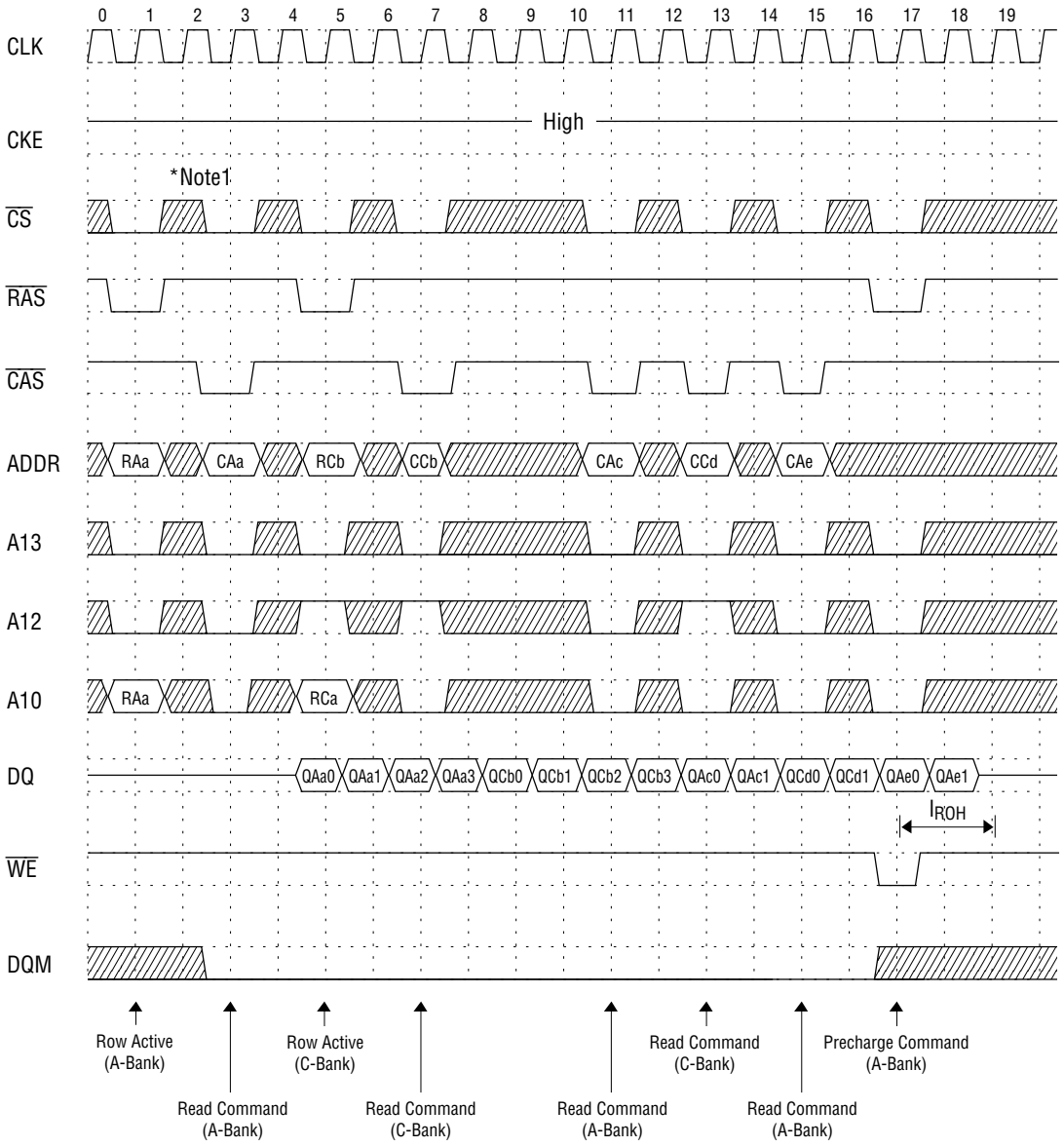
Bank Interleave Random Row Read Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4



Bank Interleave Random Row Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

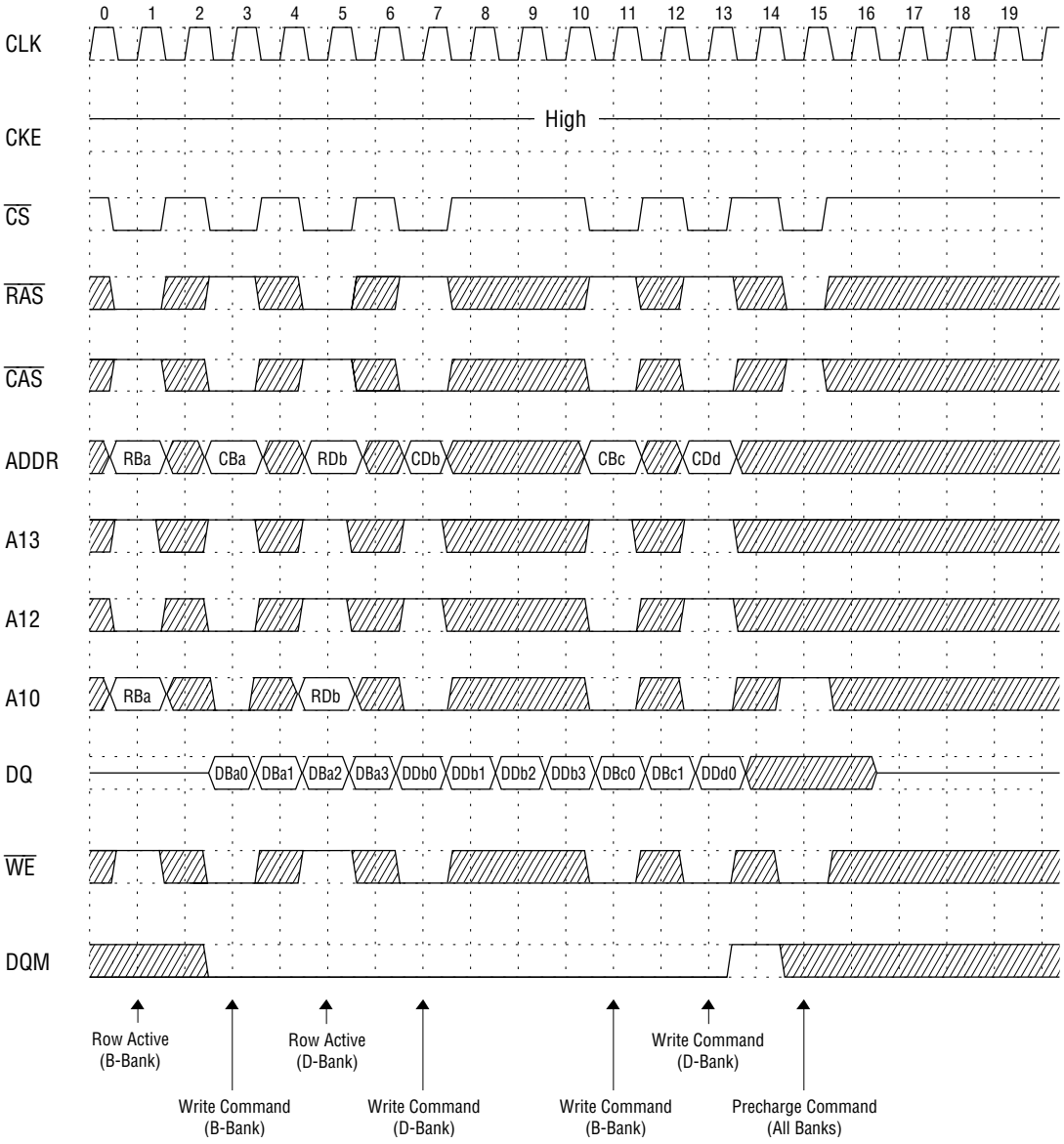


Bank Interleave Page Read Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4

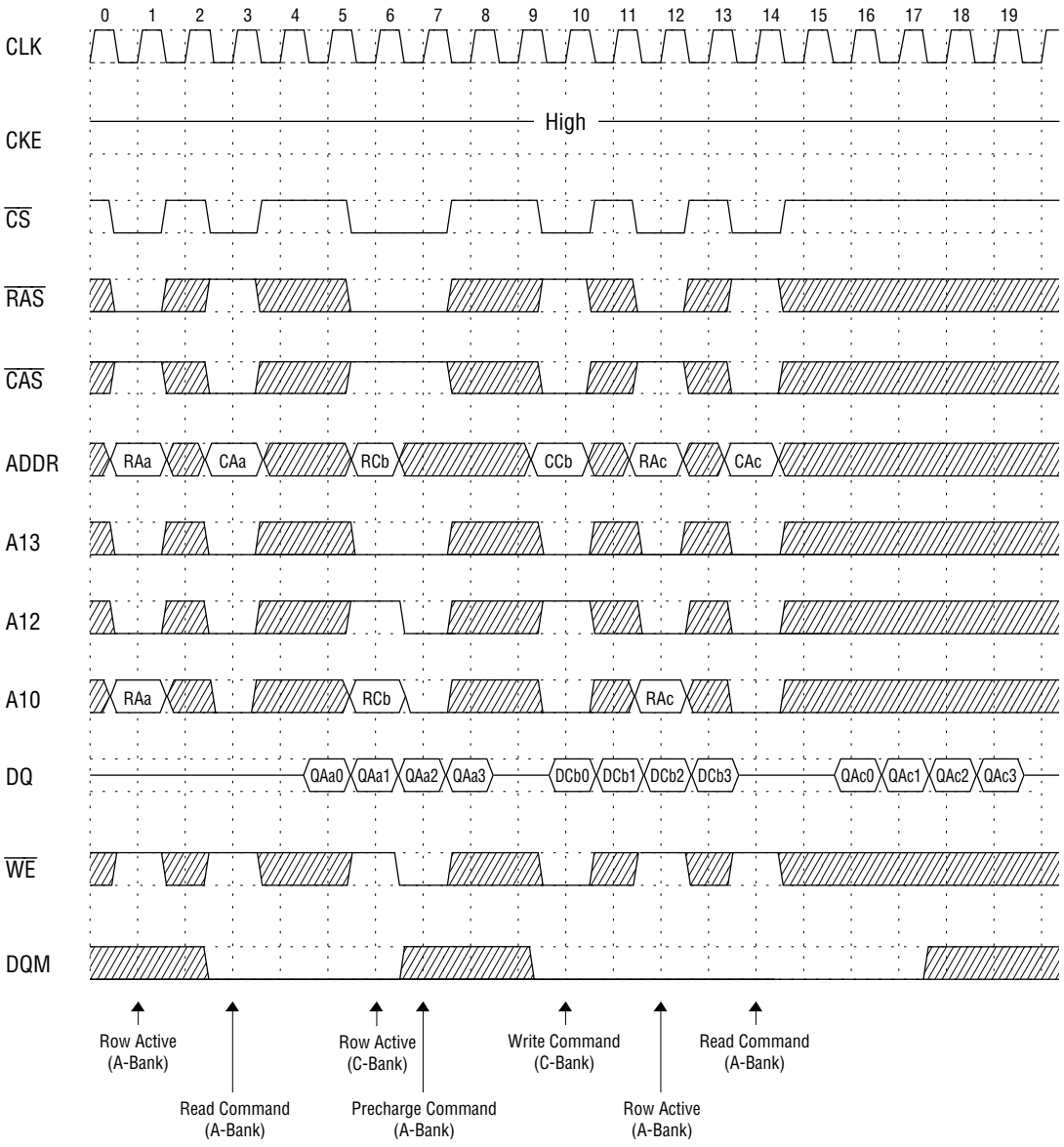


***Note:** 1. $\overline{CS}$ is ignored when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the same cycle.

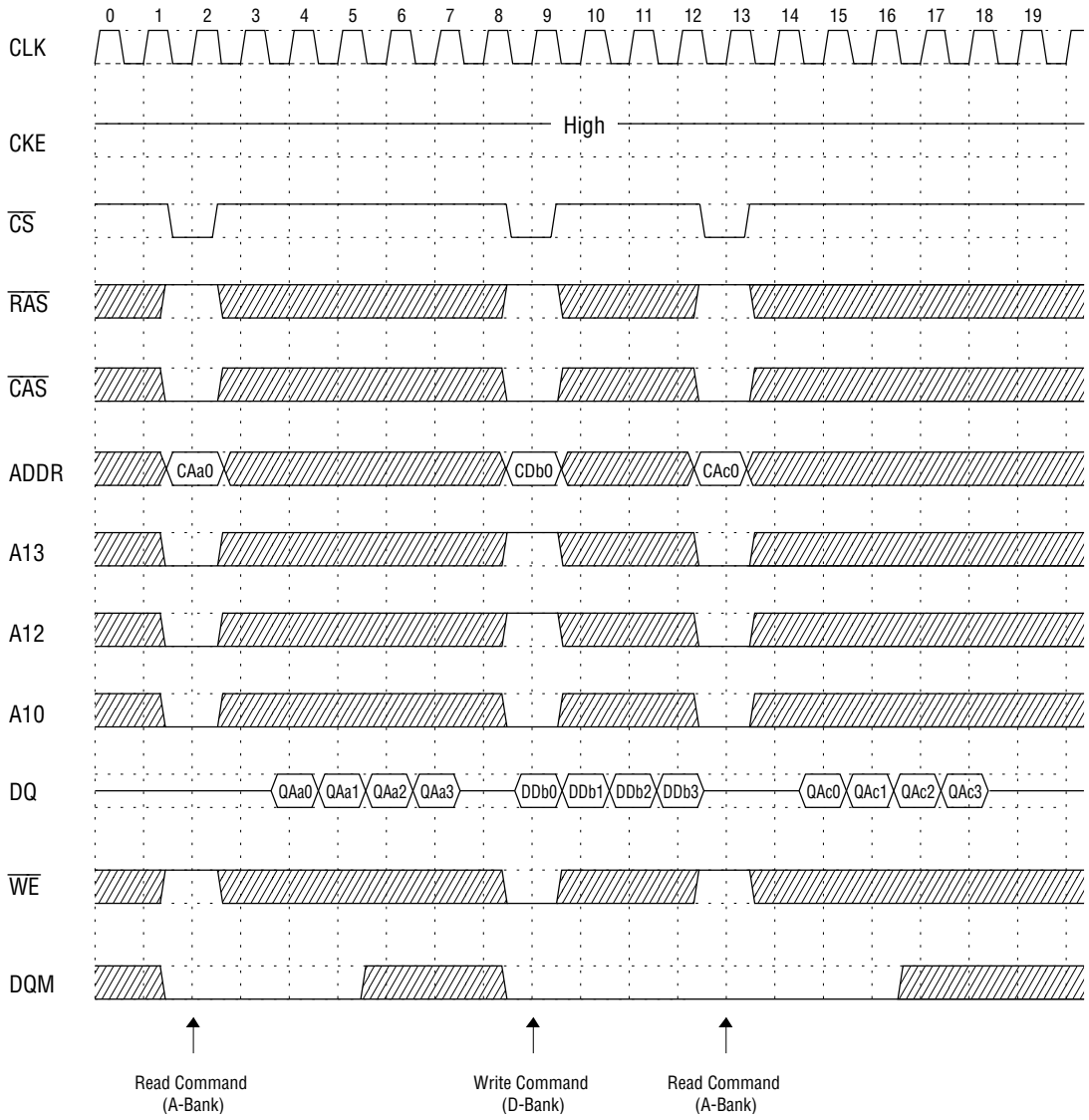
Bank Interleave Page Write Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4



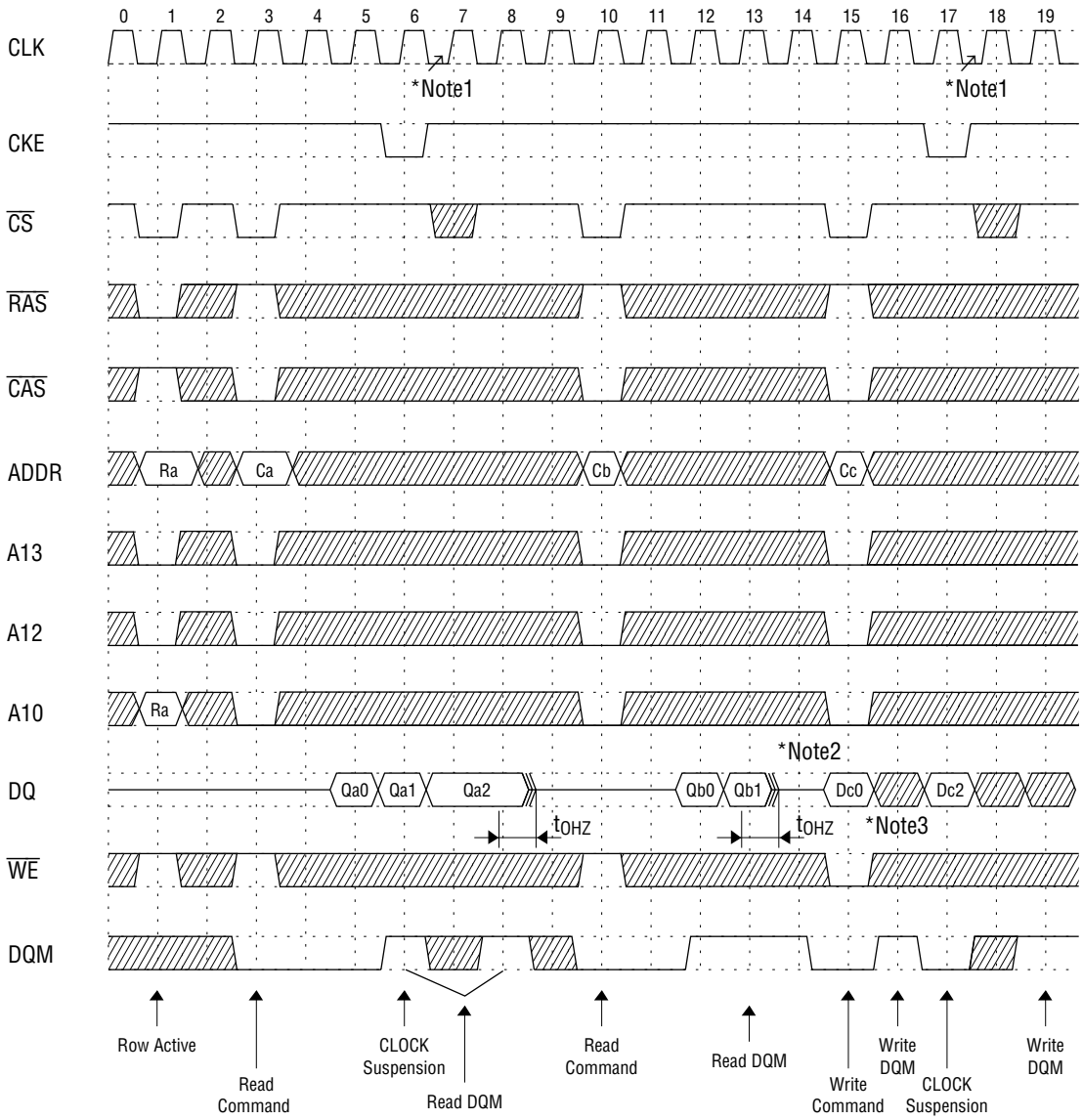
Bank Interleave Random Row Read/Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4

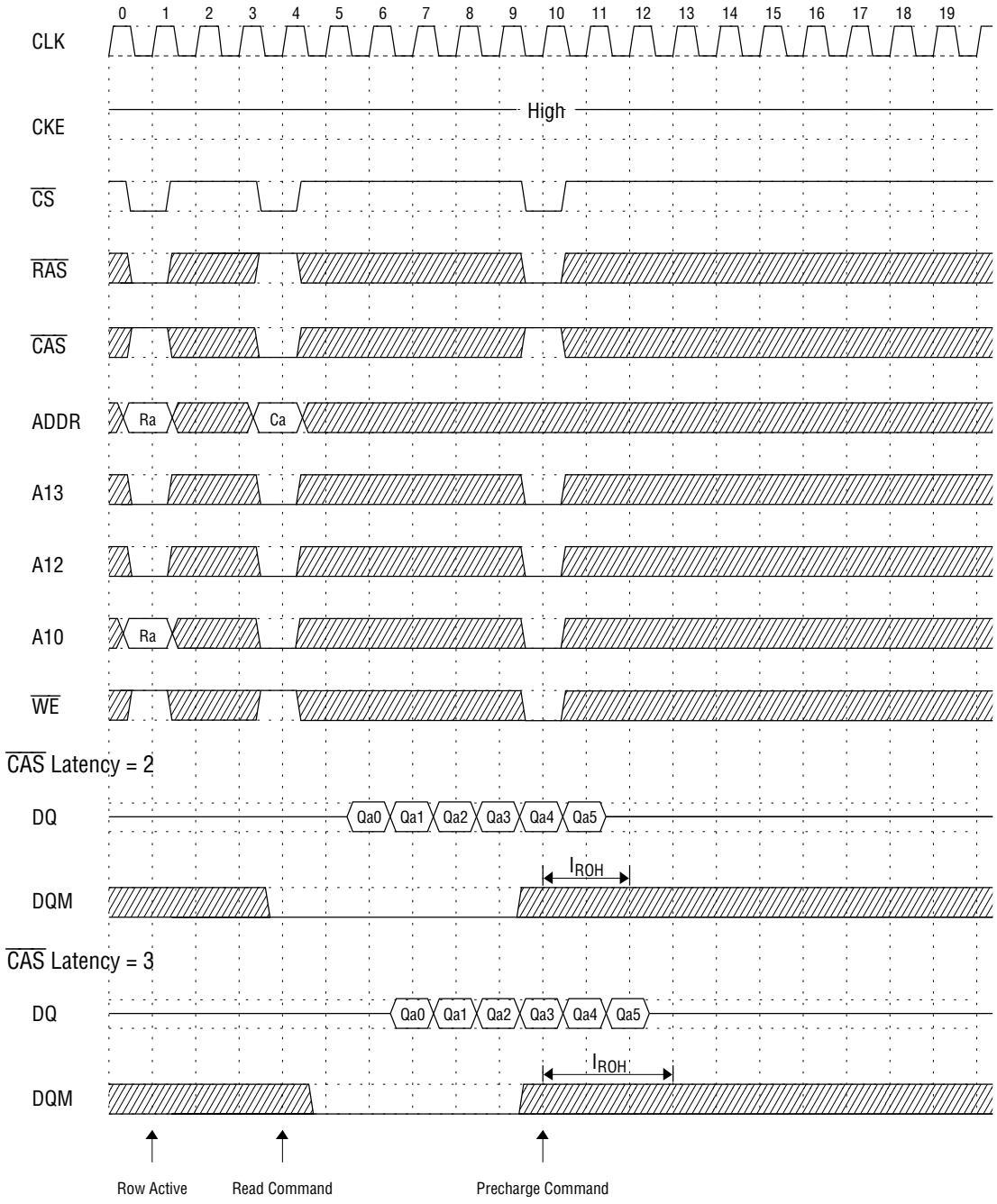


Clock Suspension & DQM Operation Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4

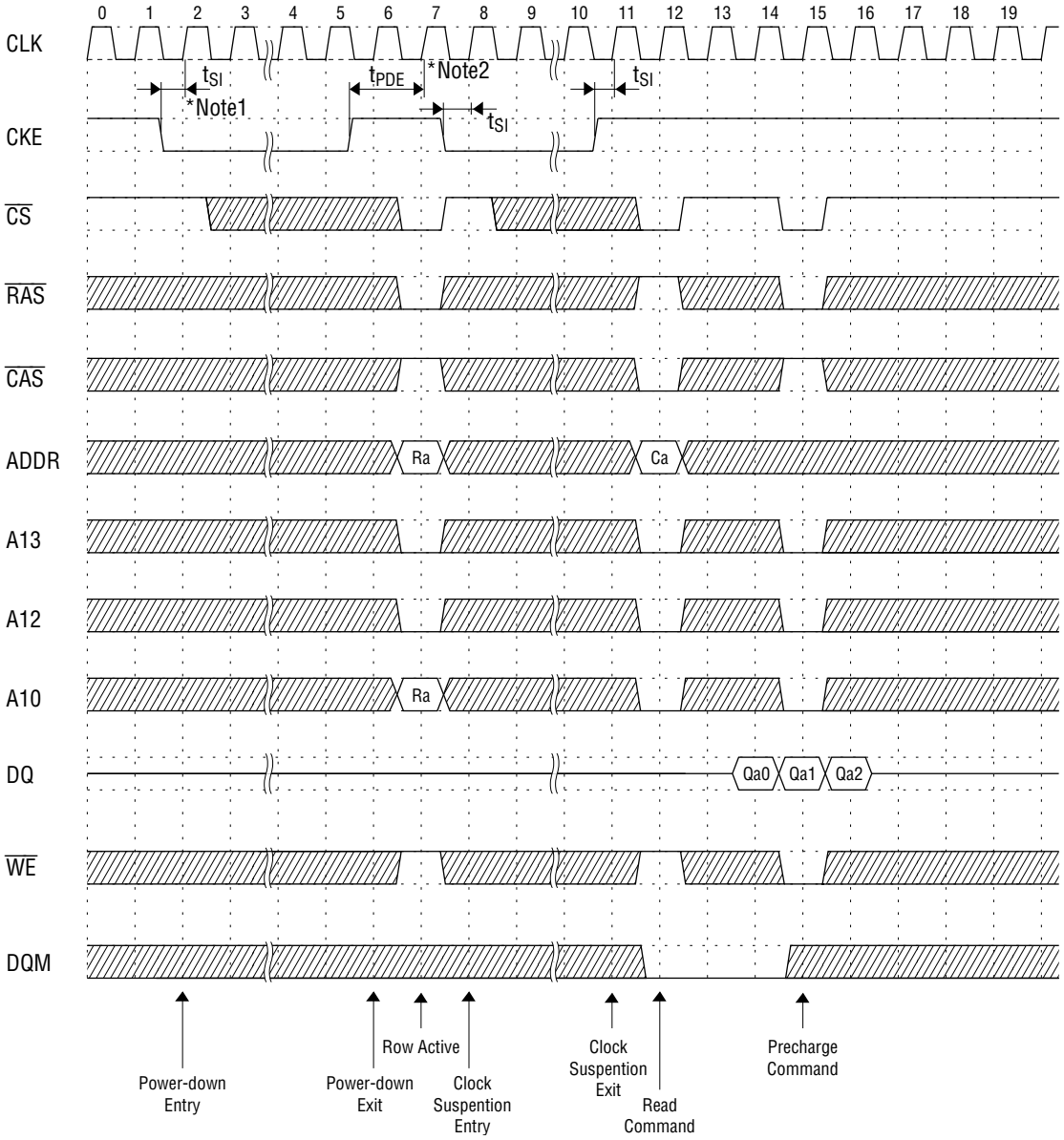


***Notes:**
1. When Clock Suspension is asserted, the next clock cycle is ignored.
2. When DQM is asserted, the read data after two clock cycles is masked.
3. When DQM is asserted, the write data in the same clock cycle is masked.

Read Interruption by Precharge Command @ Burst Length = 8

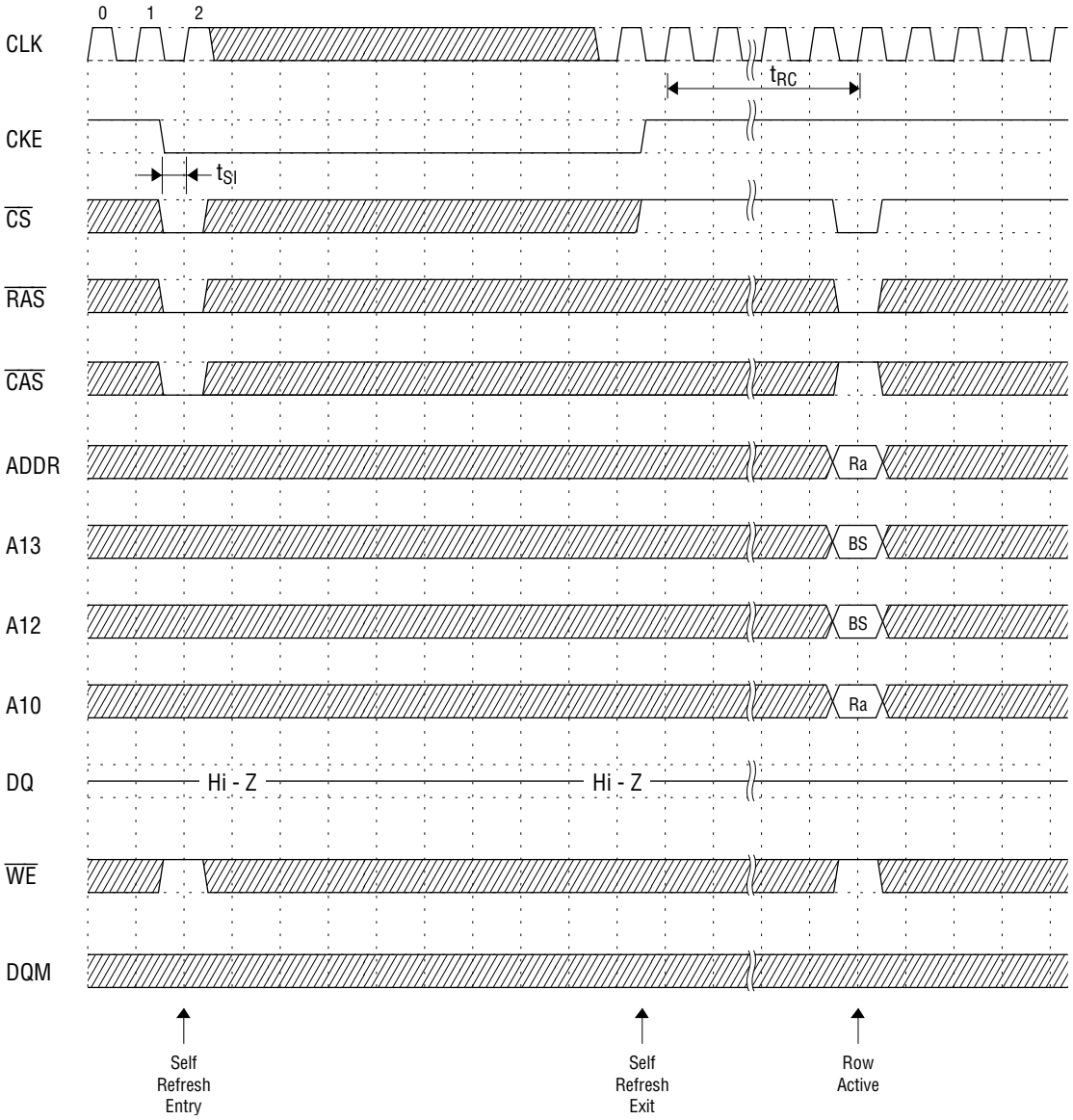


Power Down Mode @ $\overline{CAS}$ Latency = 2, Burst Length = 4

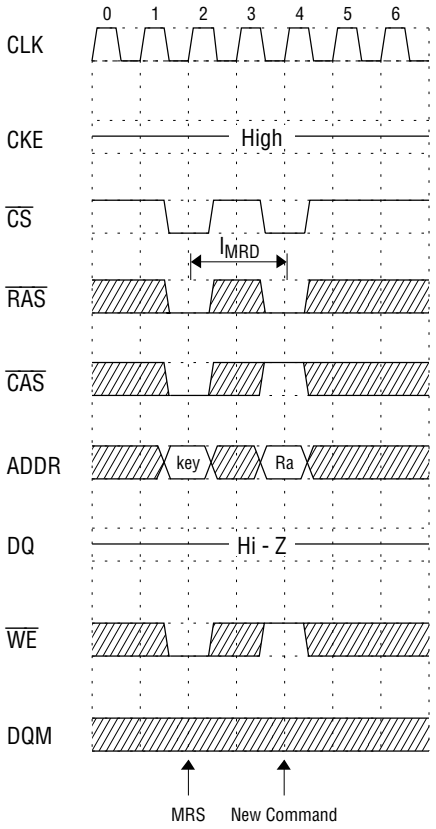


***Notes:**
1. When all banks are in precharge state, and if CKE is set low, then the MD56V62800A enters power-down mode and maintains the mode while CKE is low.
2. To release the circuit from power-down mode, CKE has to be set high for t_{PDE} (t_{SI} + 1 CLK) or more.

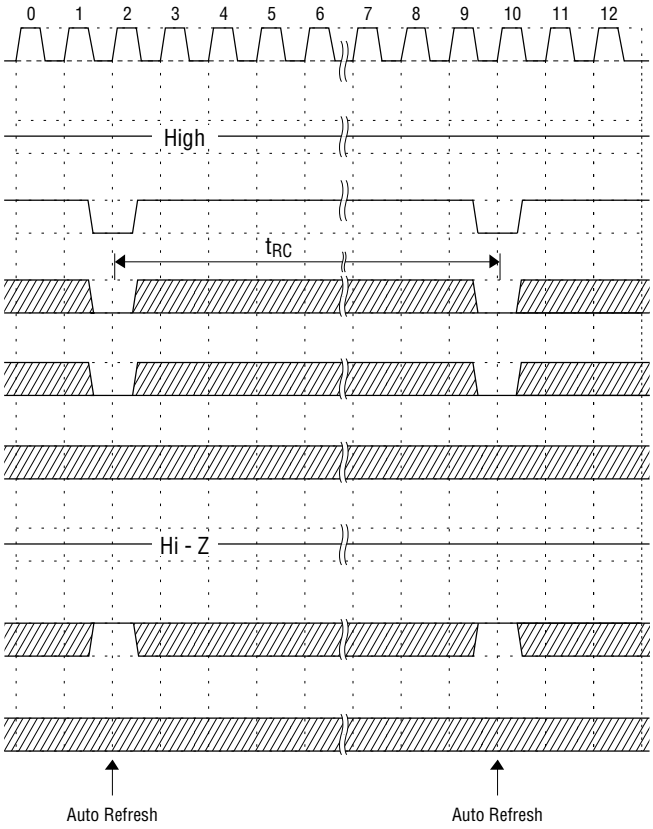
Self Refresh Cycle



Mode Register Set Cycle



Auto Refresh Cycle



FUNCTION TRUTH TABLE (Table 1) (1/2)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh [5]
	L	L	L	L	L	OP Code	Mode Register Write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A10	Read
	L	H	L	L	BA	CA, A10	Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Term Burst
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Term Burst
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (2/2)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP --> Idle after t_{RP}
	L	H	H	H	X	X	NOP --> Idle after t_{RP}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP --> Idle after t_{RC}
	L	H	H	X	X	X	NOP --> Idle after t_{RC}
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No OPeration command
CA = Column Address AP = Auto Precharge

Notes:
1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of l_{CCD} and t_{WR} to prevent bus contention.
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE for CKE (Table 2)

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL [6]
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle [6]	H	H	X	X	X	X	X	Refer to Table 1
(ABI)	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other	H	H	X	X	X	X	X	Refer to Operations in Table 1
than Listed Above	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

Note: 6. Power-down and self refresh can be entered only when all the banks are in an idle state.