OKI Semiconductor

FEDD56V82160-01
Issue Date:Feb.14, 2008

MD56V82160

4-Bank × 4,194,304-Word × 16-Bit SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The MD56V82160 is a 4-Bank × 4,194,304-word × 16-bit Synchronous dynamic RAM.
The device operates at 3.3 V. The inputs and outputs are LVTTL compatible.

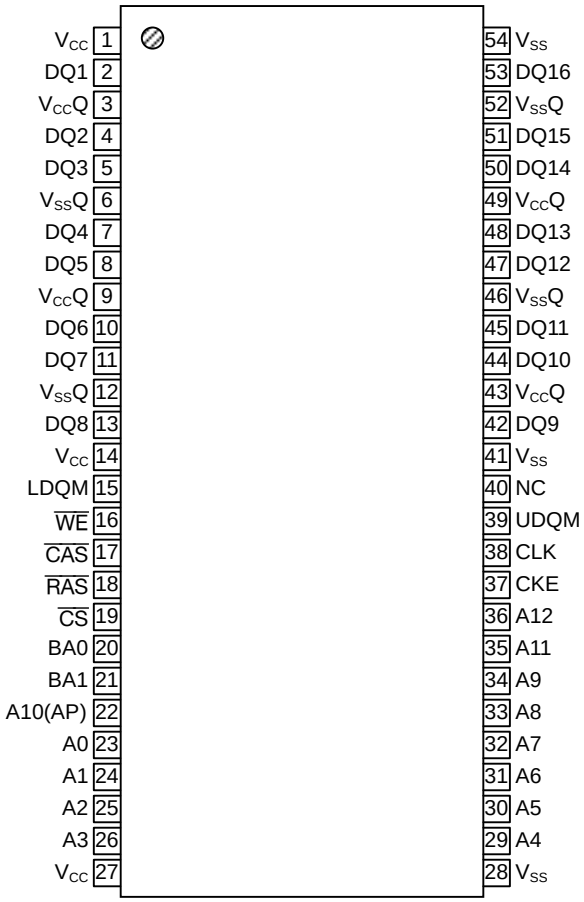
FEATURES

• Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
• 4-Bank × 4,194,304-word × 16-bit configuration
• Single 3.3 V power supply, ±0.3 V tolerance
• Input : LVTTL compatible
• Output : LVTTL compatible
• Refresh : 8192 cycles/64 ms
• Programmable data transfer mode
  - $\overline{\text{CAS}}$ Latency (2, 3)
  - Burst Length (1, 2, 4, 8, Full Page)
  - Data scramble (sequential, interleave)
• Auto-refresh, Self-refresh capability
• Lead-Free Package:
  54-pin 400 mil plastic TSOP (TypeII) (TSOP(2)54-P-400-0.80-K)(Product: MD56V82160-xxTAZ03)
  xx indicates speed rank.

PRODUCT FAMILY

Family	CL-tRP-tRCD	Max. Frequency	Access Time (Max.)	
			t_{AC2}	t_{AC3}
MD56V82160-6	3-3-3	166 MHz	–	5.4 ns
	2-3-3	133 MHz	5.4 ns	–

PIN CONFIGURATION (TOP VIEW)



54-Pin Plastic TSOP(II)
(K Type)

Pin Name	Function	Pin Name	Function
CLK	System Clock	UDQM, LDQM	Data Input/ Output Mask
$\overline{CS}$	Chip Select	DQi	Data Input/ Output
CKE	Clock Enable	V_{CC}	Power Supply (3.3 V)
A0–A12	Address	V_{SS}	Ground (0 V)
BA0,1	Bank Select Address	$V_{CC}Q$	Data Output Power Supply (3.3 V)
$\overline{RAS}$	Row Address Strobe	$V_{SS}Q$	Data Output Ground (0 V)
$\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Write Enable		

Note : The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}Q$ pin.

The same GND voltage level must be provided to every V_{SS} pin and $V_{SS}Q$ pin.

PIN DESCRIPTION

CLK	Fetches all inputs at the “H” edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, UDQM and LDQM.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address : RA0 – RA12 Column Address : CA0 – CA8
BA0, BA1	Slects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
UDQM, LDQM	Masks the read data of two clocks later when UDQM and LDQM are set “H” at the “H” edge of the clock signal. Masks the write data of the same clock when UDQM and LDQM are set “H” at the “H” edge of the clock signal. UDQM controls upper byte and LDQM controls lower byte.
DQi	Data inputs/outputs are multiplexed on the same pin.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to 4.6	V
V_{CC} Supply Voltage	V_{CC} , $V_{CC}Q$	–0.5 to 4.6	V
Storage Temperature	T_{stg}	–65 to 150	°C
Power Dissipation	P_{D*}	1000	mW
Short Circuit Output Current	I_{OS}	50	mA
Operating Temperature	T_{opr}	0 to 70	°C

*: Ta = 25°C

Recommended Operating Conditions

(Voltages referenced to V_{SS} = $V_{SS}Q$ = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}, $V_{CC}Q$	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	0	0.8	V

V_{IH}(MAX)=4.6V AC for pulse width ≤ 10ns acceptable.

V_{IL}(MIN)=－1.5V AC for pulse width ≤ 10ns acceptable.

Pin Capacitance

(V_{bias} = 1.4 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	C_{CLK}	2	3	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, UDQM, LDQM,)	C_{IN}	1.5	4.5	pF
Input Capacitance (Address)	C_{ADD}	1.5	3	
Input/Output Capacitance (DQ1 – DQ16)	C_{OUT}	2	4.5	pF

DC Characteristics

Parameter	Symbol	Condition			MD56V82160-6		Unit	Note
		Bank	CKE	Others	Min.	Max.		
Output High Voltage	V_{OH}	—	—	I_{OH} =–1.0mA	2.4	—	V	
Output Low Voltage	V_{OL}	—	—	I_{OL} =1.0mA	—	0.4	V	
Input Leakage Current	I_{LI}	Any input 0V ≤ VIN ≤ V_{CC} + 0.3V, all other pins are not under test = 0V			–5	5	μA	
Output Leakage Current	I_{LO}				–5	5	μA	
Operating Current	I_{CC1}	One Bank Active	—	t_{RC} = Min. BL=2 I_O=0mA	—	150	mA	
Precharge Standby Current (Power-Down)	I_{CC2P}	—	CKE = $V_{IL(max)}$	t_{CC} = 10ns	—	15	mA	
	I_{CC2PS}	—	CKE **&** CLK = $V_{IL(max)}$	t_{CC} = ∞	—	5		
Precharge Standby Current (Non Power Down)	I_{CC2N}	ALL Banks Precharge	CKE = $V_{IH(min)}$	CS = $V_{IH(min)}$ t_{CC} = 10ns Input Signals are changed one time during20ns.	—	40	mA	
	I_{CC2NS}	ALL Banks Precharge	CKE = $V_{IH(min)}$	CLK = $V_{IL(max)}$ t_{CC} = ∞ Input Signals are stable.	—	30		
Active Standby Current (Power-Down)	I_{CC3P}	One Bank Active	CKE= $V_{IL(max)}$	t_{CC} = 10ns	—	35	mA	
	I_{CC3PS}		CKE **&** CLK = $V_{IL(max)}$	t_{CC} = ∞	—	20		
Active Standby Current (Non Power Down)	I_{CC3N}	One Bank Active	CKE = $V_{IH(min)}$	CS = $V_{IH(min)}$ t_{CC} = 10ns Input Signals are changed one time during20ns.	—	65	mA	
	I_{CC3NS}		CKE = $V_{IH(min)}$	CLK = $V_{IL(max)}$ t_{CC} = ∞ Input Signals are stable.	—	45		
Operating Current(Burst)	I_{CC4}	4Banks Activated	—	I_O=0mA Page Burst t_{CCD}=2CLKs	—	165	mA	1
Refresh Current	I_{CC5}	—	—	t_{ARFC} = t_{ARFC}(min.)	—	200	mA	2
Self-Refresh Current	I_{CC6}	—	CKE=0.2V	—	—	6	mA	

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted,input swing level is VIH/VIL=VCCQ/VSSQ.

Mode Set Address Keys

Single Write		$\overline{CAS}$ Latency				Burst Type		Burst Length				
A9	BRSW	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Normal	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single Write	0	0	1	Reserved	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

Notes: A7, A8, A10, A11,A12,BA0 and BA1 should stay “L” during mode set cycle.

POWER ON SEQUENCE

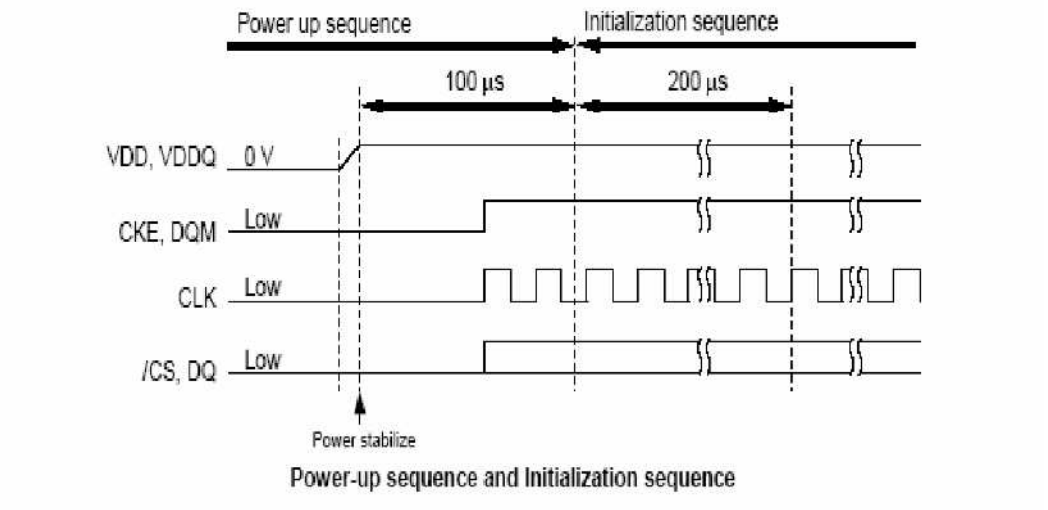
1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   -Apply V_{CC} before or the same time as V_{CCQ}.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

Notice: (POWER ON SEQUENCE)

1.The SDRAM should be goes on the following sequence with power up.
2.The CLK,CKE,/CS,DQM and DQ pins keep low till power stabilizes.
3.The CLK pin is stabilized within 100us after power stabilizes before the following initialization sequence.
4.The CKE and DQM is driven to high between power stabilizes and the initialization sequence.
5.This SDRAM has VCC clamp diodes for CLK ,CKE,Address,/RAS,/CAS,/WE,/CS,DQM and DQ pins. If these pins go high before power up ,the large current flows from these pins to VCC through the diodes.

INITIALIZATION SEQUENCE

When 200us or more has past after the above power-up sequence, all banks must be precharged using the precharge command(PALL).After tRP delay, set 8 or more auto refresh commands(REF).Set the mode register set command(MRS) to initialize the mode register. We recommend that by keeping DQM and CKE to high, the output buffer becomes High-Z during initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.



Power-up sequence and Initialization sequence

AC Characteristics (1/2)

Note1, 2

Parameter		Symbol	MD56V82160-6		Unit	Note
			Min.	Max.		
Clock Cycle Time	CL = 3	t_{CC3}	6	—	ns	
	CL = 2	t_{CC2}	7.5	—	ns	
Access Time from Clock	CL = 3	t_{AC3}	—	5.4	ns	3, 4
	CL = 2	t_{AC2}	—	5.4	ns	3, 4
Clock High Pulse Time		t_{CH}	2.5	—	ns	
Clock Low Pulse Time		t_{CL}	2.5	—	ns	
Input Setup Time		t_{SI}	1.5	—	ns	
Input Hold Time		t_{HI}	1	—	ns	
Output High Impedance Time from Clock		t_{OHZ}	—	5.4	ns	
Output Hold from Clock		t_{OH}	2.5	—	ns	3
Random Read or Write Cycle Time		t_{RC}	60	—	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	18	—	ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	42	100,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	18	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Bank Active Delay Time		t_{RRD}	12	—	ns	
Refresh Time		t_{REF}	—	64	ms	
Power-down Exit setup Time		t_{PDE}	1CLK + t_{SI}	—	ns	
Write Recovery Time		t_{WR}	2		Cycle	
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Min.)		l_{CCD}	1		Cycle	
Last data in to active delay		l_{DAL}	5		Cycle	
Clock Disable Time from CKE		l_{CKE}	1		Cycle	
Data Output High Impedance Time from UDQM, LDQM		l_{DOZ}	2		Cycle	
Dada Input Mask Time from UDQM, LDQM		l_{DID}	0		Cycle	

AC Characteristics (2/2)

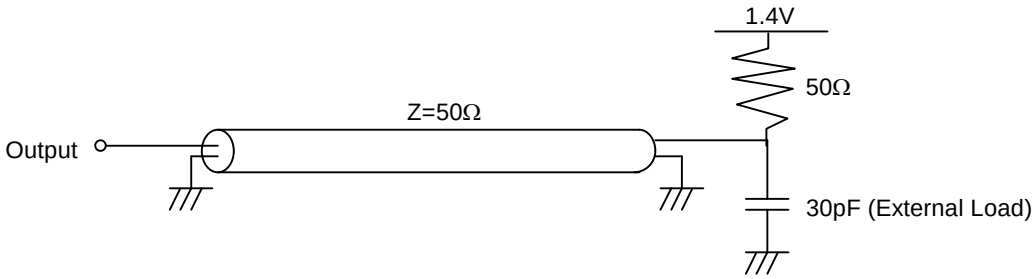
Note1, 2

Parameter	Symbol	MD56V82160-6		Unit	Note
		Min.	Max.		
Data Input Mask Time from Write Command	l_{DWD}	0		Cycle	
Data Output High Impedance Time from Precharge Command	l_{ROH}	CL		Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	l_{MRD}	2		Cycle	
Write Command Input Time from Output	l_{OWD}	2		Cycle	

Notes: 1. AC measurements assume that t_T = 1 ns.

2. The reference level for timing of input signals is 1.4 V.
   The input signal conditions are below.
   V_{IH} = 2.4 V, V_{IL} = 0.4 V

3. Output load.

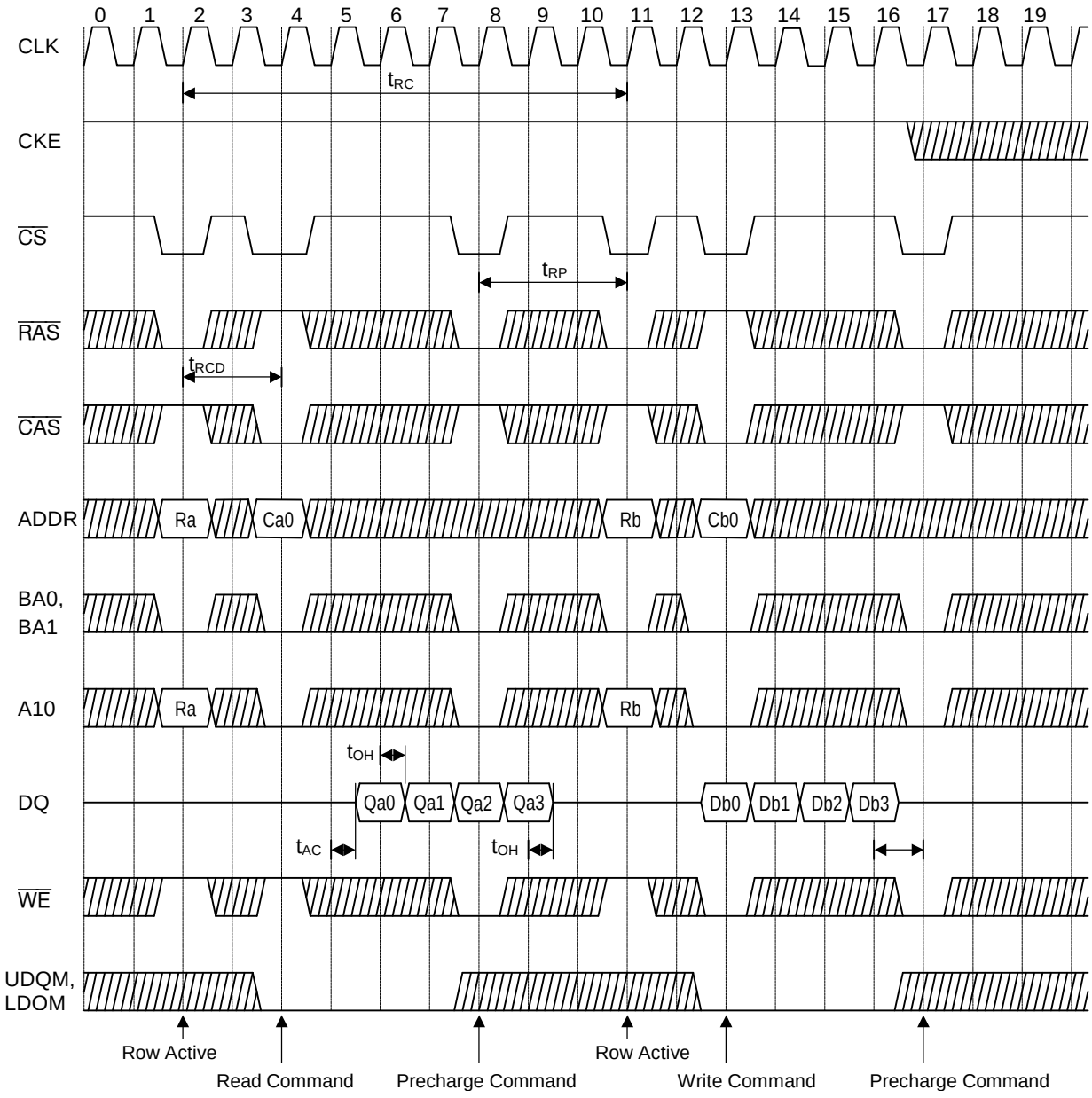


4. The access time is defined at 1.4 V.

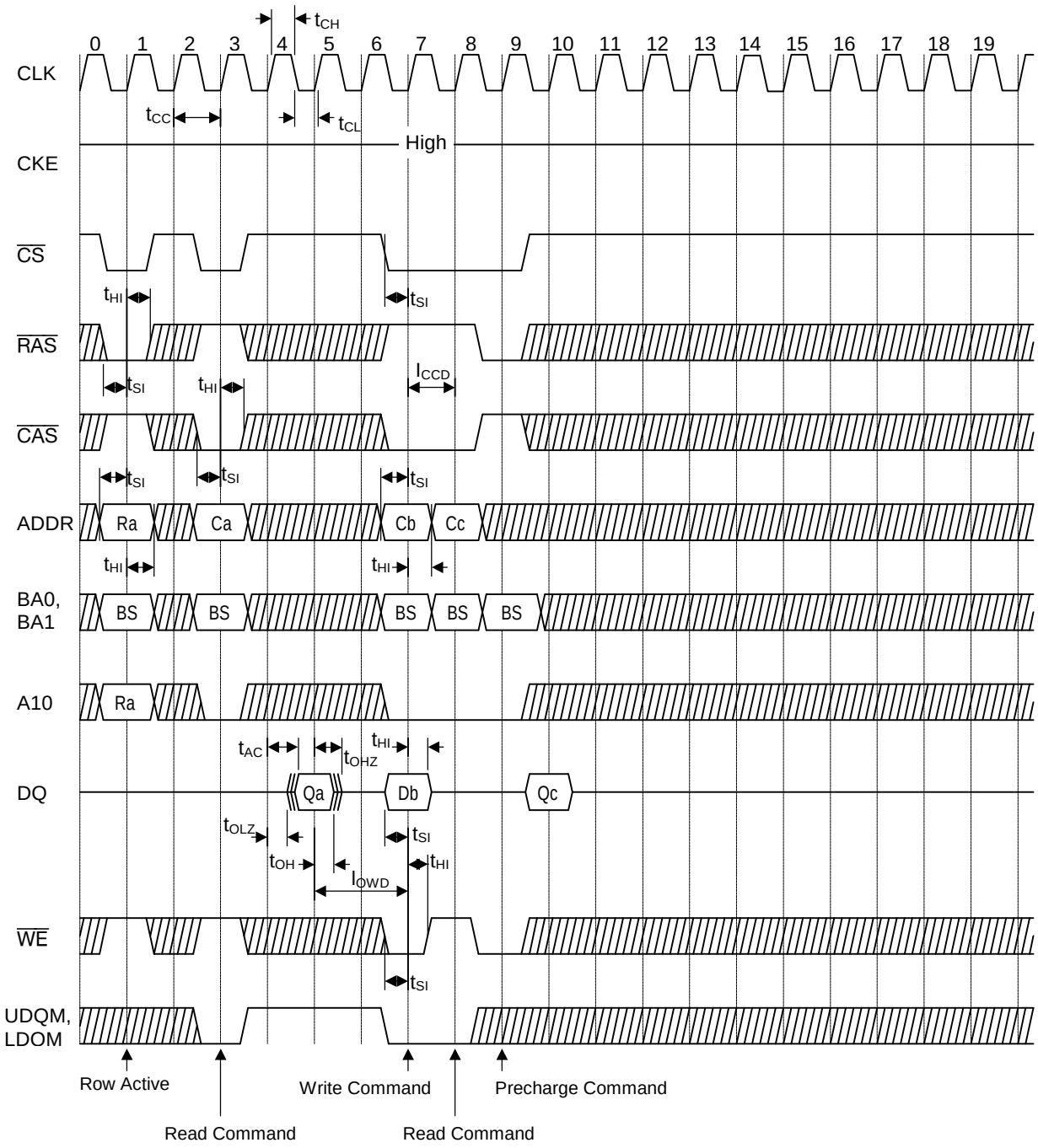
5. If t_T is longer than 1 ns, then the reference level for timing of input signals is V_{IH} and V_{IL}.

TIMING CHART

Read & Write Cycle (Same Bank) @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Single Bit Read-Write-Read Cycle (Same Page) @$\overline{CAS}$ Latency = 2, Burst Length = 4



*Notes: 1. When $\overline{CS}$ is set "High" at a clock transition from "Low" to "High", all inputs except CLK, CKE, UDQM and LDQM are invalid.

2. When issuing an active, read or write command, the bank is selected by BA0 and BA1.

BA0	BA1	Active, read or write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

A10	BA0	BA1	Operation
0	0	0	After the end of burst, bank A holds the Row-Active status.
1	0	0	After the end of burst, bank A is precharged automatically.
0	0	1	After the end of burst, bank B holds the Row-Active status.
1	0	1	After the end of burst, bank B is precharged automatically.
0	1	0	After the end of burst, bank C holds the Row-Active status.
1	1	0	After the end of burst, bank C is precharged automatically.
0	1	1	After the end of burst, bank D holds the Row-Active status.
1	1	1	After the end of burst, bank D is precharged automatically.

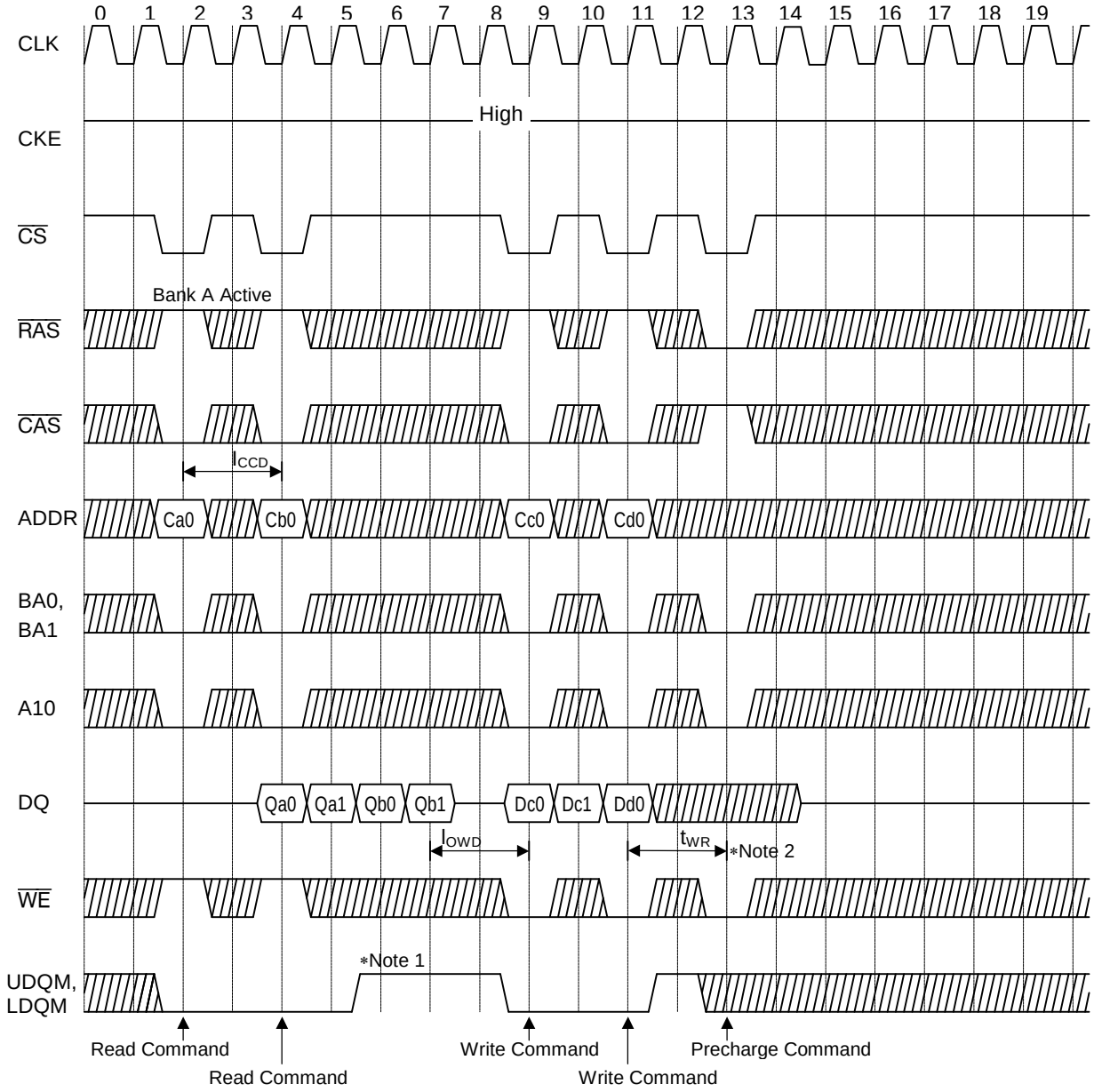
4. When issuing a precharge command, the bank to be precharged is selected by the A12 and A13 inputs.

A10	BA0	BA1	Operation
0	0	0	Bank A is precharged.
0	0	1	Bank B is precharged.
0	1	0	Bank C is precharged.
0	1	1	Bank D is precharged.
1	X	X	All banks are precharged.

5. The input data and the write command are latched by the same clock (Write latency = 0).

6. The output is forced to high impedance by (1CLK+ t_{OHZ}) after UDQM, LDQM entry.

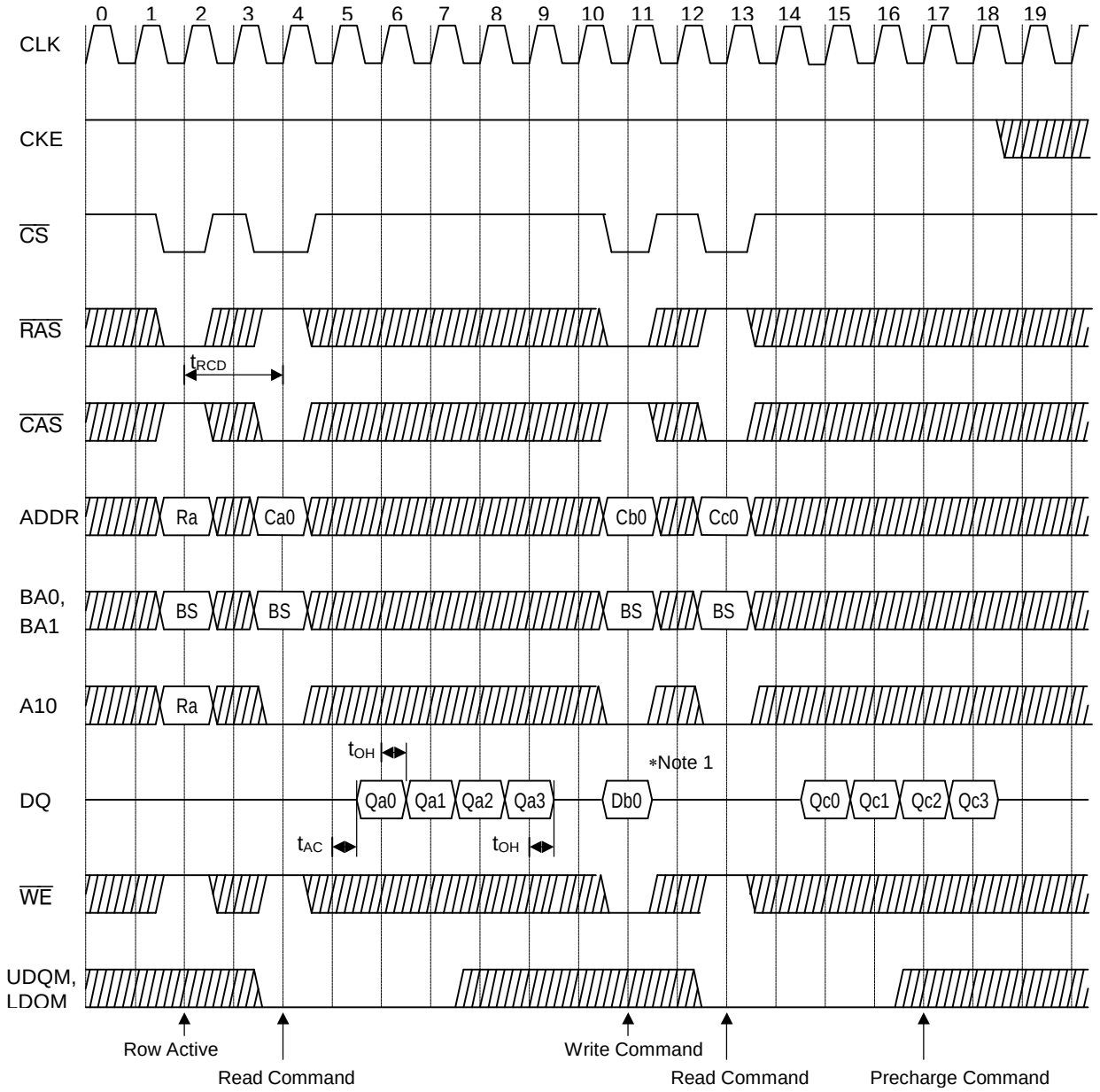
Page Read & Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4



*Notes: 1. To write data before a burst read ends, UDQM and LDQM should be asserted three cycles prior to the write command to avoid bus contention.

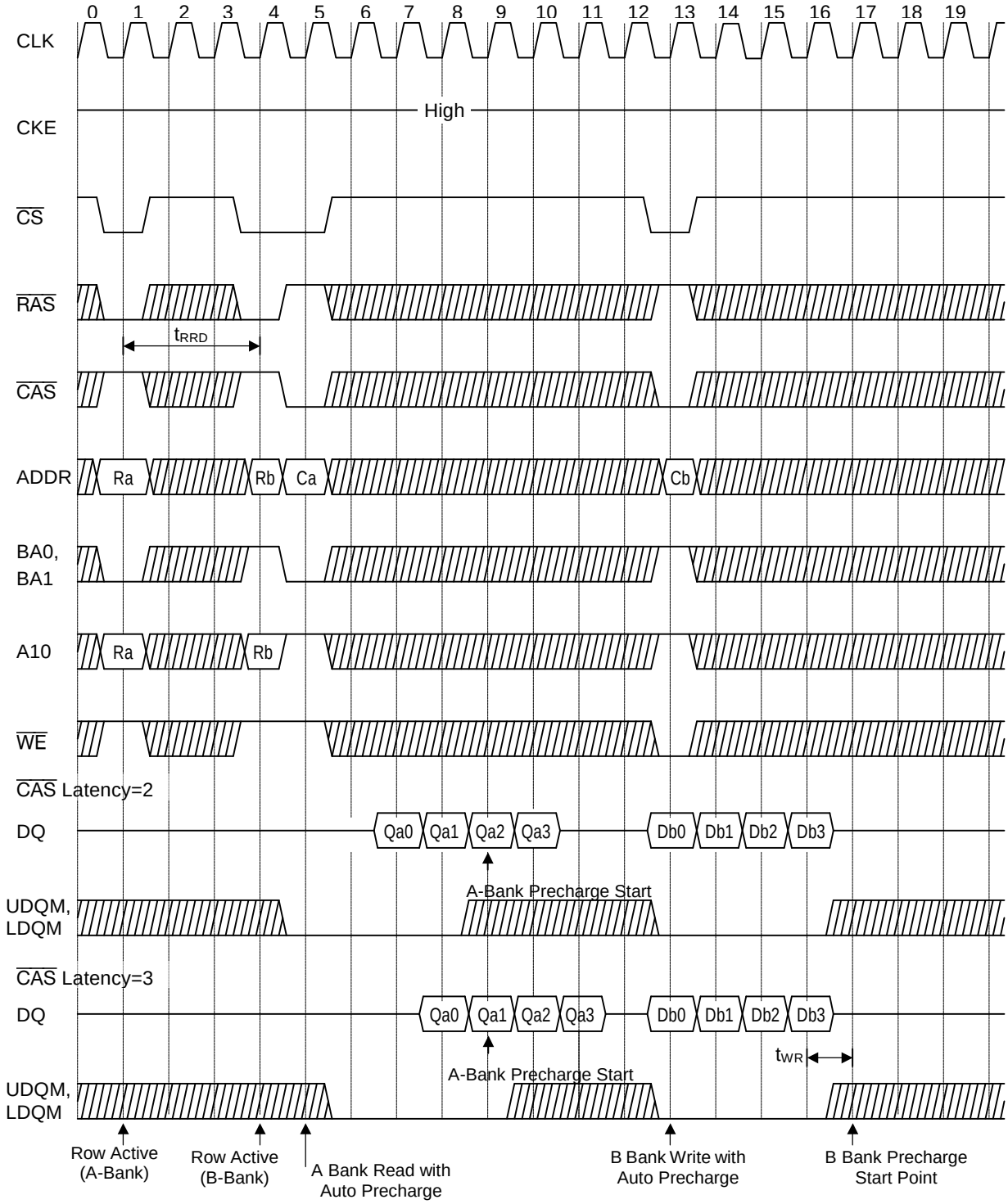
2. To assert row precharge before a burst write ends, wait t_{WR} after the last write data input. Input data during the precharge input cycle will be masked internally.

Burst Read & Single Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4

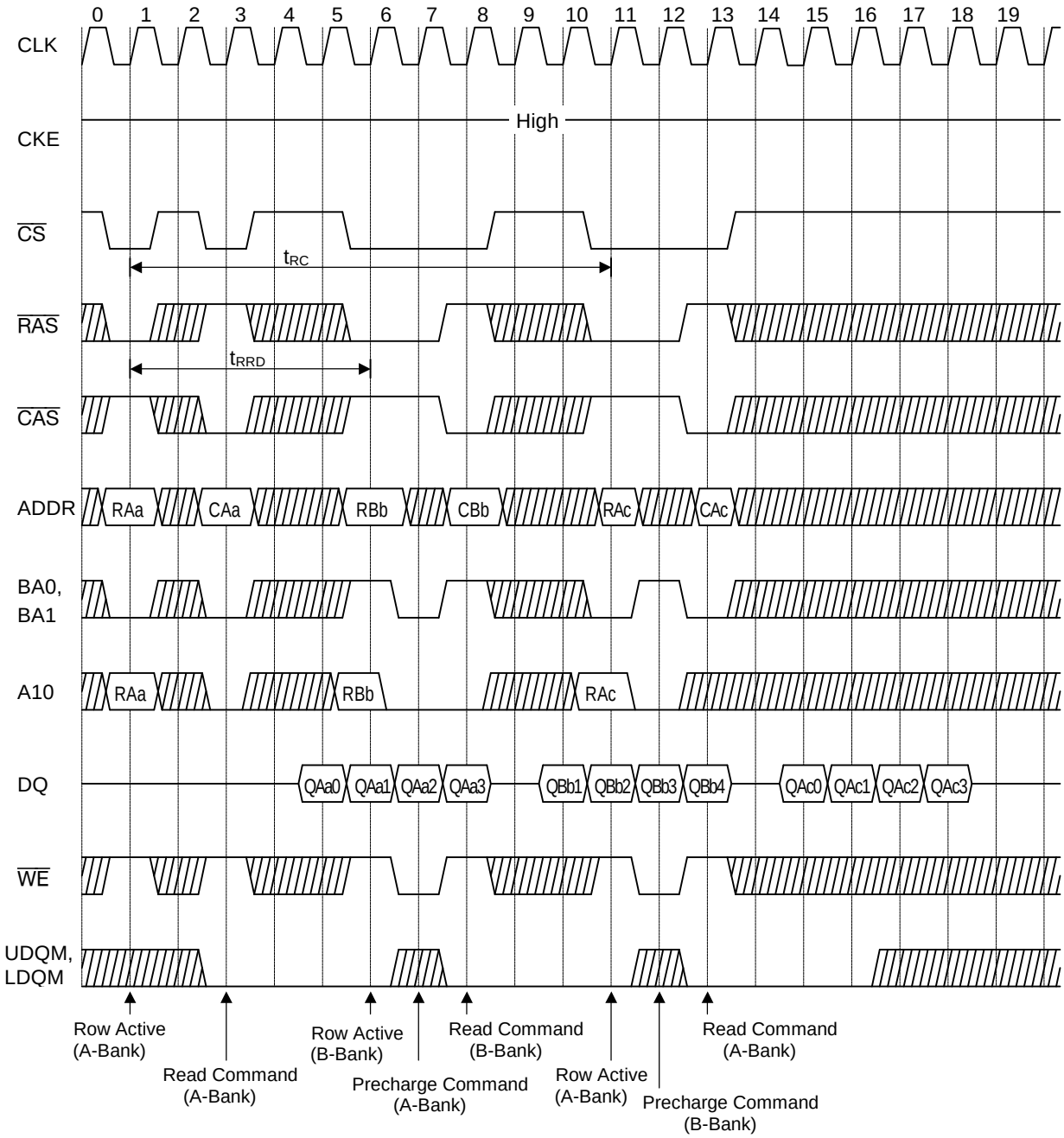


*Note: 1. If you set A9 to high during mode register set cycle, the write burst length is set to 1.

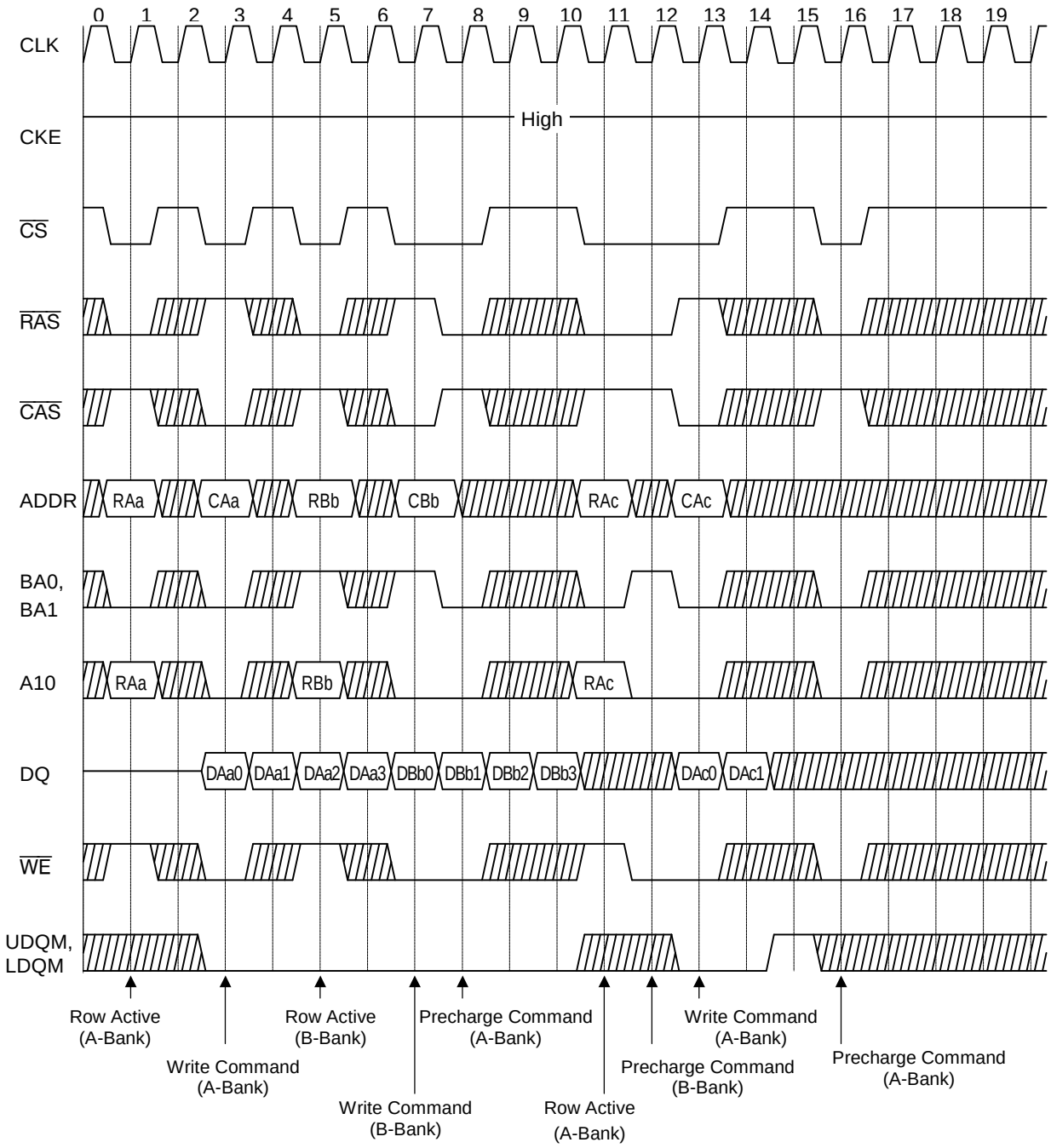
Read & Write Cycle with Auto Precharge @ Burst Length = 4



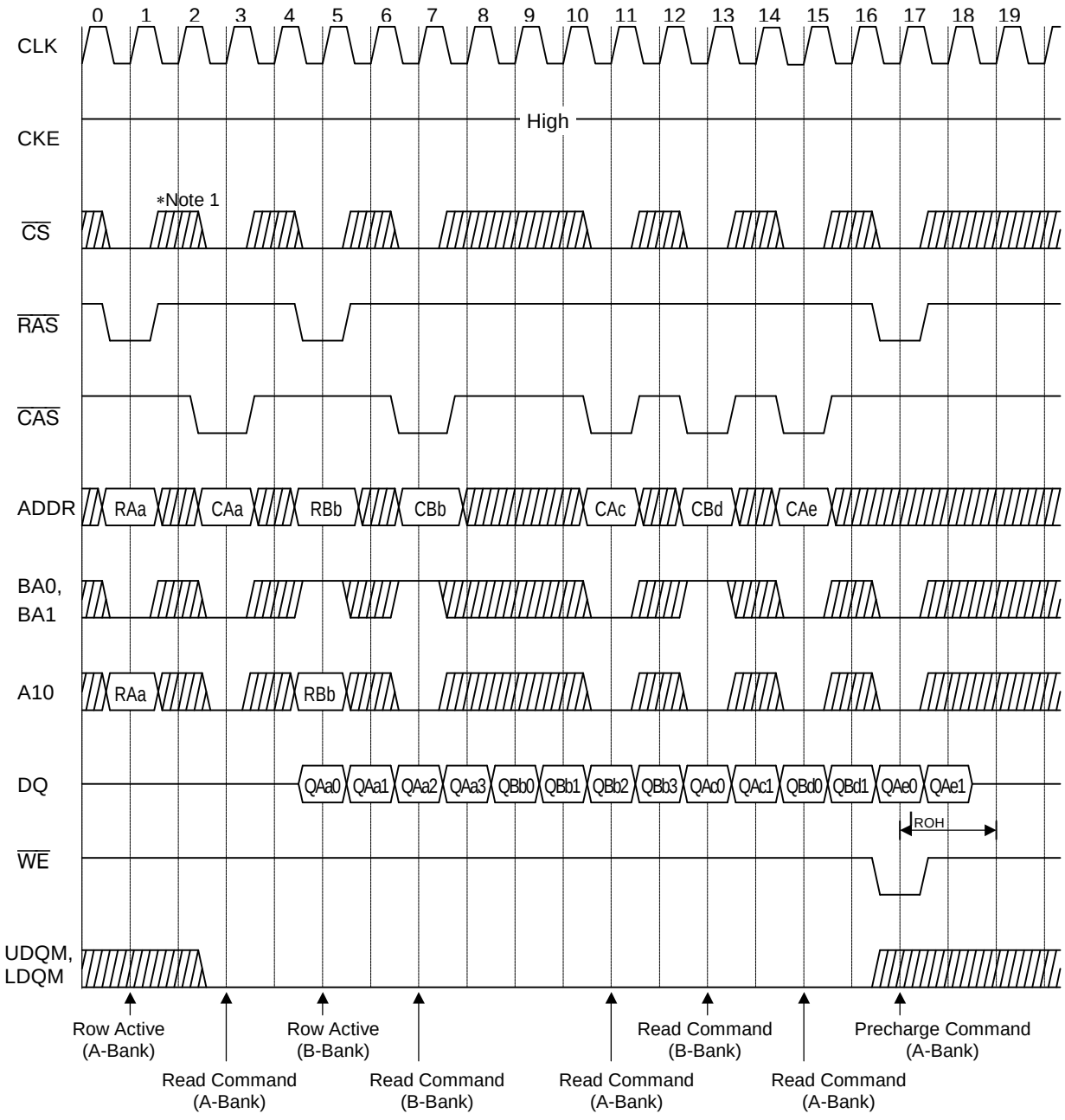
Bank Interleave Random Row Read Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4



Bank Interleave Random Row Write Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

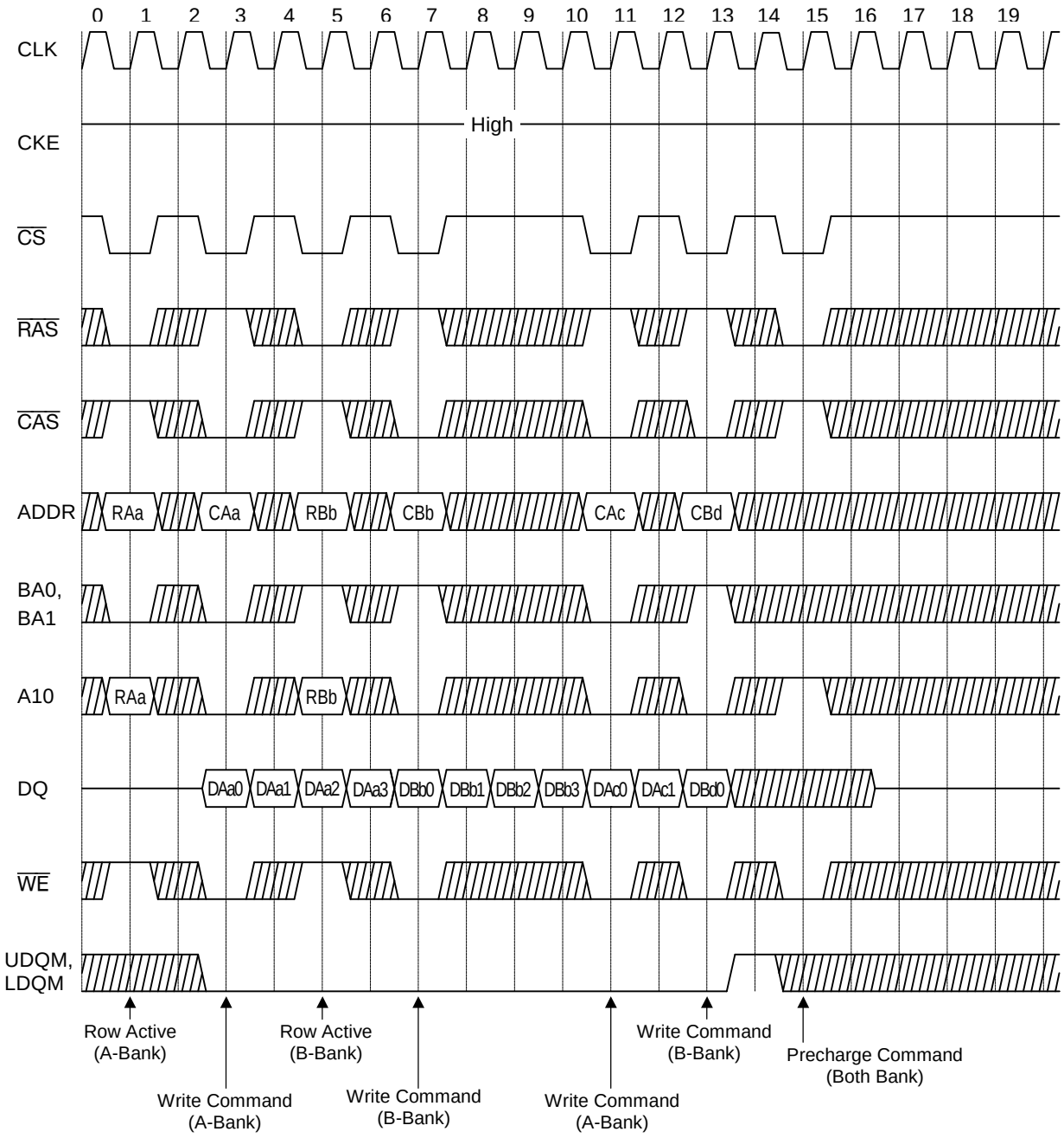


Bank Interleave Page Read Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4

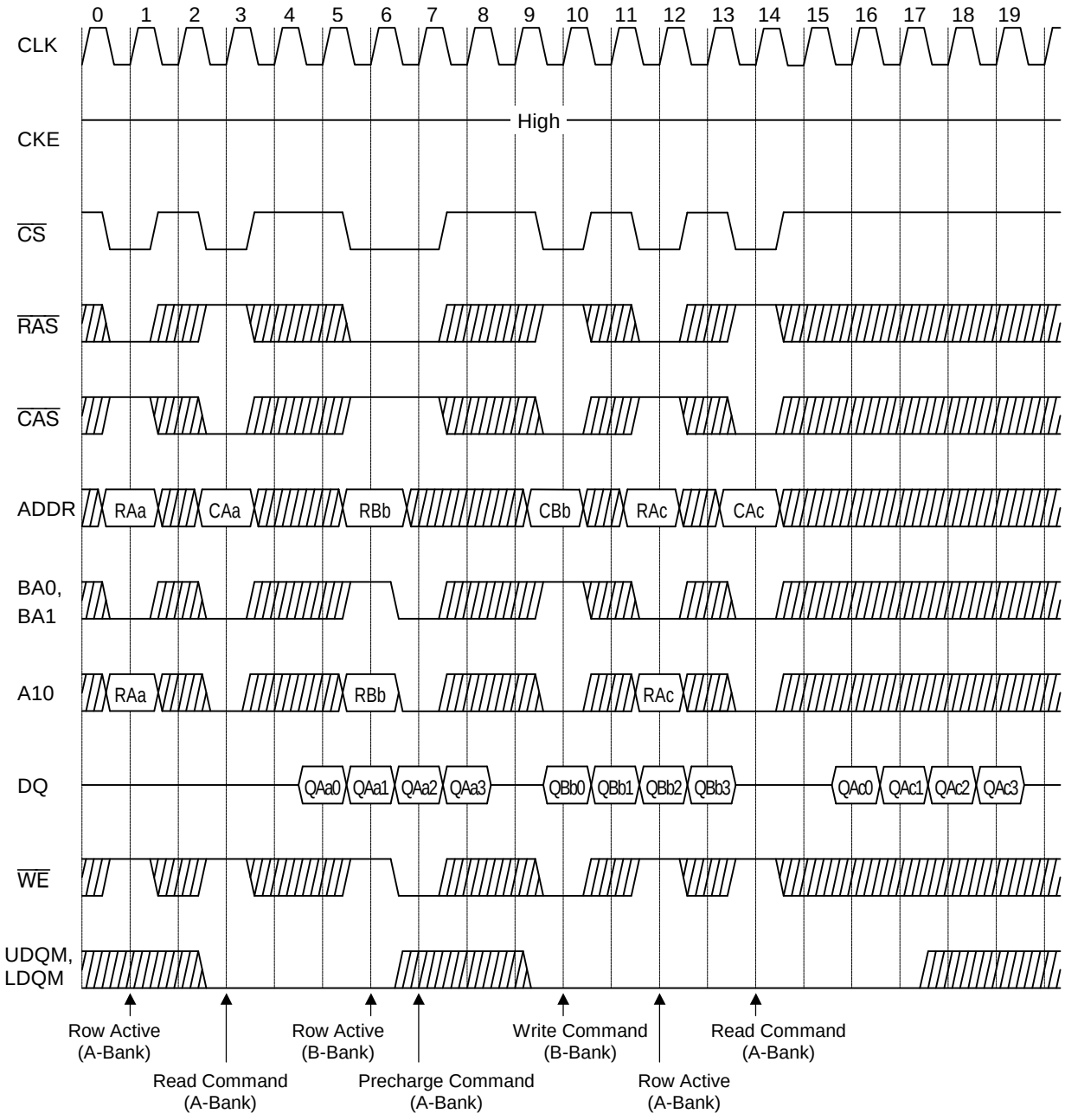


*Note: 1. $\overline{CS}$ is ignored when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the same cycle.

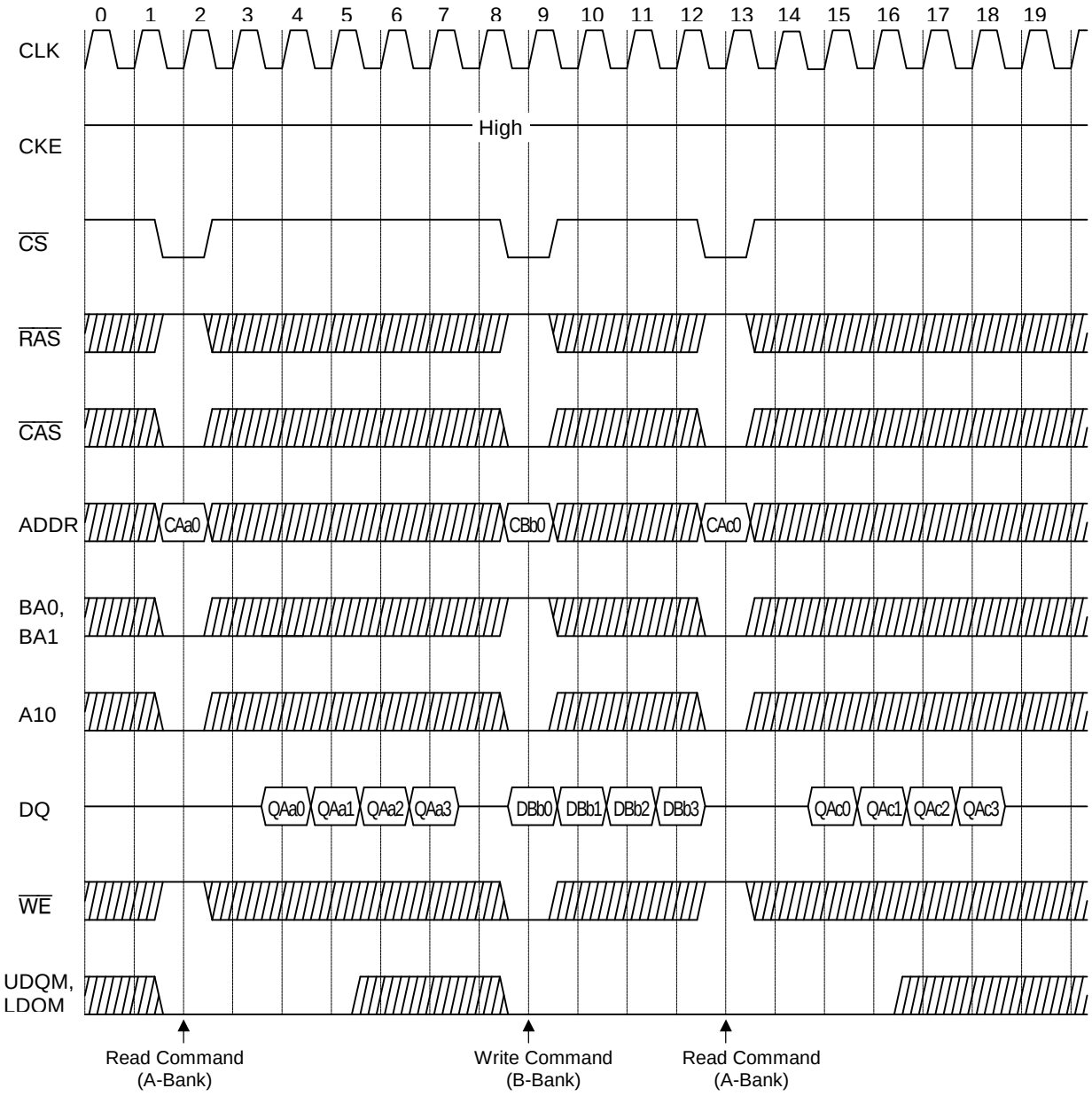
Bank Interleave Page Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4



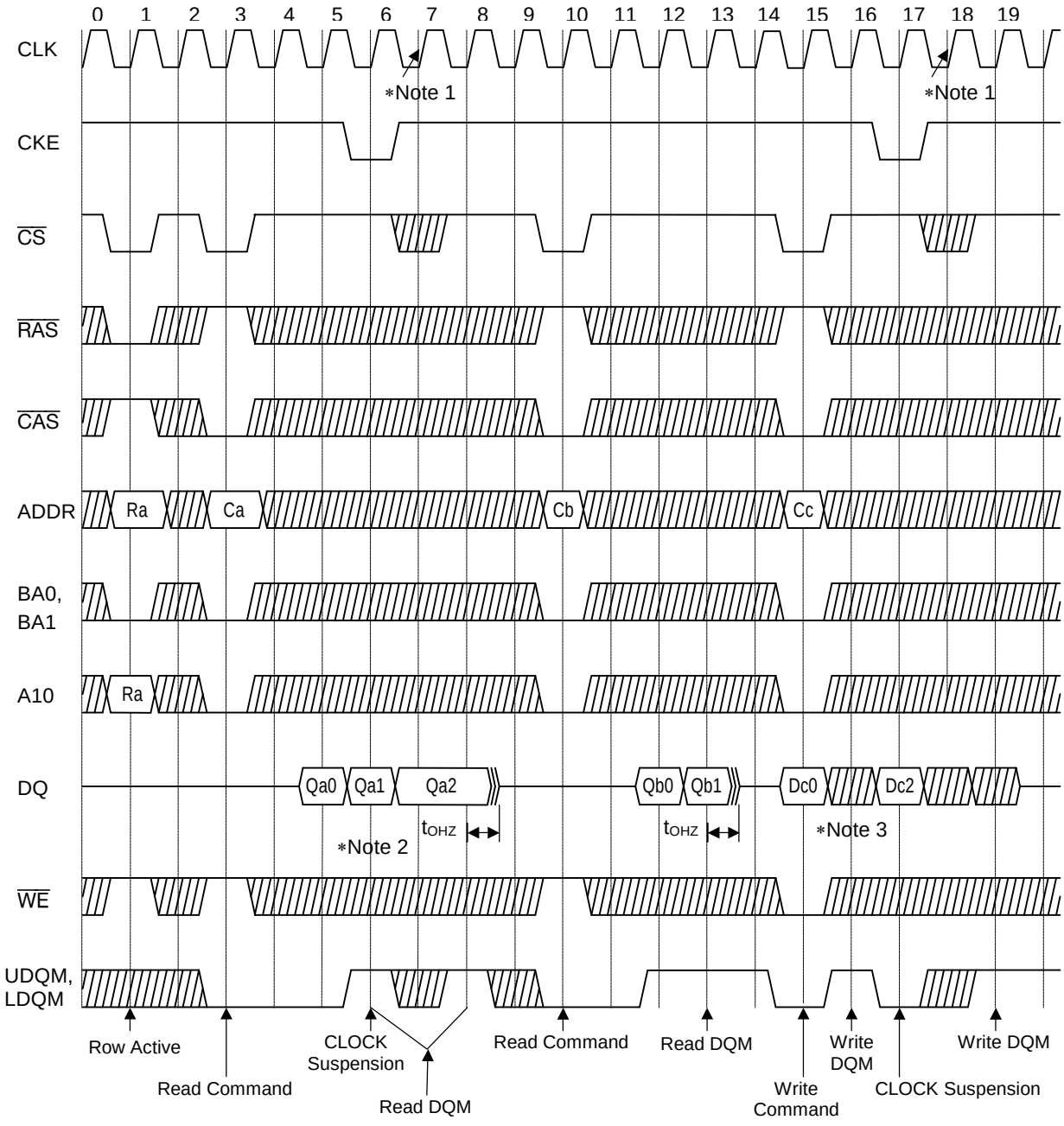
Bank Interleave Random Row Read/Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4

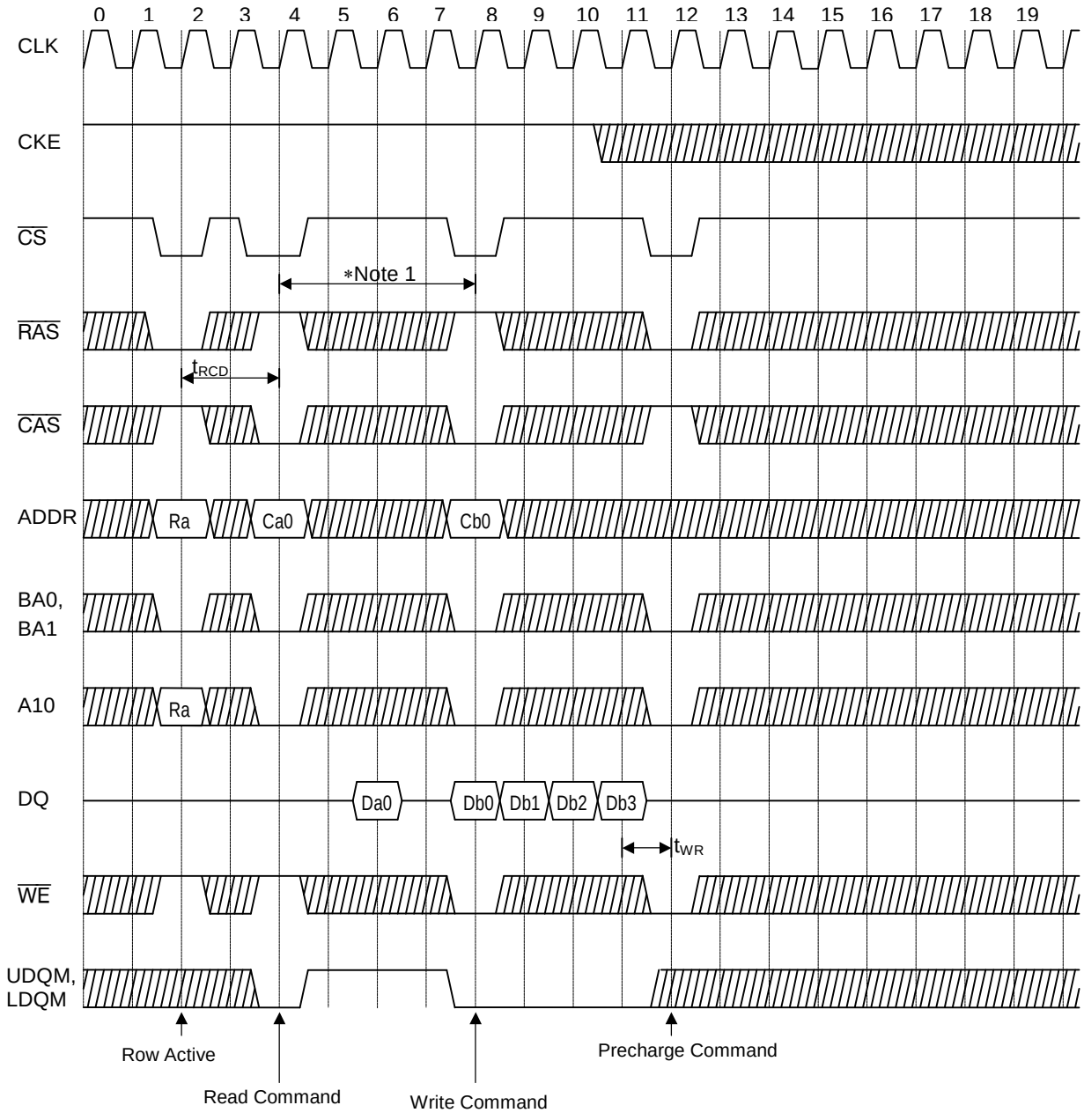


Clock Suspension & DQM Operation Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



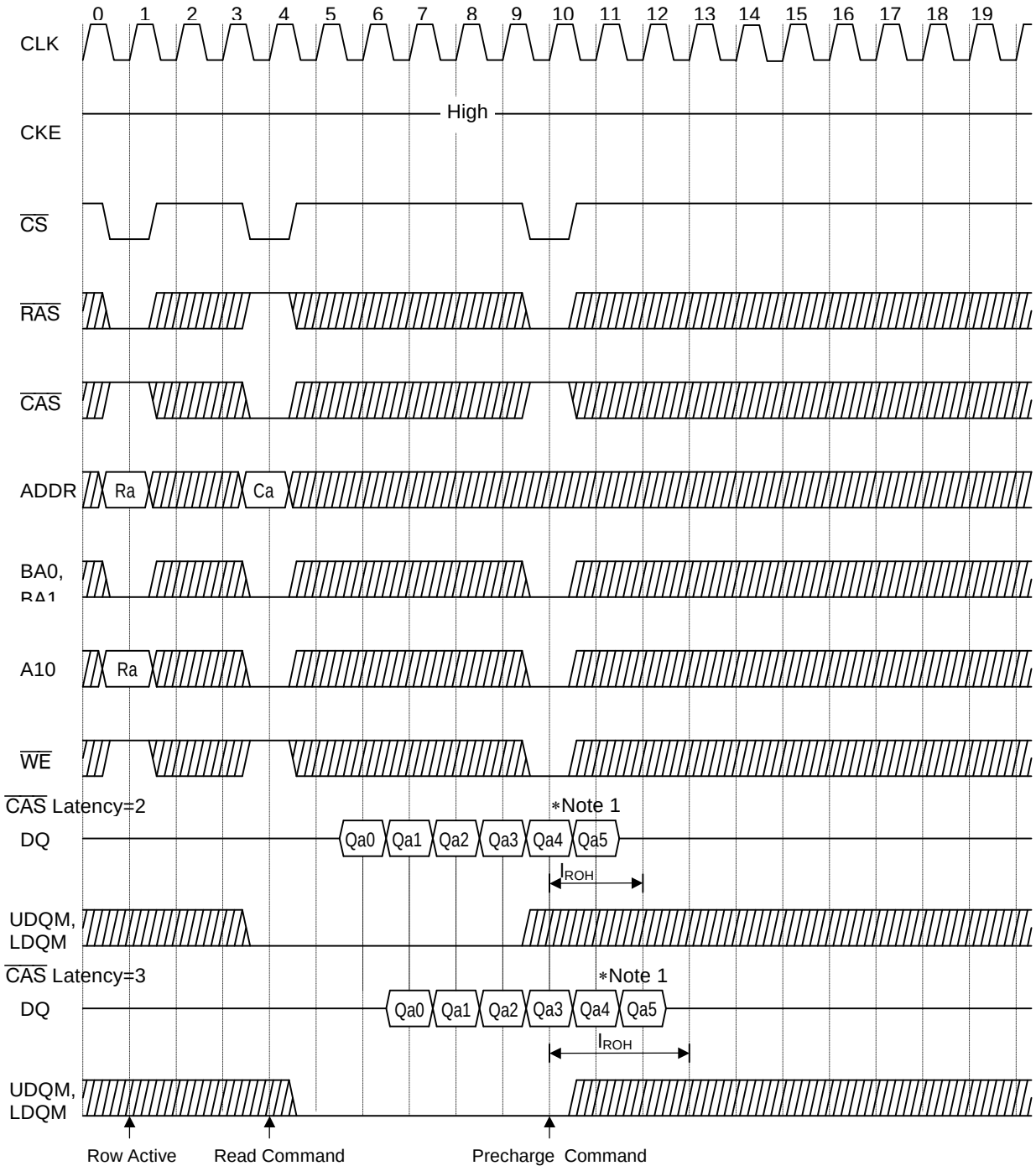
*Note: 1. When Clock Suspension is asserted, the next clock cycle is ignored.
2. When UDQM and LDQM are asserted, the read data after two clock cycles is masked.
3. When UDQM and LDQM are asserted, the write data in the same clock cycle is masked.
4. When LDQM is set High, the input/output data of DQ1 – DQ8 is masked.
5. When UDQM is set High, the input/output data of DQ9 – DQ16 is masked.

Read to Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4



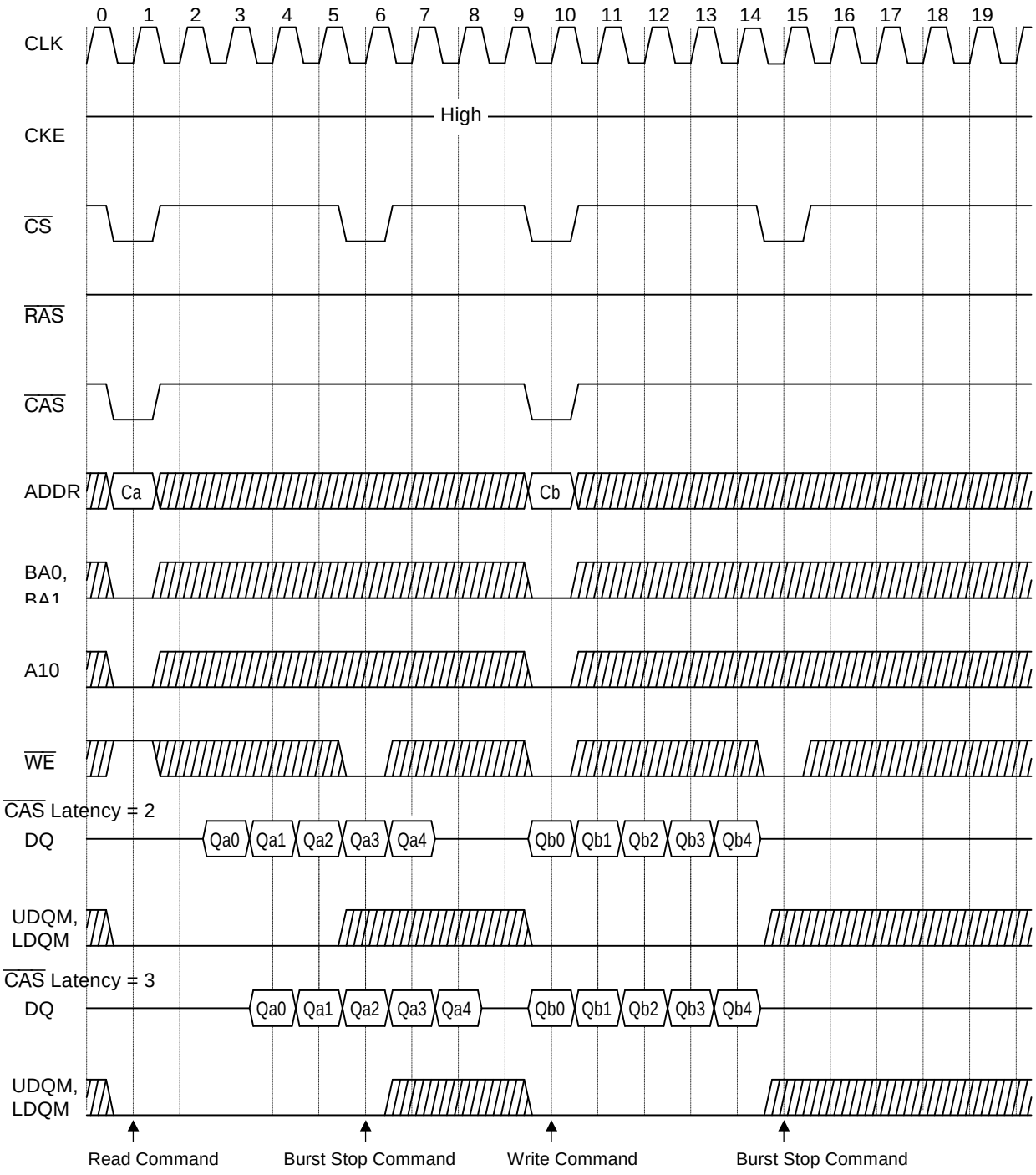
*Note: 1. In Case $\overline{CAS}$ latency is 3, READ can be interrupted by WRITE.
The minimum command interval is [burst length + 1] cycles.
UDQM, LDQM must be high at least 3 clocks prior to the write command.

Read Interruption by Precharge Command @Burst Length = 8

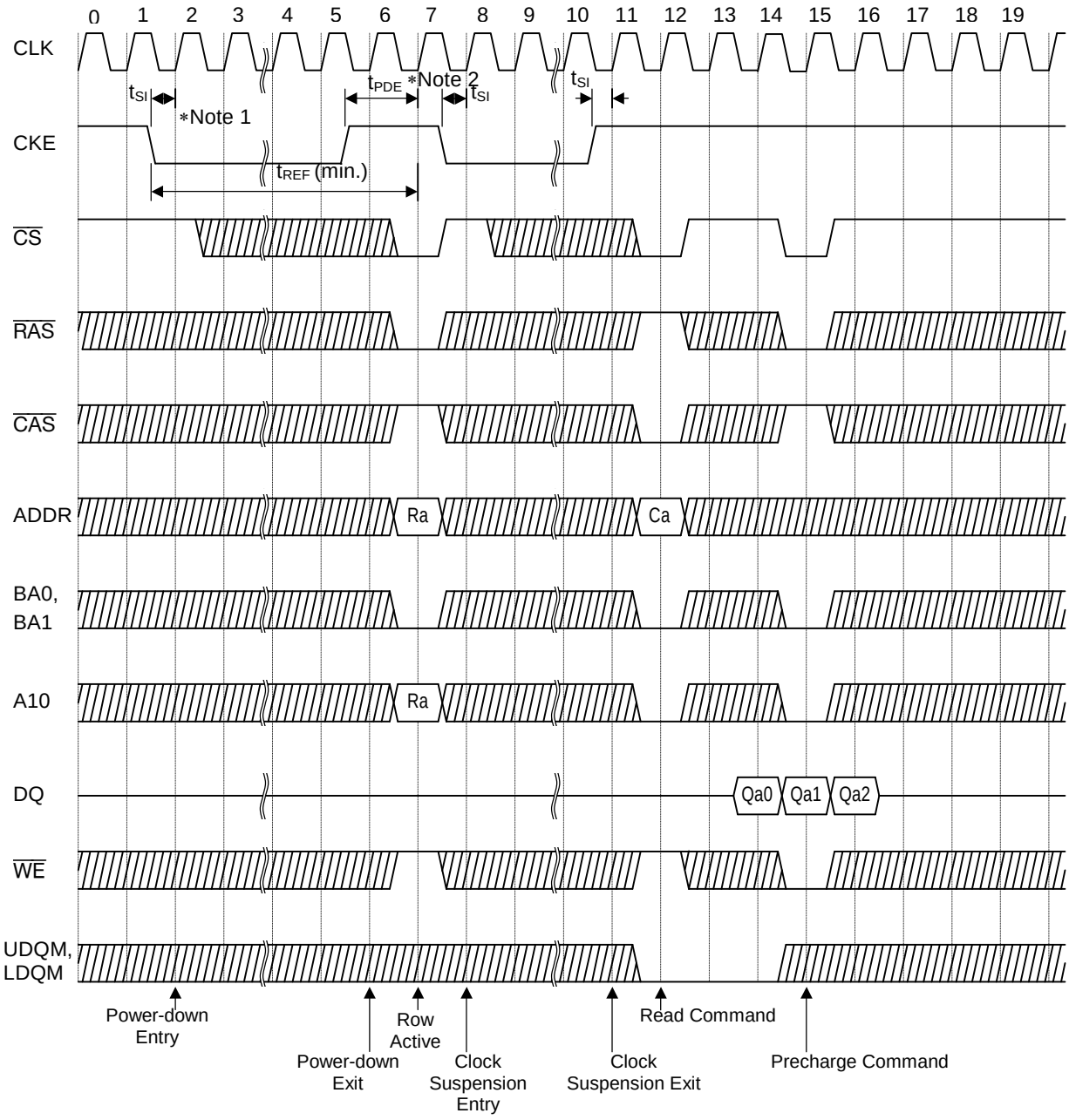


*Note: 1. If row precharge is asserted before a burst read ends, then the read data will not output after l_{ROH} equals $\overline{CAS}$ latency.

Burst Stop Command @Burst Length = 8



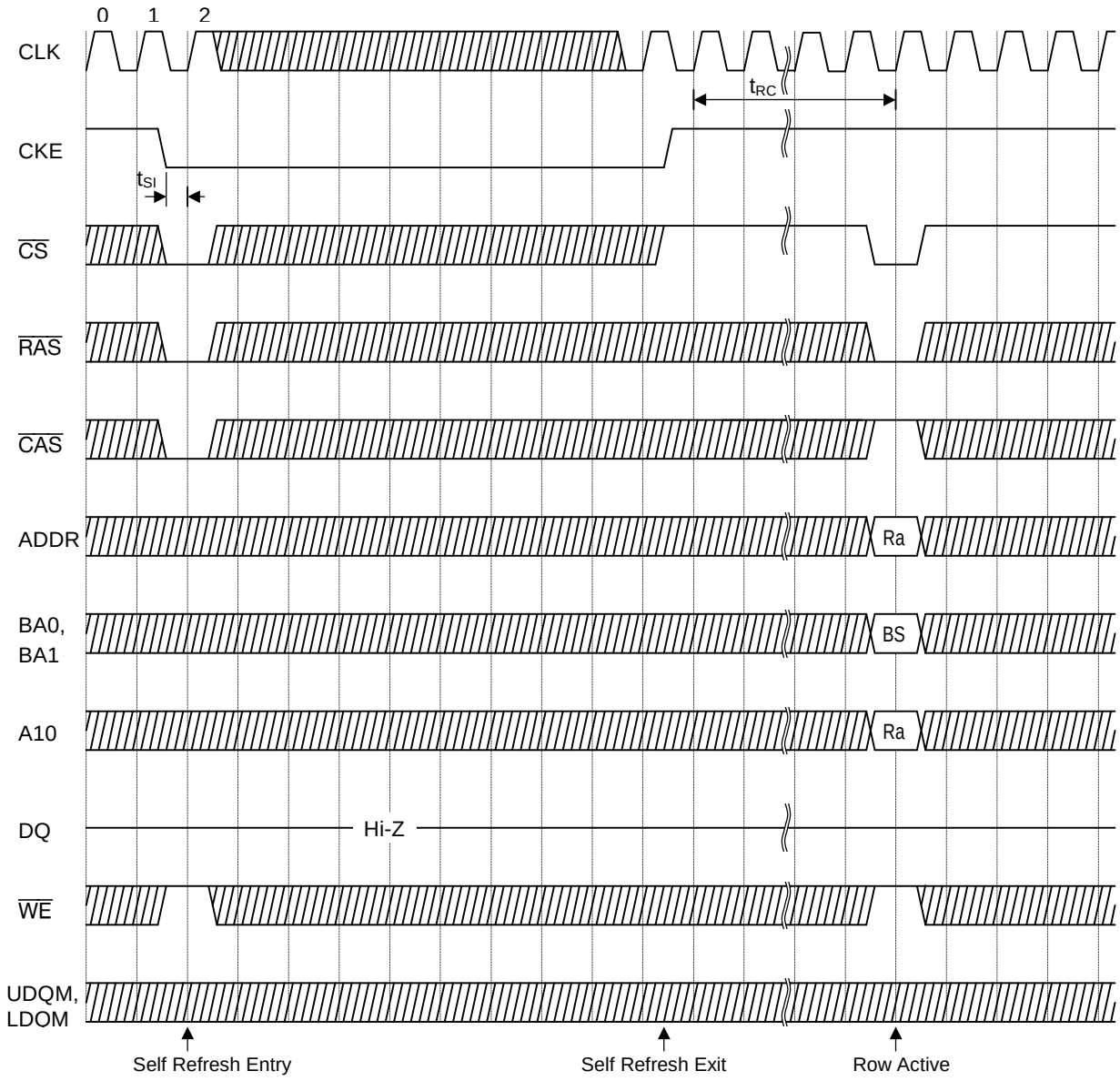
Power Down Mode @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



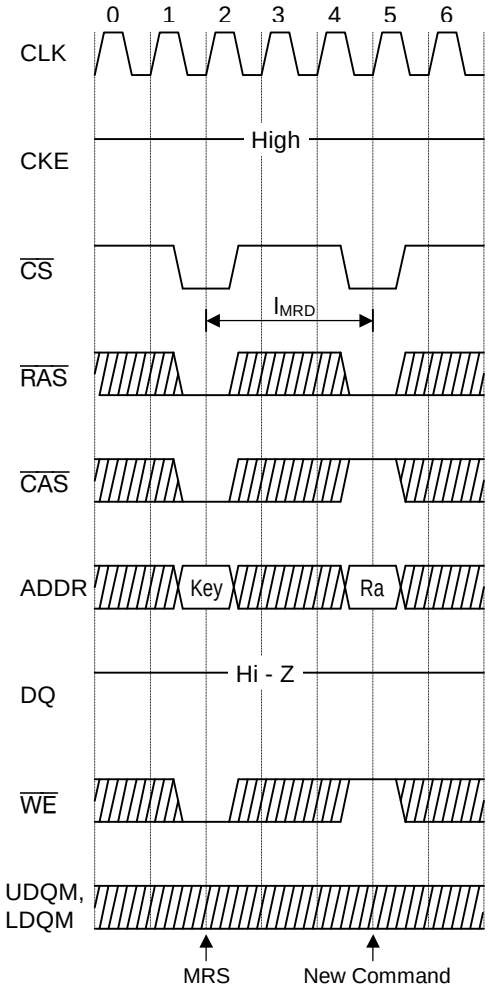
*Note: 1. When both banks are in precharge state, and if CKE is set low, then the MD56V82160 enters power-down mode and maintains the mode while CKE is low.

2. To release the circuit from power-down mode, CKE has to be set high for longer than t_{PDE} (t_{SI} + 1CLK).

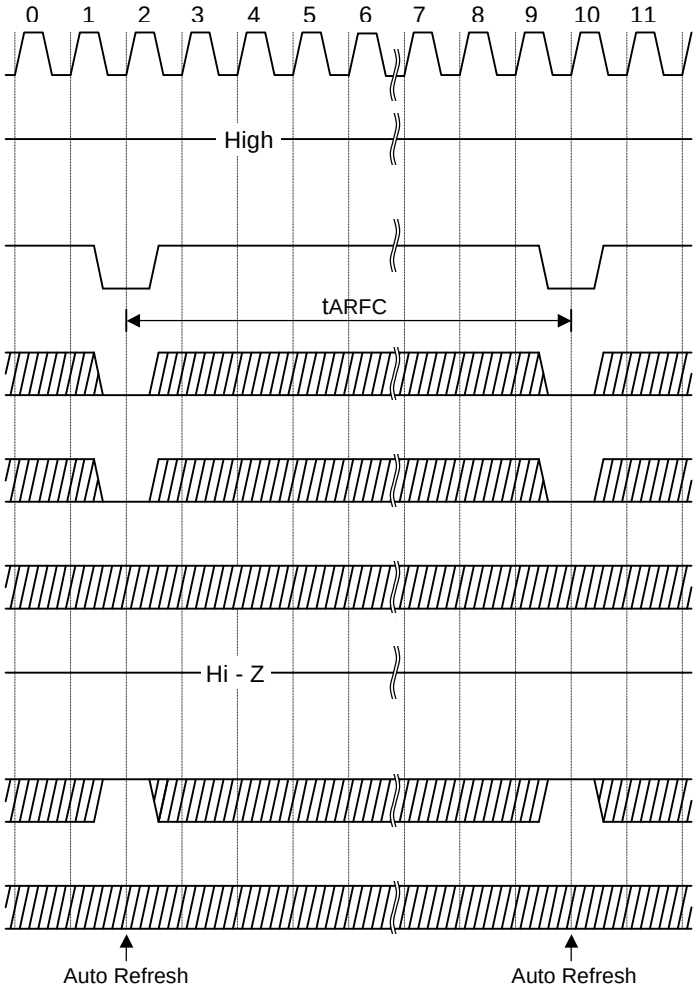
Self Refresh Cycle



Mode Register Set Cycle



Auto Refresh Cycle



FUNCTION TRUTH TABLE (Table 1) (1/3)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Command	Action
Idle	H	X	X	X	X	X	DESL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	BA	X	BST	NOP
	L	H	L	L	BA	CA	RD/RDA	ILLEGAL[1]
	L	H	L	H	BA	CA	WR/WRA	ILLEGAL[1]
	L	L	H	H	BA	RA	ACT	Row Active
	L	L	H	L	BA	A10	PRE/PALL	NOP
	L	L	L	H	X	X	REF	Auto-Refresh
	L	L	L	L	L	OP Code	MRS	Mode Register Write
Row Active	H	X	X	X	X	X	DESL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	BA	X	BST	NOP
	L	H	L	L	BA	CA	RD/RDA	Read[2]
	L	H	L	H	BA	CA	WR/WRA	Write[2]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	Precharge[3]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Read	H	X	X	X	X	X	DESL	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	BST	Term Burst --> Row Active
	L	H	L	L	BA	CA	RD/RDA	Term Burst, start new Burst Read[4]
	L	H	L	H	BA	CA	WR/WRA	Term Burst, start new Burst Write[4,5]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	Term Burst, execute Row Precharge
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Write	H	X	X	X	X	X	DESL	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	BST	Term Burst --> Row Active
	L	H	L	L	BA	CA	RD/RDA	Term Burst, start new Burst Read [4,5]
	L	H	L	H	BA	CA	WR/WRA	Term Burst, start new Burst Write [4]
	L	L	H	H	BA	RA	ACT	ILLEGAL [1]
	L	L	H	L	BA	A10	PRE/PALL	Term Burst, execute Row Precharge [6]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (2/3)

Current State[1]	CS	RAS	CAS	WE	BA	ADDR	Command	Action
Read with Auto Precharge	H	X	X	X	X	X	DESL	Continue Burst to End → Precharging
	L	H	H	H	X	X	NOP	Continue Burst to End → Precharging
	L	H	H	L	BA	X	BST	ILLEGAL
	L	H	L	L	BA	CA	RD/RDA	Support Concurrent auto-precharge[1]
	L	H	L	H	BA	CA	WR/WRA	Support Concurrent auto-precharge[1]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL[1]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	DESL	Continue Burst to End → Write recovering
	L	H	H	H	X	X	NOP	Continue Burst to End → Write recovering
	L	H	H	L	BA	X	BST	ILLEGAL
	L	H	L	L	BA	CA	RD/RDA	Support Concurrent auto-precharge[1]
	L	H	L	H	BA	CA	WR/WRA	Support Concurrent auto-precharge[1]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL[1]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Precharge	H	X	X	X	X	X	DESL	NOP --> Enter idle after t_{RP}
	L	H	H	H	X	X	NOP	NOP --> Enter idle after t_{RP}
	L	H	H	L	BA	X	BST	ILLEGAL
	L	H	L	L	BA	CA	RD/RDA	ILLEGAL[1]
	L	H	L	H	BA	CA	WR/WRA	ILLEGAL[1]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	NOP --> Enter idle after t_{RP}
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Row Active	H	X	X	X	X	X	DESL	NOP --> Enter Bank Active after t_{RCD}
	L	H	H	H	X	X	NOP	NOP --> Enter Bank Active after t_{RCD}
	L	H	H	L	BA	X	BST	ILLEGAL
	L	H	L	L	BA	CA	RD/RDA	ILLEGAL[1]
	L	H	L	H	BA	CA	WR/WRA	ILLEGAL[1]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1,7]
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL[1]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Write Recovery	H	X	X	X	X	X	DESL	NOP→Enter row active after tWR
	L	H	H	H	X	X	NOP	NOP→Enter row active after tWR
	L	H	H	L	BA	X	BST	NOP→Enter row active after tWR
	L	H	L	L	BA	CA	RD/RDA	Begin read
	L	H	L	H	BA	CA	WR/WRA	Begin new write
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL[1]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (3/3)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Command	Action
Write Recovery with auto precharge	H	X	X	X	X	X	DESL	NOP→Enter precharge after tWR
	L	H	H	H	X	X	NOP	NOP→Enter precharge after tWR
	L	H	H	L	BA	X	BST	NOP→Enter precharge after tWR
	L	H	L	L	BA	CA	RD/RDA	ILLEGAL
	L	H	L	H	BA	CA	WR/WRA	ILLEGAL[1,5]
	L	L	H	H	BA	RA	ACT	ILLEGAL[1]
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL[1]
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Refresh	H	X	X	X	X	X	DESL	NOP --> Enter idle after t_{RC}[1]
	L	H	H	H	X	X	NOP	NOP --> Enter idle after t_{RC}[1]
	L	H	H	L	BA	X	BST	NOP --> Enter idle after t_{RC}[1]
	L	H	L	L	BA	CA	RD/RDA	ILLEGAL
	L	H	L	H	BA	CA	WR/WRA	ILLEGAL
	L	L	H	H	BA	RA	ACT	ILLEGAL
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL
Mode Register Access	H	X	X	X	X	X	DESL	NOP --> Enter idle after t_{MRD}
	L	H	H	H	X	X	NOP	NOP --> Enter idle after t_{MRD}
	L	H	H	L	BA	X	BST	NOP --> Enter idle after t_{MRD}
	L	H	L	L	BA	CA	RD/RDA	ILLEGAL
	L	H	L	H	BA	CA	WR/WRA	ILLEGAL
	L	L	H	H	BA	RA	ACT	ILLEGAL
	L	L	H	L	BA	A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	X	REF	ILLEGAL
	L	L	L	L	L	OP Code	MRS	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No OPeration command

CA = Column Address AP = Auto Precharge

∗Notes : 1.Illegal to bank in specified states;Function may be legal in the bank indicated by Bank Address(BA), depending on the state of that bank.

2. Illegal if tRCD is not satisfied.
3. Illegal if tRAS is not satisfied.
4. Must satisfy burst interrupt condition.
5. Must satisfy bus contention,bus turn around,and/or write recovery requirements.
6. Must mask preceding data which don't satisfy tWR.
7. Illegal if tRRD is not satisfied.

FUNCTION TRUTH TABLE for CKE (Table 2)

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	Action
Self Refresh[8]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down[8]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL [6]
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle[9] (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

*Notes : 8. If the minimum set-up time t_{PDE} is satisfied when CKE transition from "L" to "H", CKE operates asynchronously so that a command can be input in the same internal clock cycle.
Before and after self-refresh mode,execute auto-refresh to all refresh addresses in or within tREF(max.) period on the condition (1) and (2) below.
(1) Enter self-refresh mode within time(tREF(max.)/refresh cycles) after either burst refreh or distributed refresh at equal interval to all refresh addresses are completed.
(2) Start burst refreh or distributed refresh at equal interval to all refresh addresses within time(tREF(max.)/refresh cycles) after exiting selfrefresh mode.

9. Power-down and self-refresh can be entered only when all the banks are in an idle state.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD56V82160-01	Feb. 14, 2008	–	–	First edition from PEDD56V82160-05

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