MD6001, F (SILICON)
MD6002, F
MD6003, F
MQ6001, MQ6002

MULTIPLE SILICON ANNULAR TRANSISTORS

. . . designed for use as differential amplifiers, dual general-purpose switches and amplifiers, front end detectors, and temperature compensation amplifiers, where complementary devices are required.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 150 mAdc
- Fast Switching Times – t_{on} = 28 ns (Typ) and t_{off} = 72 ns (Typ)
- DC Current Gain Specified – 0.1 mAdc to 300 mAdc
- High Current-Gain–Bandwidth Product – f_T = 340 MHz (Typ) @ I_C = 50 mAdc

NPN, PNP SILICON MULTIPLE TRANSISTORS

MAXIMUM RATINGS

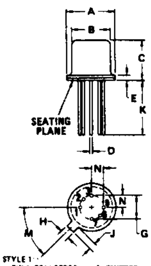
Rating	Symbol	MD6003 MD6003F	MD6001,F MD6002,F MQ6001,2	Unit
Collector-Emitter Voltage	V_{CEO}	30		Vdc
Collector-Base Voltage	V_{CB}	50	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	500		mAdc
		One Die	All Die Equal Power	
Total Power Dissipation @ T_A = 25°C	P_D			mW
MD6001,2,3		575	625	
MD6001F,2F,3F		350	400	
MQ6001,2		400	600	
Derate above 25°C				mW/°C
MD6001,2,3		3.29	3.57	
MD6001F,2F,3F		2.0	2.28	
MQ6001,2		2.28	3.42	
Total Power Dissipation @ T_C = 25°C	P_D			Watts
MD6001,2,3		1.8	2.5	
MD6001F,2F,3F		1.0	2.0	
MQ6001,2		0.9	3.6	
Derate above 25°C				mW/°C
MD6001,2,3		10.3	14.3	
MD6001F,2F,3F		5.71	11.4	
MQ6001,2		5.13	20.5	
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	One Die	All Die Equal Power	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)			°C/W
MD6001,2,3		304	280	
MD6001F,2F,3F		500	438	
MQ6001,2		438	292	
Thermal Resistance, Junction to Case	$R_{\theta JC}$			°C/W
MD6001,2,3		97	70	
MD6001F,2F,3F		175	87.5	
MQ6001,2		195	48.8	
		Junction to Ambient	Junction to Case	
Coupling Factor				%
MD6001,2,3		84	44	
MD6001F,2F,3F		75	0	
MQ6001,2 (Q1-Q2)		57	0	
(Q1-Q3 or Q1-Q4)		55	0	

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

MD6001
MD6002
MD6003

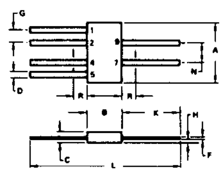


STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. OMITTED
5. EMITTER
6. BASE
7. COLLECTOR
8. OMITTED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.70	0.150	0.185
D	0.41	0.53	0.016	0.021
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 654-07

MD6001F
MD6002F
MD6003F

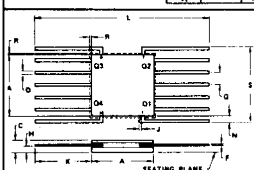


STYLE 1
PIN 1. BASE
2. EMITTER
4. EMITTER
5. BASE
7. COLLECTOR
9. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	7.36	0.240	0.290
B	2.92	4.06	0.115	0.160
C	0.76	2.03	0.030	0.080
D	0.36	0.48	0.014	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	–	0.89	–	0.035
K	3.81	–	0.150	–
N	2.54 BSC		0.100 BSC	
R	–	1.27	–	0.050

CASE 610A-03

MQ6001
MQ6002



STYLE 1
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NOT CONNECTED
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NOT CONNECTED
12. EMITTER
13. BASE
14. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.080
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

CASE 607-04

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

Where ΔT_{J1} is the change in junction temperature of die 1
$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4
P_{D1} thru 4 is the power dissipation in die 1 through 4
$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

Where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4P_D$ equation (3) can be further simplified and by substituting into equation (2) results in

(4) $R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4}) /4$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	MD6003,F	BV_{CBO}	50	–	–	Vdc
	MD6001,F, MD6002,F, MQ6001, MQ6002		60	–	–	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	5.0	–	–	Vdc
Collector-Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	MD6003,F	I_{CBO}	–	–	100	nA
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 3.0 Vdc)	MD6003,F	I_{CEV}	–	–	30	nAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	MD6001,F,2,F, MQ6001,2		–	–	20	nAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 3.0 Vdc, T_A = 150°C)	MD6001,F,2,F, MQ6001,2		–	–	30	μAdc
Base Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 3.0 Vdc)	MD6003,F	I_{BEV}	–	–	50	nAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	MD6001,F,2,F,MQ6002,F		–	–	30	
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	MD6001,F, MQ6001	h_{FE}	20	80	–	–
	MD6002,F, MQ6002		35	70	–	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	MD6001,F, MQ6001		25	90	–	
	MD6003,F		40	70	–	
	MQ6002,F, MQ6002		50	100	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	MD6001,F, MQ6001		35	70	–	
	MD6002,F, MQ6002		75	110	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)	MD6001,F, MQ6001		40	–	120	
	MD6003,F		70	110	–	
	MD6002,F, MQ6002		100	200	300	
(I_C = 300 mAdc, V_{CE} = 10 Vdc)	MD6001,F, MQ6001		20	–	–	
	All Other Devices		30	90	–	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)	MD6001,F, MQ6001		20	80	–	
	MD6002,F, MQ6002		50	–	–	
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	All Devices	$V_{CE(sat)}$	–	0.3	0.4	Vdc
(I_C = 300 mAdc, I_B = 30 mAdc)	MD6001, MD6002,F, MQ6001,2		–	0.59	1.4	
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	All Devices	$V_{BE(sat)}$	–	1.02	1.3	Vdc
(I_C = 300 mAdc, I_B = 30 mAdc)	MD6001, MD6002,F, MQ6001,2		–	1.25	2.0	

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	200	340	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	5.6	8.0	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	16	30	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Turn-On Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) MD6001F,2F, MQ6001,2	t_{on}	–	28	60	ns
Delay Time		t_d	–	–	20	ns
Rise Time		t_r	–	–	40	ns
Turn-Off Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) MD6001F,2F, MQ6001,2	t_{off}	–	72	350	ns
Storage Time		t_s	–	–	280	ns
Fall Time		t_f	–	–	70	ns

FIGURE 1 – DC CURRENT GAIN

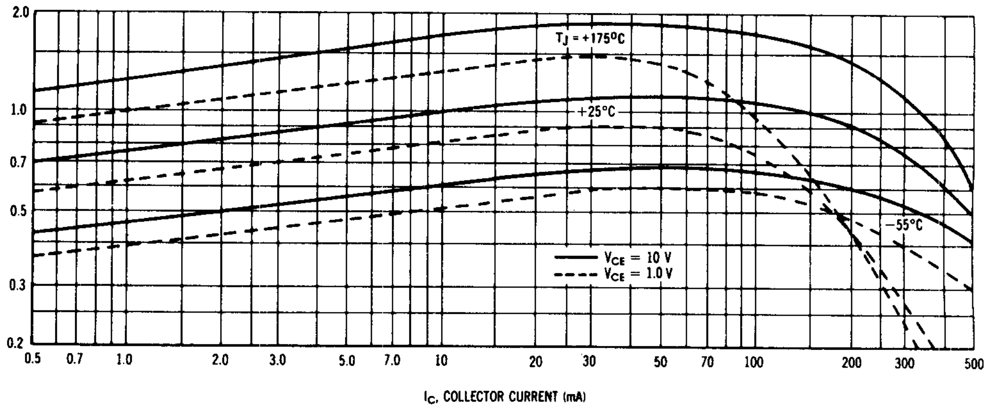


FIGURE 2 – "ON" VOLTAGES

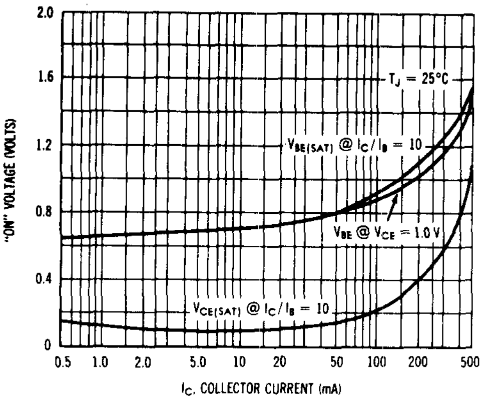
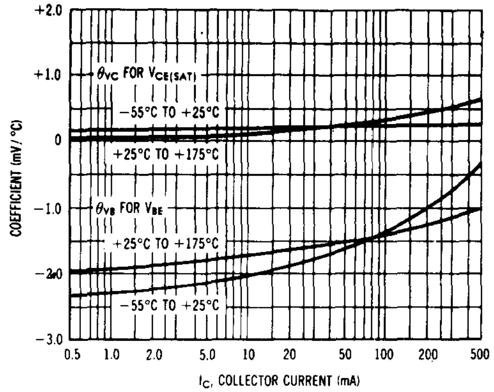


FIGURE 3 – TEMPERATURE COEFFICIENTS



NOISE FIGURE

$V_{CE} = 10$ V, $T_A = 25°C$

FIGURE 4 – FREQUENCY EFFECTS

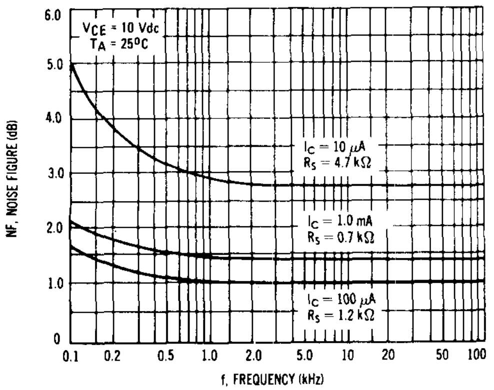


FIGURE 5 – SOURCE RESISTANCE EFFECTS

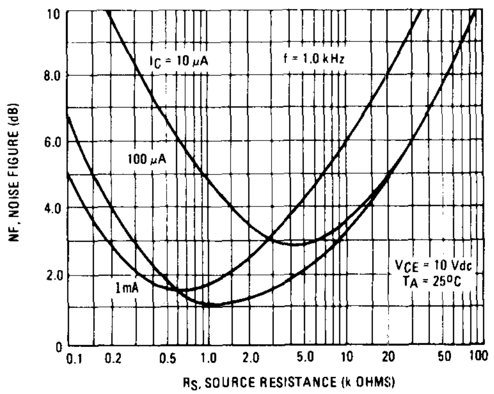


FIGURE 6 – CURRENT-GAIN BANDWIDTH PRODUCT

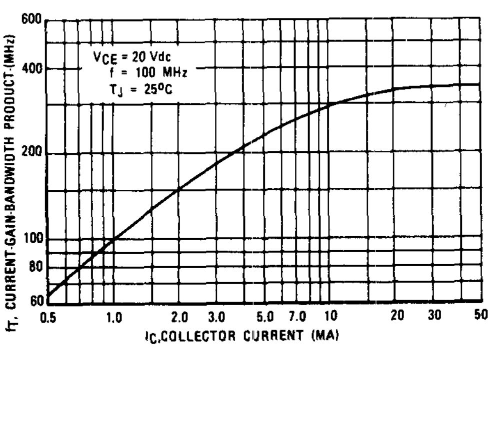


FIGURE 7 – CAPACITANCE

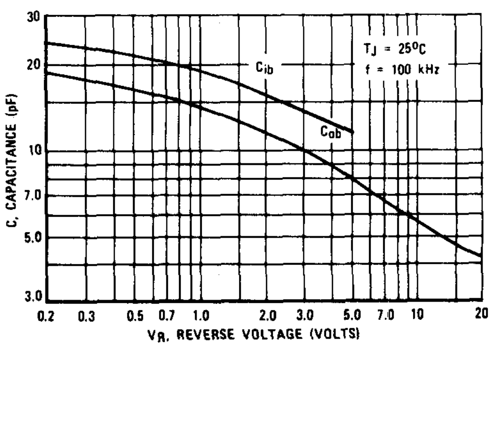


FIGURE 8 — TURN ON TIME

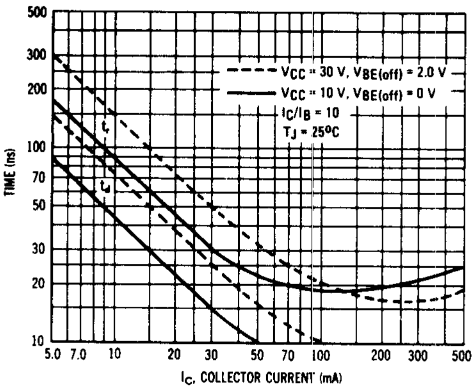


FIGURE 9 — CHARGE DATA

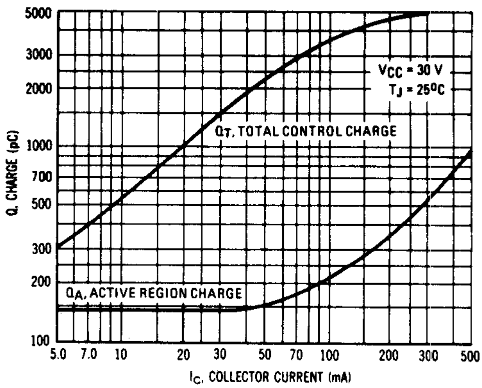


FIGURE 10 — STORAGE TIME

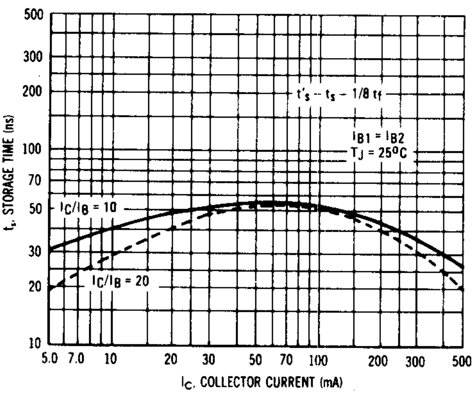


FIGURE 11 — FALL TIME

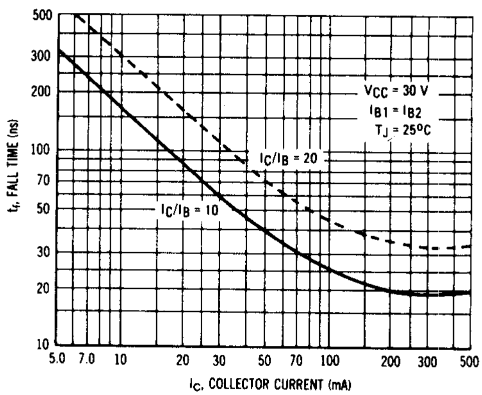


FIGURE 12 — DELAY AND RISE TIME TEST CIRCUIT

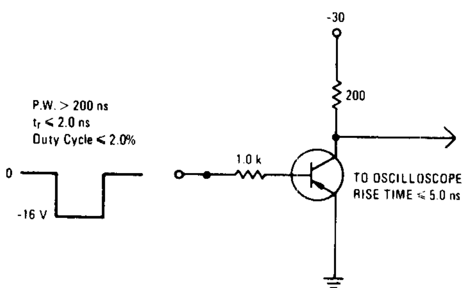
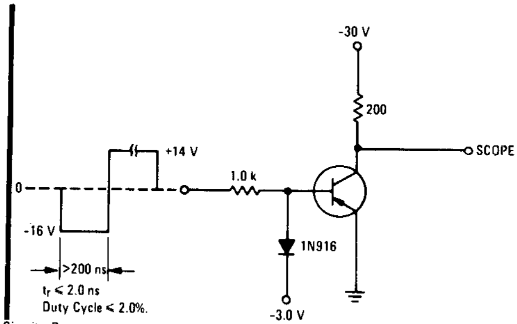


FIGURE 13 — STORAGE AND FALL TIME TEST CIRCUIT



For NPN Test Circuits, Reverse Diode and all Voltage Polarities.