

T-49-19-08

MHS

data sheet

80C51/80C31

CMOS SINGLE - CHIP 8 BIT MICROCONTROLLER

PRELIMINARY

OCTOBER 1987

- 80C51 - CMOS SINGLE-CHIP 8 BIT MICROCONTROLLER with factory mask-programmable ROM.
- 80C31 - ROM LESS VERSION OF THE 80C51

OTHER DEVICES
WITH A SPECIFIC
DATA SHEET

- 80C51/31 : 0 TO 12 MHz.
- 80C51/31-1 : 0 TO 16 MHz.
- 80C51/31-L : Vcc = 2.7V TO 6V (0 TO 6 MHz)
- 80C51F : THE INTERNAL ROM CODE CANNOT BE READ OR DUMPED AFTER ACTIVATION OF A SPECIAL PROTECTION

Features

- POWER CONTROL MODES
- 128 x 8 BIT RAM
- 32 PROGRAMMABLE I/O LINES
- TWO 16-BIT TIMER/COUNTERS
- 64K PROGRAM MEMORY SPACE
- FULLY STATIC DESIGN
- HIGH PERFORMANCE SAJI VI CMOS PROCESS
- BOOLEAN PROCESSOR
- 5 INTERRUPT SOURCES
- PROGRAMMABLE SERIAL PORT
- 64K DATA MEMORY SPACE
- TEMPERATURE RANGE : Commercial, Industrial and Military

Description

MHS's 80C51 and 80C31 are high performance CMOS versions of the 8051/8031 NMOS single chip 8 bit μ C and is manufactured using a self-aligned silicon gate CMOS process (SAJI VI).

The fully static design of the MHS 80C51/80C31 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The 80C51 retains all the features of the 8051 : 4K bytes of ROM ; 128 bytes of RAM ; 32 I/O lines ; two 16 bit timers a 5-source, 2-level interrupt structure ; a full duplex serial port ; and on-chip oscillator and clock circuits.

In addition, the 80C51 has two software-selectable modes of reduced activity for further reduction in power consumption. In the Idle Mode the CPU is frozen while the RAM, the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode the RAM is saved and all other functions are inoperative.

The 80C31 is identical to the 80C51 except that it has no on-chip ROM.

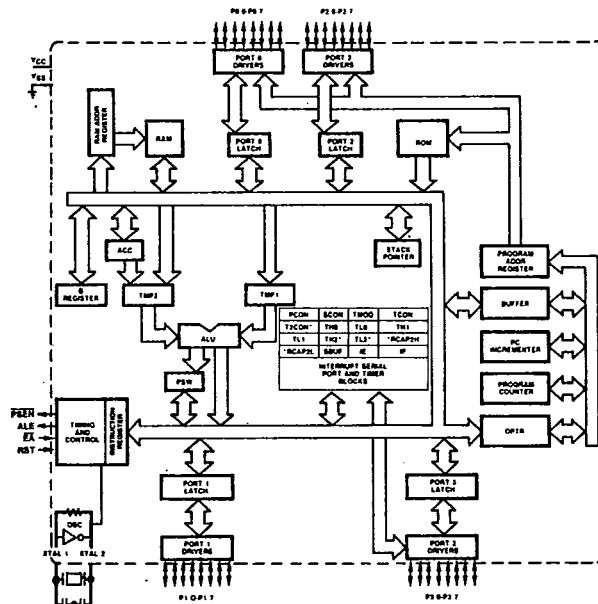


Figure 1. Block Diagram
4-2



80C51/80C31

T-49-19-08

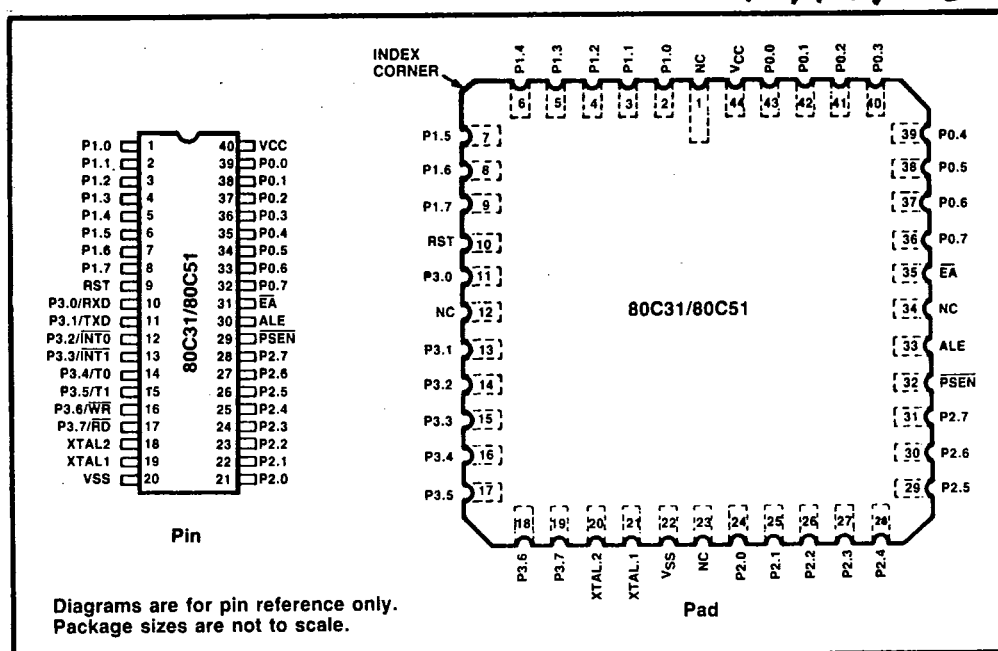


Figure 2. Configurations

IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is gated off.

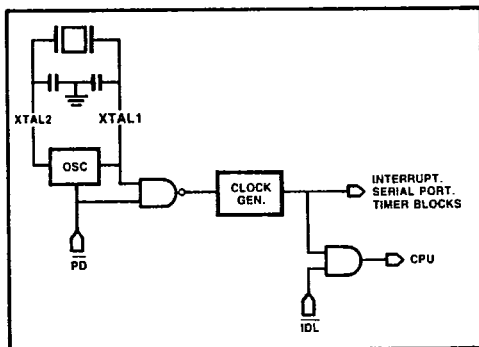


Figure 3. Idle and Power Down Hardware

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON : Power Control Register

(MSB)	SMOD	—	—	—	GF1	GF0	PD	IDL	(LSB)
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Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
—	PCON.6	(Reserved)
—	PCON.5	(Reserved)
—	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes precedence. The reset value of PCON is (0XXX0000).



80C51/80C31

7-49-19-08

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other registers maintain their data during Idle. Table 1 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote a 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. A hardware reset is the only way of exiting the power down mode. The hardware reset initiates the Special Function Register (see Table 1).

In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, p1, shown in Figure 4.

Due to static design, the MHS 80C31/C51 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

80C51 I/O PORTS

The I/O port drive of the 80C51 is similar to the 8051. The I/O buffers for Ports 1, 2, and 3 are implemented as shown in figure 4.

When the port latch contains a 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, p1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET p3 turns on through the inverter to supply the IOH source current. This inverter and p3 form a latch which holds the 1 and is supported by p2.

When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have is strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as I_{TL} under the D.C. Specifications. When the input goes below approximately 2V, p3 turns off to save ICC current. Note, when returning to a logical 1, p2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

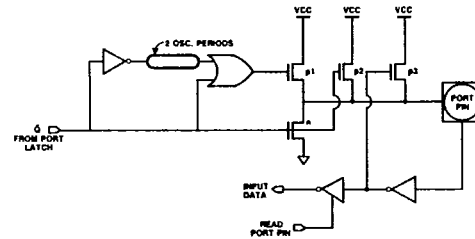


Fig. 4 : I/O Buffers in the 80C51 (Ports 1, 2, 3)

80C31/80C51 PIN DESCRIPTIONS

VSS

Circuit ground potential

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data



80C51/80C31

7-49-19-08

Memory. In this application it uses strong internal pull-ups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C51. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during program verification. In the 80C51, Port 1 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the 80C51. Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the pullups. It also serves the functions of various special features of the MCS-51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	TO (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to VCC.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE

is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

PSEN

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

EA

When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 0FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in figure 5. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in figure 6. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

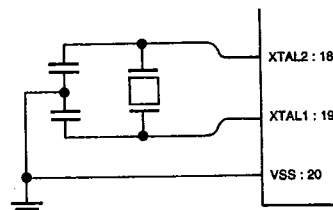


Figure 5. Crystal Oscillator

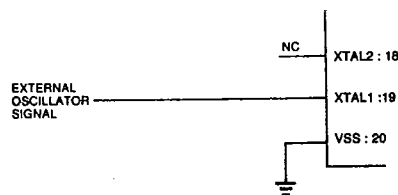


Figure 6. External Drive Configuration



5868455 MATRA DESIGN SEMICOND

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80C51/80C31

T-49-19-08

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias : commercial 0°C to 70°C
 industrial - 40°C to + 85°C
 Storage Temperature - 65°C to + 150°C
 Voltage on VCC to VSS - 0.5V to + 7V
 Voltage on Any Pin to VSS.. - 0.5V to VCC + 0.5V
 Power Dissipation 200mW

**NOTICE : Stresses at or above those listed under «Absolute Maximum Ratings» may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*

DC CHARACTERISTICS (see Note 2)

(TA = 0°C to 70°C ; VCC = 5V ± 20% ; VSS = 0V)

Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	- 0.5	0.2 VCC - 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 0.9	VCC + 0.5	V	
VIH1	Input High Voltage (RST and XTAL1)	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6 mA (note 1)
VOL1	Output Low Voltage Port 0, ALE, PSEN		0.45	V	IOL = 3.2 mA (note 1)
VOH	Output High Voltage Ports 1, 2, 3	0.9 VCC		V	IOH = - 10µA
		0.75 VCC		V	IOH = - 25 µA
		2.4		V	IOH = - 60 µA VCC = 5V ± 10 %
VOH1	Output High Voltage (Port 0 (Port 0, ALE, PSEN)	0.9 VCC		V	IOH = - 40 µA
		0.75 VCC		V	IOH = - 150 µA
		2.4		V	IOH = - 400 µA VCC = 5V ± 10 %
IIL	Logical 0 Input Current Ports 1, 2, 3		- 50	µA	Vin = 0.45V
ILI	Input Leakage Current (Port 0, EA)		± 10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		- 650	µA	Vin = 2.0V
IPD	Power Supply Current (Power Down Mode)		50	µA	VCC = 2.0V (note 2)
RRST	RST Pulldown Resistor	40	125	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	f _c = 1 MHz, T _A = 25°C
ICC	Power supply current Active mode 12 MHz Idle mode 12 MHz		20	mA	(notes 1,2)
			5	mA	

4



T-49-19-08

Note 1 :

ICC max is given by :

Active Mode : $ICCMAX = 1.47 \times FREQ + 2.35$

Idle Mode : $ICCMAX = 0.33 \times FREQ + 1.05$

where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See Figure 1.

See figures 1 through 5 for ICC test conditions.

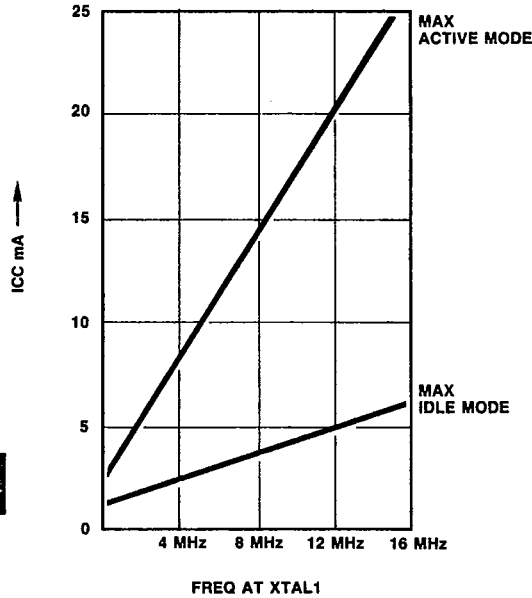


Figure 1 : ICC vs. Frequency.
Valid only within frequency specifications of the device under test.

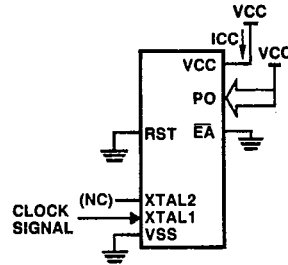


Figure 2 ICC Test Condition, Idle Mode.
All other pins are disconnected.

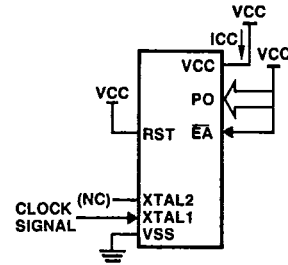


Figure 3 : ICC Test Condition, Active Mode.
All other pins are disconnected.

4



5868455 MATRA DESIGN SEMICOND
80C51/80C31

94D 00628 D

T-49-19-08

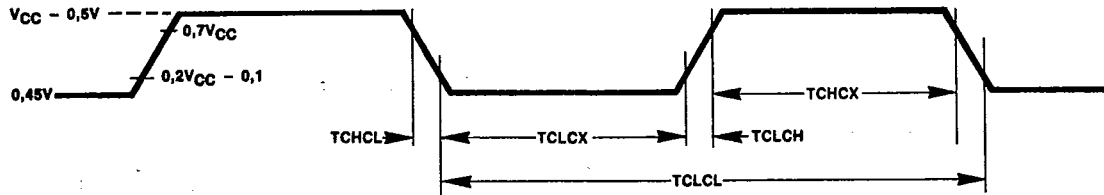


Figure 4 : Clock Signal Waveform for ICC Tests In Active and Idle Modes. TCLCH = TCHCL = 5 ns.

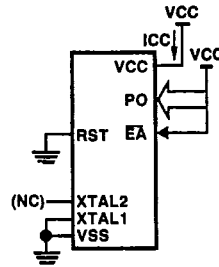


Figure 5 : ICC Test Condition, Power Down Mode. All other pins are disconnected.

Note 2 :

ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 5V, VIH = VCC - 5V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC
ICC would be slightly higher if a crystal oscillator used.

Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 5V, VIH = VCC - 5V ; XTAL2 N.C. ; Port 0 = VCC ; EA = RST = VSS.

Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 3 : Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45V with maxi VOL peak 0.6V. A Schmitt Trigger use is not necessary.

EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL 1)

Symbol	Parameter	Variable clock freq = to 12 MHz		Unit
		Min	Max	
1/TCLCL	Oscillator Frequency		12 (80C51-1) 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



5868455 MATRA DESIGN SEMICOND

94D 00629 D

80C51/80C31

7-49-19-08

A.C. PARAMETERS :

TA = 0°C + 70°C ; VSS = 0V ; VCC = 5V ± 20 % (commercial)

TA = - 40°C + 85°C ; VSS = 0V ; VCC = 5V ± 20 % (industrial)

(Load Capacitance for Port 0, ALE, and $\overline{\text{PSEN}}$ = 100 pf ; Load Capacitance for All Other Outputs = 80 pf).**EXTERNAL PROGRAM MEMORY CHARACTERISTICS**

Symbol	Parameter (notes 4 and 5)	Min	Max	Units
TLHLL	ALE Pulse Width	2TCLCL-40		ns
TAVLL	Address Valid to ALE	TCLCL-55		ns
TLLAX	Address Hold After ALE	TCLCL-35		ns
TLLIV	ALE to Valid Instr in		4TCLCL-100	ns
TLLPL	ALE to $\overline{\text{PSEN}}$	TCLCL-40		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	3TCLCL-45		ns
TPLIV	$\overline{\text{PSEN}}$ to Valid Instr in		3TCLCL-105	ns
TPXIX	Input Instr Hold After $\overline{\text{PSEN}}$	0		ns
TPXIZ	Input Instr Float After $\overline{\text{PSEN}}$		TCLCL-25	ns
TPXAV	$\overline{\text{PSEN}}$ to Address Valid	TCLCL-8		ns
TAVIV	Address to Valid Instr in		5TCLCL-105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10	ns

4

EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter (notes 4 and 5)	Min	Max	Units
TRLRH	$\overline{\text{RD}}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	6TCLCL-100		ns
TLLAX	Data Address Hold After ALE	TCLCL-35		ns
TRLDV	$\overline{\text{RD}}$ to Valid Data in		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		2TCLCL-70	ns
TLLDV	ALE to Valid Data in		8TCLCL-150	ns
TAVDV	Address to Valid Data in		9TCLCL-165	ns
TLLWL	ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	3TCLCL-50	3TCLCL + 50	ns
TAVWL	Address to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	4TCLCL-130		ns
TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	TCLCL-60		ns
TQVWH	Data Setup to $\overline{\text{WR}}$ High	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{\text{WR}}$	TCLCL-50		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	TCLCL-40	TCLCL + 40	ns



5868455 MATRA DESIGN SEMICONDUCTOR
80C51/80C31

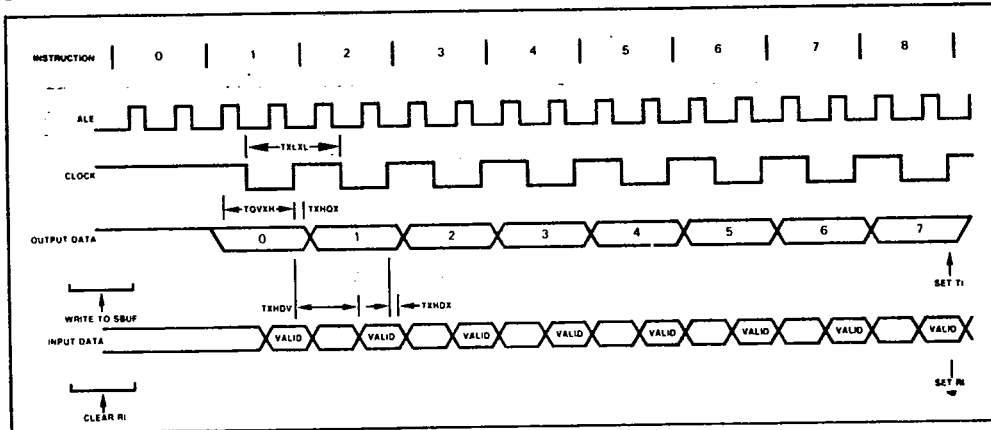
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T-49-19-08

SERIAL PORT TIMING — SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
TXLXL	Serial Port Clock Cycle Time	12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL—133		ns
TXHQX	Output Data Hold After Clock Rising Edge	2TCLCL—117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		10TCLCL—133	ns

SHIFT REGISTER TIMING WAVEFORMS



EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list all the characters and what they stand for.

- A : Address.
- C : Clock.
- D : Input data.
- H : Logic level HIGH.
- I : Instruction (program memory contents).
- L : Logic level LOW, or ALE.

- P : PSEN.
- Q : Output data.
- R : READ signal.
- T : Time.
- V : Valid.
- W : WRITE signal.
- X : No longer a valid logic level.
- Z : Float.

EXAMPLE :

TAVLL = Time for Address Valid to ALE low.
TLLPL = Time for ALE low to PSEN low.



T-49-19-08

ABSOLUTE MAXIMUM RATINGS*

Ambiant Temperature Under Bias . . . - 55°C to +125°C
Storage Temperature - 65°C to +150°C
Voltage on Any Pin to VSS -0.5 V to VCC + 0.5 V
Voltage on VCC to VSS -0.5 V to 6.5 V
Power Dissipation 200 mW

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC CHARACTERISTICS

TA = - 55°C to + 125°C ; VSS = 0V
VCC = 5V ± 10 %

Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage (Except EA)	- 0.5	0.2 VCC - 25	V	
VIL1	Input Low Voltage (EA)	- 0.5	0.2 VCC - 45	V	
VIH	Input High Voltage (Except XTAL1, RST)	0.2VCC+1.1	VCC+0.5	V	
VIH1	Input High Voltage (XTAL1, RST)	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6 mA (note 3)
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	IOL = 3.2 mA
VOH	Output High Voltage (Ports 1, 2, 3)	2.4		V	IOH = - 60µA VCC = 5V ± 10%
		0.75 VCC		V	IOH = - 25 µA
		0.9 VCC		V	IOH = - 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, PEN)	2.4		V	IOH = - 400 µA VCC = 5V ± 10%
		0.75 VCC		V	IOH = - 150 µA
		0.9VCC		V	IOH = 40 µA (Note 2)
IIL	Logical 0 Input Current Ports 1, 2, 3		- 75	µA	Vin = 0.45V
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		- 750	µA	Vin = 2 V
ILI	Input Leakage Current (Port 0, EA)		± 10	µA	0.45 < Vin < VCC
RRST	Reset Pulldown Resistor	50	150	KOhm	
CIO	Pin Capacitance		10	pF	Test Freq = 1 MHz, TA = 25°C
IPD	Power Down Current		75	µA	VCC = 2 to 6 V
ICC	Power supply current Active mode 12 MHz Idle mode 12 MHz		21	mA	VCC = 5.5V
			7	mA	VCC = 5.5V



5868455 MATRA DESIGN SEMICOND
M 80C51/M 80C31

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T-49-19-08

A.C. PARAMETERS :

TA = 0°C + 70°C ; VSS = 0V

TA = 5V ± 10 %

(See Note 2 - Load Capacitance for Port 0, ALE, and PSEN = 100 pf ; Load Capacitance for All Other Outputs = 80 pf).

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

FREQ = 12 MHz (MAX)

Symbol	Parameter	Min	Max	Units
TLHLL	ALE Pulse Width	2TCLCL-55		ns
TAVLL	Address Valid to ALE	TCLCL-70		ns
TLLAX	Address Hold After ALE	TCLCL-50		ns
TLLIV	ALE to Valid Instr in		4TCLCL-115	ns
TLLPL	ALE to PSEN	TCLCL-55		ns
TPLPH	PSEN Pulse Width	3TCLCL-60		ns
TPLIV	PSEN to Valid Instr in		3TCLCL-120	ns
TPXIX	Input Instr Hold After PSEN	0		ns
TPXIZ	Input Instr Float After PSEN		TCLCL-40	ns
TPXAV	PSEN to Address Valid	TCLCL-8		ns
TAVIV	Address to Valid Instr in		5TCLCL-120	ns
TPLAZ	PSEN Low to Address Float		25	ns

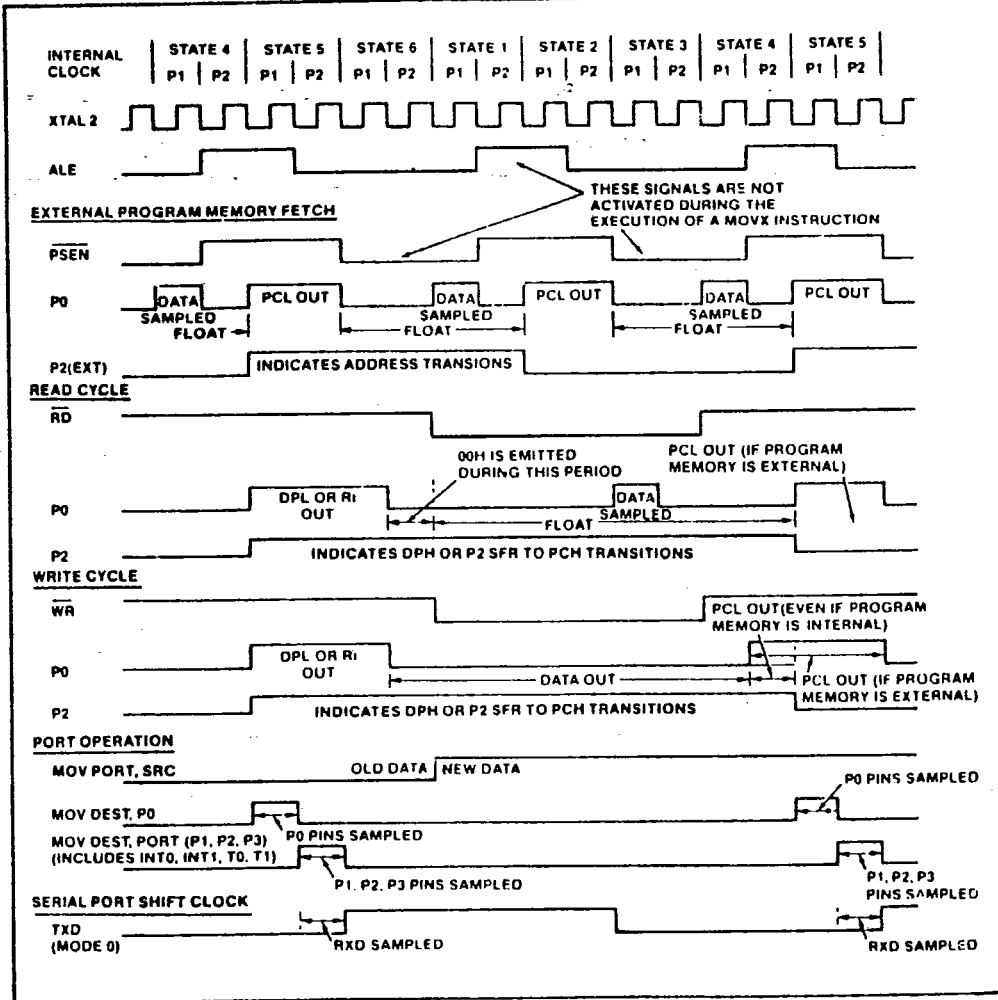
EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
TRLRH	RD Pulse Width	6TCLCL-100		ns
TWLWH	WR Pulse Width	6TCLCL-100		ns
TLLAX	Data Address Hold After ALE	TCLCL-35		ns
TRLDV	RD to Valid Data in		5TCLCL-185	ns
TRHDX	Data Hold After RD	0		ns
TRHDZ	Data Float After RD		2TCLCL-85	ns
TLLDV	ALE to Valid in		8TCLCL-170	ns
TAVDV	Address to Valid Data in		9TCLCL-185	ns
TLLWL	ALE to WR or RD	3TCLCL-65	3TCLCL + 65	ns
TAVWL	Address to WR or RD	4TCLCL-145		ns
TQVWX	Data Valid to WR Transition	TCLCL-75	ns	
TQVWH	Data Setup to WR High	7TCLCL-150		ns
TWHQX	Data Hold After WR	TCLCL-65		ns
TRLAZ	RD Low to Address Float		0	ns
TWHLH	RD or WR High to ALE High	TCLCL-65	TCLCL + 65	ns



T-49-19-08

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though ($T_A = 25^\circ\text{C}$, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.



80C51/80C31

T-49-19-08

Table 1. MCS[®]-51 Instruction Set Description

ARITHMETIC OPERATIONS			
Mnemonic		Description	Byte Cyc
ADD	A,Rn	Add register to Accumulator	1 1
ADD	A,direct	Add direct byte to Accumulator	2 1
ADD	A,@Ri	Add indirect RAM to Accumulator	1 1
ADD	A,#data	Add immediate data to Accumulator	2 1
ADDC	A,Rn	Add register to Accumulator with Carry	1 1
ADDC	A,direct	Add direct byte to A with Carry flag	2 1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1 1
ADDC	A,#data	Add immediate data to A with Carry flag	2 1
SUBB	A,Rn	Subtract register from A with Borrow	1 1
SUBB	A,direct	Subtract direct byte from A with Borrow	2 1
SUBB	A,@Ri	Subtract indirect RAM from A with Borrow	1 1
SUBB	A,#data	Subtract immed data from A with Borrow	2 1
INC	A	Increment Accumulator	1 1
INC	Rn	Increment register	1 1
INC	direct	Increment direct byte	2 1
INC	@Ri	Increment indirect RAM	1 1
INC	DPTR	Increment Data Pointer	1 2
DEC	A	Decrement Accumulator	1 1
DEC	Rn	Decrement register	1 1
DEC	direct	Decrement direct byte	2 1
DEC	@Ri	Decrement indirect RAM	1 1
MUL	AB	Multiply A & B	1 4
DIV	AB	Divide A by B	1 4
DA	A	Decimal Adjust Accumulator	1 1
LOGICAL OPERATIONS			
Mnemonic		Destination	Byte Cyc
ANL	A,Rn	AND register to Accumulator	1 1
ANL	A,direct	AND direct byte to Accumulator	2 1
ANL	A,@Ri	AND indirect RAM to Accumulator	1 1
ANL	A,#data	AND immediate data to Accumulator	2 1
ANL	direct,A	AND Accumulator to direct byte	2 1
ANL	direct,#data	AND immediate data to direct byte	3 2
ORL	A,Rn	OR register to Accumulator	1 1
ORL	A,direct	OR direct byte to Accumulator	2 1

LOGICAL OPERATIONS (CONTINUED)			
Mnemonic		Destination	Byte Cyc
ORL	A,@Ri	OR indirect RAM to Accumulator	1 1
ORL	A,#data	OR immediate data to Accumulator	2 1
ORL	direct,A	OR Accumulator to direct byte	2 1
ORL	direct,#data	OR immediate data to direct byte	3 2
XRL	A,Rn	Exclusive-OR register to Accumulator	1 1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2 1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1 1
XRL	A,#data	Exclusive-OR immediate data to A	2 1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2 1
XRL	direct,#data	Exclusive-OR immediate data to direct	3 2
CLR	A	Clear Accumulator	1 1
CPL	A	Complement Accumulator	1 1
RL	A	Rotate Accumulator Left	1 1
RLC	A	Rotate A Left through the Carry flag	1 1
RR	A	Rotate Accumulator Right	1 1
RRC	A	Rotate A Right through Carry flag	1 1
SWAP	A	Swap nibbles within the Accumulator	1 1
DATA TRANSFER			
Mnemonic		Description	Byte Cyc
MOV	A,Rn	Move register to Accumulator	1 1
MOV	A,direct	Move direct byte to Accumulator	2 1
MOV	A,@Ri	Move indirect RAM to Accumulator	1 1
MOV	A,#data	Mov immediate data to Accumulator	2 1
MOV	Rn,A	Move Accumulator to register	1 1
MOV	Rn,direct	Move direct byte to register	2 2
MOV	Rn,#data	Move immediate data to register	2 1
MOV	direct,A	Move Accumulator to direct byte	2 1
MOV	direct,Rn	Move register to direct byte	2 2
MOV	direct,direct	Move direct byte to direct	3 2
MOV	direct,@Ri	Move indirect RAM to direct byte	2 2



80C51/80C31
Table 1. (Cont.)

T-49-19-04

DATA TRANSFER (CONTINUED)			PROGRAM AND MACHINE CONTROL		
Mnemonic	Description	Byte Cyc	Mnemonic	Description	Byte Cyc
MOV	direct,#data	3 2	ACALL	addr11	2 2
MOV	@Ri,A	1 1	LCALL	addr16	3 2
MOV	@Ri,direct	2 2	RET		1 2
MOV	@Ri,#data	2 1	RETI		1 2
MOV	DPTR,#data16	3 2	AJMP	addr11	2 2
MOVC	A,@A+DPTR	1 2	LJMP	addr16	3 2
MOVC	A,@A+PC	1 2	SJMP	rel	2 2
MOVX	A,@Ri	1 2	JMP	@A+DPTR	1 2
MOVX	A,@DPTR	1 2	JZ	rel	2 2
MOVX	@Ri,A	1 2	JNZ	rel	2 2
MOVX	@DPTR,A	1 2	JC	rel	2 2
PUSH	direct	2 2	JNC	rel	2 2
POP	direct	2 2	JB	bit,rel	3 2
XCH	A,Rn	1 1	JNB	bit,rel	3 2
XCH	A,direct	2 1	JBC	bit,rel	3 2
XCH	A,@Ri	1 1	CJNE	A,direct,rel	3 2
XCHD	A,@Ri	1 1	CJNE	A,#data,rel	3 2
			CJNE	Rn,#data,rel	3 2
			CJNE	@Ri,#data,rel	3 2
			DJNZ	Rn,rel	2 2
			DJNZ	direct,rel	3 2
			NOP		1 1
			Notes on data addressing modes:		
			Rn	—Working register R0-R7	
			direct	—128 internal RAM locations, any I/O port, control or status register	
			@Ri	—Indirect internal RAM location addressed by register R0 or R1	
			#data	—8-bit constant included in instruction	
			#data16	—16-bit constant included as bytes 2 & 3 of instruction	
			bit	—128 software flags, any I/O pin, control or status bit	
			Notes on program addressing modes:		
			addr16	—Destination address for LCALL & LJMP may be anywhere within the 64-K program memory address space	
			Addr11	—Destination address for ACALL & AJMP will be within the same 2-K page of program memory as the first byte of the following instruction	
			rel	—SJMP and all conditional jumps include an 8-bit offset byte. Range is +127-128 bytes relative to first byte of the following instruction	
			All mnemonics copyrighted © Intel Corporation 1979		
BOOLEAN VARIABLE MANIPULATION					
Mnemonic	Description	Byte Cyc			
CLR	C	1 1			
CLR	bit	2 1			
SETB	C	1 1			
SETB	bit	2 1			
CPL	C	1 1			
CPL	bit	2 1			
ANL	C,bit	2 2			
ANL	C,1 bit	2 2			
ORL	C/bit	2 2			
ORL	C,1 bit	2 2			
MOV	C/bit	2 1			
MOV	bit,C	2 2			

4



80C51/80C31

T-49-19-08

Table 2. Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP		33	1	RLC	A
01	2	AJMP	code addr	34	2	ADDC	A,#data
02	3	LJMP	code addr	35	2	ADDC	A,data addr
03	1	RR	A	36	1	ADDC	A,@R0
04	1	INC	A	37	1	ADDC	A,@R1
05	2	INC	data addr	38	1	ADDC	A,R0
06	1	INC	@R0	39	1	ADDC	A,R1
07	1	INC	@R1	3A	1	ADDC	A,R2
08	1	INC	R0	3B	1	ADDC	A,R3
09	1	INC	R1	3C	1	ADDC	A,R4
0A	1	INC	R2	3D	1	ADDC	A,R5
0B	1	INC	R3	3E	1	ADDC	A,R6
0C	1	INC	R4	3F	1	ADDC	A,R7
0D	1	INC	R5	40	2	JC	code addr
0E	1	INC	R6	41	2	AJMP	code addr
0F	1	INC	R7	42	2	ORL	data addr,A
10	3	JBC	bit addr, code addr	43	3	ORL	data addr,#data
11	2	ACALL	code addr	44	2	ORL	A,#data
12	3	LCALL	code addr	45	2	ORL	A,data addr
13	1	RRC	A	46	1	ORL	A,@R0
14	1	DEC	A	47	1	ORL	A,@R1
15	2	DEC	data addr	48	1	ORL	A,R0
16	1	DEC	@R0	49	1	ORL	A,R1
17	1	DEC	@R1	4A	1	ORL	A,R2
18	1	DEC	R0	4B	1	ORL	A,R3
19	1	DEC	R1	4C	1	ORL	A,R4
1A	1	DEC	R2	4D	1	ORL	A,R5
1B	1	DEC	R3	4E	1	ORL	A,R6
1C	1	DEC	R4	4F	1	ORL	A,R7
1D	1	DEC	R5	50	2	JNC	code addr
1E	1	DEC	R6	51	2	ACALL	code addr
1F	1	DEC	R7	52	2	ANL	data addr,A
20	3	JB	bit addr, code addr	53	3	ANL	data addr,#data
21	2	AJMP	code addr	54	2	ANL	A,#data
22	1	RET		55	2	ANL	A,data addr
23	1	RL	A	56	1	ANL	A,@R0
24	2	ADD	A,#data	57	1	ANL	A,@R1
25	2	ADD	A,data addr	58	1	ANL	A,R0
26	1	ADD	A,@R0	59	1	ANL	A,R1
27	1	ADD	A,@R1	5A	1	ANL	A,R2
28	1	ADD	A,R0	5B	1	ANL	A,R3
29	1	ADD	A,R1	5C	1	ANL	A,R4
2A	1	ADD	A,R2	5D	1	ANL	A,R5
2B	1	ADD	A,R3	5E	1	ANL	A,R6
2C	1	ADD	A,R4	5F	1	ANL	A,R7
2D	1	ADD	A,R5	60	2	JZ	code addr
2E	1	ADD	A,R6	61	2	AJMP	code addr
2F	1	ADD	A,R7	62	2	XRL	data addr A
30	3	JNB	bit addr, code addr	63	3	XRL	data addr,#data
31	2	ACALL	code addr	64	2	XRL	A,#data
32	1	RETI		65	2	XRL	A,data addr

4



80C51/80C31

Table 2, (Cont.)

T-49-19-08

4

Hex Code	Number of Bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	data addr, data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0

Hex Code	Number of Bytes	Mnemonic	Operands
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3



80C51/80C31
Table 2. (Cont.)

T-49-19-08

Hex Code	Number of Bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr

Hex Code	Number of Bytes	Mnemonic	Operands
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

4

Ordering Information

