

8251/Am9551

Programmable Communication Interface

iAPX86 Family

MILITARY INFORMATION

8251/Am9551

DISTINCTIVE CHARACTERISTICS

- Separate control and transmit register input buffers
- Synchronous or asynchronous serial data transfer
- Parity, overrun, and framing errors detected
- Half- or full-duplex signaling
- Character length of 5, 6, 7, or 8 bits
- Internal or external synchronization
- Odd parity, even parity, or no parity bit
- Modem interface controlled by processor
 - Programmable Sync pattern
 - Fully TTL-compatible logic levels

GENERAL DESCRIPTION

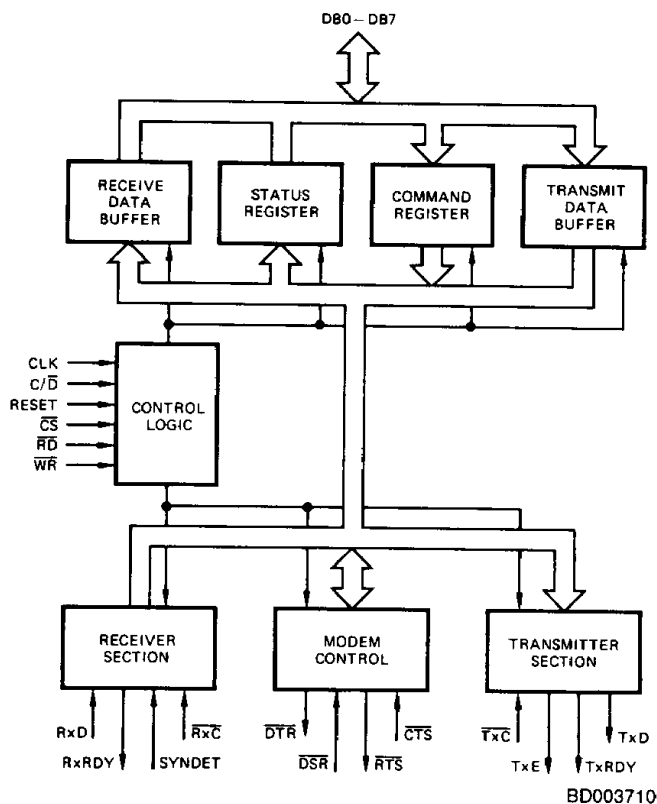
The 8251/Am9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream.

Simultaneously, serial data can be received, converted into parallel form, deformatted, and then presented to the CPU. The USART can operate in an independent full-duplex mode.

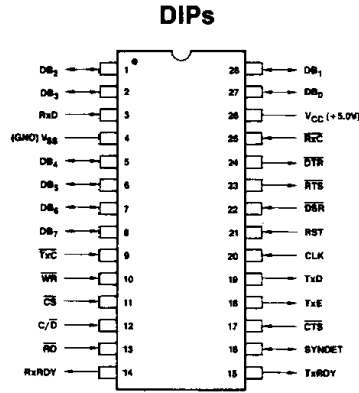
Data, control, operation, and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the 8251/Am9551 to service a wide range of communication disciplines and applications.

BLOCK DIAGRAM



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Amendment /0
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CONNECTION DIAGRAM Top View



CD005482

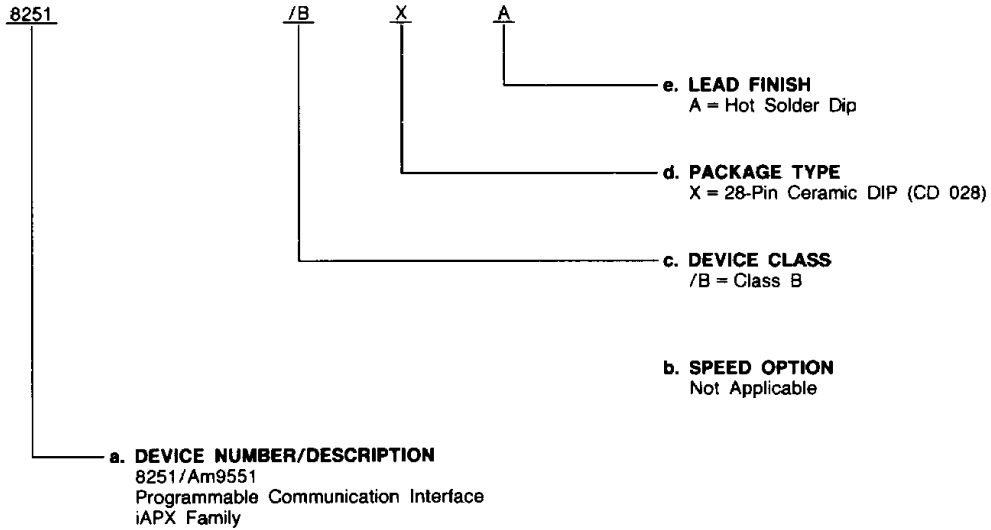
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations

Valid Combinations	
8251	/BXA
AM9551	

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 VCC with Respect to VSS -0.5 to +7.0 V
 All Signal Voltages
 with Respect to VSS -0.5 V to +7.0 V
 Power Dissipation 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
 Temperature (T_C) -55 to +125°C
 Supply Voltage (VCC) 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	8251		Am9551		Unit
			Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	I _{OH} = -200 μA, V _{CC} = 4.5 V	2.4				V
		I _{OH} = -100 μA	2.4				
VOL	Output LOW Voltage	I _{OL} = 1.6 mA, V _{CC} = 4.5 V	0.45		0.45		V
V _{IH}	Input HIGH Voltage	V _{CC} = 5 V ± 10%	2.2	V _{CC} *	2.2	V _{CC} *	V
V _{IL}	Input LOW Voltage	V _{CC} = 5 V ± 10%	-0.5*	0.8	-0.5*	0.8	V
I _{LI}	Input Load Current	V _{CC} = 5.5 V, V _I = 1.5 V, V _O = 0 V		±10		±10	μA
I _{DL}	Data Bus Leakage Current	V _{DD} = 0 V, V _{CC} = 5.5 V		-50		-50	μA
		V _{DD} = 5.5 V, V _{CC} = 5.5 V		10		10	
I _{CC}	V _{CC} Supply Current		120		120		mA
C _O †	Output Capacitance	f _c = 1.0 MHz, Inputs = 0 V		15*		15*	pF
C _I †	Input Capacitance			10*		10*	pF
C _{I/O} †	I/O Capacitance			20*		20*	pF

* Guaranteed by design; not tested.
 † Not included in Group A tests.

Notes: 1. I_{CC} is measured in a static condition with outputs in the worst-case condition with all outputs unloaded.

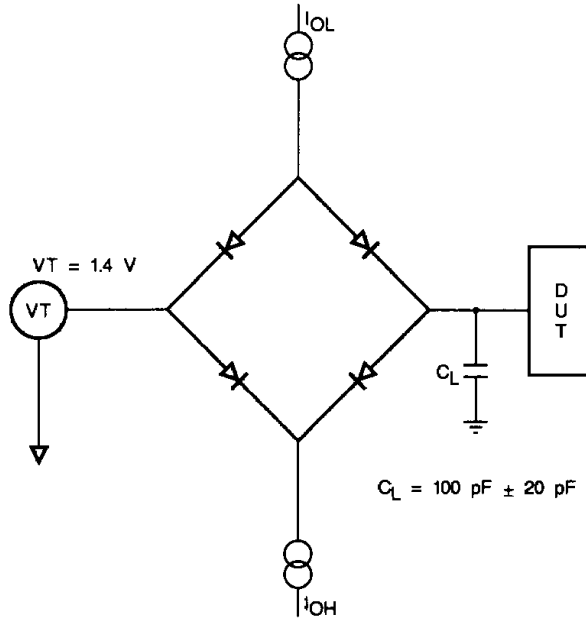
SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF006490

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING TEST CIRCUIT



TC003851

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 4)

Parameter Symbol	Parameter Description	8251		Am9551		Unit	
		Min.	Max.	Min.	Max.		
tAR	\overline{CS} , C/D Stable to \overline{READ} LOW Setup Time	50		50		ns	
tAW	\overline{CS} , C/D Stable to \overline{WRITE} LOW Setup Time	20		20		ns	
tCR	\overline{DSR} , \overline{CTS} to \overline{READ} LOW Setup Time		16		16	tCY	
tCY	Clock Period	0.420	1.35	0.380	1.35	μ s	
tDF	\overline{READ} HIGH to Data Bus Off Delay	25	200	25	200	ns	
tDTx	TxC LOW to TxD Delay		1.0		1.0	μ s	
tDW	Data to \overline{WRITE} HIGH Setup Time	200		150		ns	
tES	External SYNDET to RxC LOW Setup Time	16		16		tCY	
tHRx	Sampling Pulse to Rx Data Hold Time (Note 5)	2.0		2.0		μ s	
tIS	Data Bit (Center) to Internal SYNDET Delay		30		30	tCY	
tPW	Clock Pulse Width	220	0.6tCY	175	0.6tCY	ns	
tRA	\overline{READ} HIGH to \overline{CS} , C/D Hold Time	5.0		5.0		ns	
tRD	\overline{READ} LOW to Data Bus On Delay		350		250	ns	
tRPD	Receiver Clock HIGH Time	1x Baud Rate		15		tCY	
		16x & 64x Baud Rate	3	3			
tRPW	Receiver Clock LOW Time	1x Baud Rate	12	12		tCY	
		16x & 64x Baud Rate	1	1			
tRR	\overline{READ} Pulse Width	430		380		ns	
tRV	Time Between \overline{WRITE} Pulses During Initialization (Note 1)	6.0		6.0		tCY	
tRx	Data Bit (Center) to RxRDY Delay		20		20	tCY	
tSRx	Rx Data to Sampling Pulse Setup Time (Note 5)	2.0		2.0		μ s	
tTPD	Transmitter Clock HIGH Time	1x Baud Rate	15	15		tCY	
		16x & 64x Baud Rate	3	3			
tTPW	Transmitter Clock LOW Time	1x Baud Rate	12	12		tCY	
		16x & 64x Baud Rate	1	1			
tTX	Data Bit (Center) to TxLD Delay		16		16	tCY	
tTxE	Data Bit (Center) to TxEMPTY Delay		16		16	tCY	
tWA	\overline{WRITE} HIGH to \overline{CS} , C/D Hold Time	20		20		ns	
tWC	\overline{WRITE} HIGH to TxE, DTR, RTS Delay		16		16	tCY	
tWD	\overline{WRITE} HIGH to Data Hold Time	40		40		ns	
tWW	\overline{WRITE} Pulse Width	430		380		ns	
fRx	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	
fTx	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	

- Notes: 1. This time period between write pulses is specified for initialization purposes only when MODE, SYNC 1, SYNC 2, COMMAND, and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1. tRV after internal Reset = 8 * tCY.
 2. Reset Pulse Width = 6tCY Min.
 3. Switching Characteristics parameters are listed in alphabetical order.
 4. Clock Rise and Fall times are controlled by the Teradyne J941 tester. Measurement of typical signals generated by the J941 showed tR = tF = 5 ns.
 5. Sampling pulse is internal and not tested; guaranteed by design.