DOCUMENT NUMBER AND REVISION

VL-FS-MDLS16166D-30 REV. A

(MDLS16166-HV-B-LED04)

DOCUMENT TITLE:

SPECIFICATION
OF
LCD MODULE TYPE
MODEL NUMBER: MDLS16166D-30

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2005.04.11	First Release Based on a.) Test Specification: VL-TS-MDLS16166D-XX, REV. O, 2005.03.31). b.) VL-QUA-012B REV.W 2004.03.20 According to VL-PUA-012B, LCD size is small because Unit Per Laminate=32 which is more than 6 pcs/Laminate.	ZHANG XIAO LAN	FRANK WANG

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VARITRONIX LIMITED

Specification
of
LCD Module Type
Model No.: MDLS16166D-30

1. General Description

- 16 characters (5 x 8 dots) x 1 line STN Negative Blue Transmisstive LCD Character Module.
- Viewing Angle: 6 O'clock direction.
- Driving scheme: 1/16 Duty, 1/4 bias.
- 'NOVATEK' NT3881DH-01/AI (die form) LCD Controller and Driver or equivalent.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	80.0(W) x 36.0(H) x 14.0 MAX.(D)	mm
Viewing area	64.5(W) x 13.8(H)	mm
Display format	16 characters x 1 line	-
Character size	3.15(W) x 6.30(H) (5 x 8 dots)	mm
Character spacing	0.60(W)	mm
Character pitch	3.75(W)	mm
Dot size	0.55(W) x 0.70(H)	mm
Dot spacing	0.10(W) x 0.10(H)	mm
Dot pitch	0.65(W) x 0.80(H)	mm
Weight:	Approx:35	grams

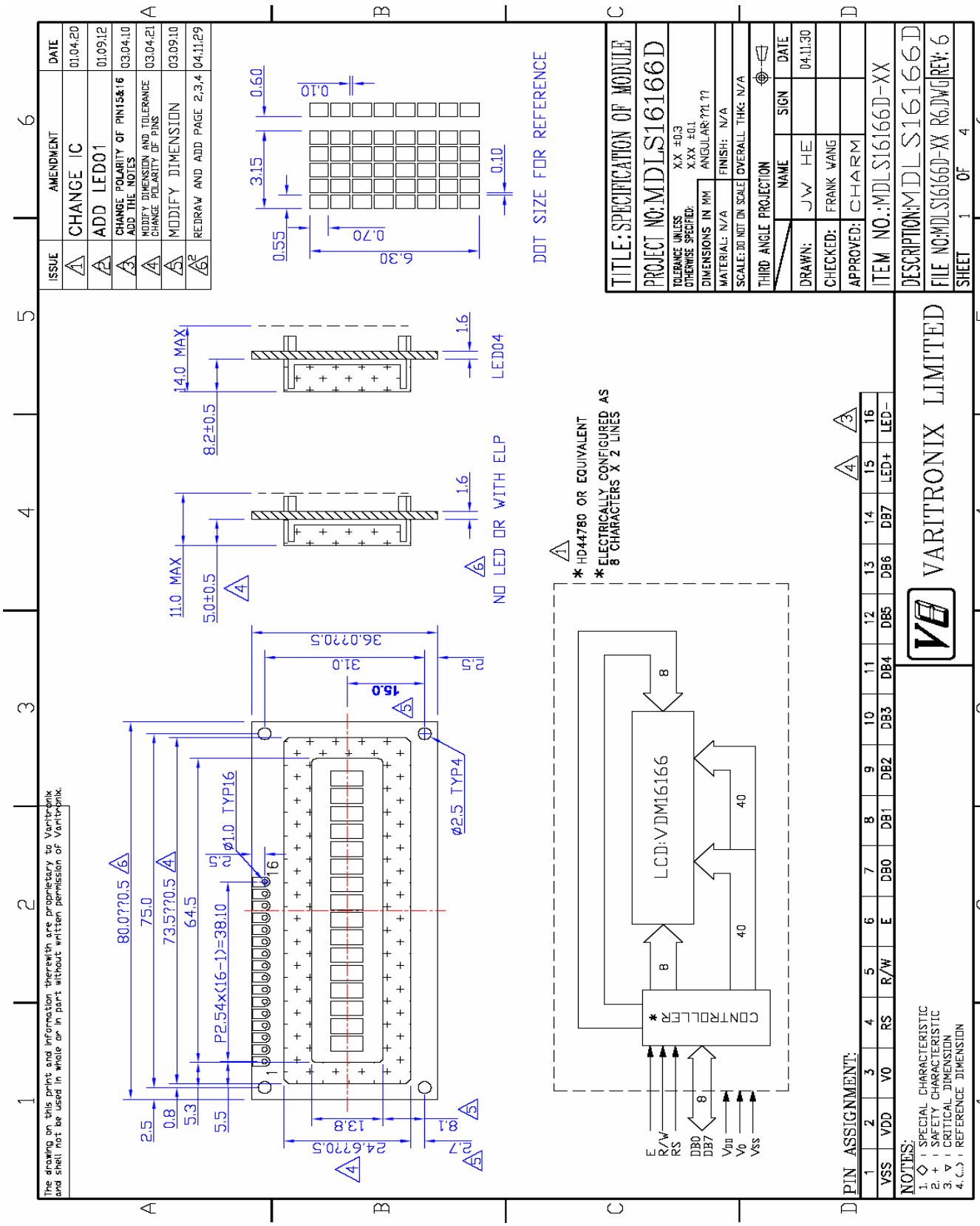

Figure 1: Module Specification

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: "High" for Data register (for read and write) "Low" for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: "High" for Read mode. "Low" for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15	LED(+)	Anode of LED backlight
16	LED(-)	Cathode of LED backlight

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings –For IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD – VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+13.5	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-10°C	+60°C	-20°C	+70°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.85	5.00	5.15	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD =5.0V, Note1.	6.7	7.1	7.5	V
Input signal voltage for E,DB0-DB7,R/W,RS.	V_{IH}	"H" level	2.2	-	VDD	V
	V_{IL}	"L" level	-0.3	-	0.8	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.3	2.0	mA
		Checker board mode, Note 1	-	2.1	3.1	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.8	1.2	mA
		Checker board mode, Note 1	-	0.8	1.2	mA
Supply voltage of yellow-green LED04 backlight	VLED	Forward current =100mA Number of LED dies=2x10=20	3.85	4.05	4.25	V
Peak wave length of yellow-green LED04 backlight	λ		-	568	-	nm
Luminance of yellow-green LED04 backlight			145	193	242	Cd/m2

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta = -10 °C To +60 °C , VDD = +5V±5%, VSS = 0V.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	t_{CYCE}	500	-	ns	
Enable ”High” level pulse width	t_{WHE}	300	-	ns	
Enable rise time	t_{RE}	-	25	ns	
Enable fall time	t_{FE}	-	25	ns	
RS, R/W set-up time	t_{AS}	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	t_{AH}	10	-	ns	
Data output delay	t_{DS}	100	-	ns	
Data hold time	t_{DHR}	10	-	ns	

Refer to Fig. 3, the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	t_{CYCE}	500	-	ns	
Enable ”High” level pulse width	t_{WHE}	300	-	ns	
Enable rise time	t_{RE}	-	25	ns	
Enable fall time	t_{FE}	-	25	ns	
RS, R/W set-up time	t_{AS}	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	t_{AH}	10	-	ns	
Read data output delay	t_{RD}	-	190	ns	
Read data hold time	t_{DHR}	20	-	ns	

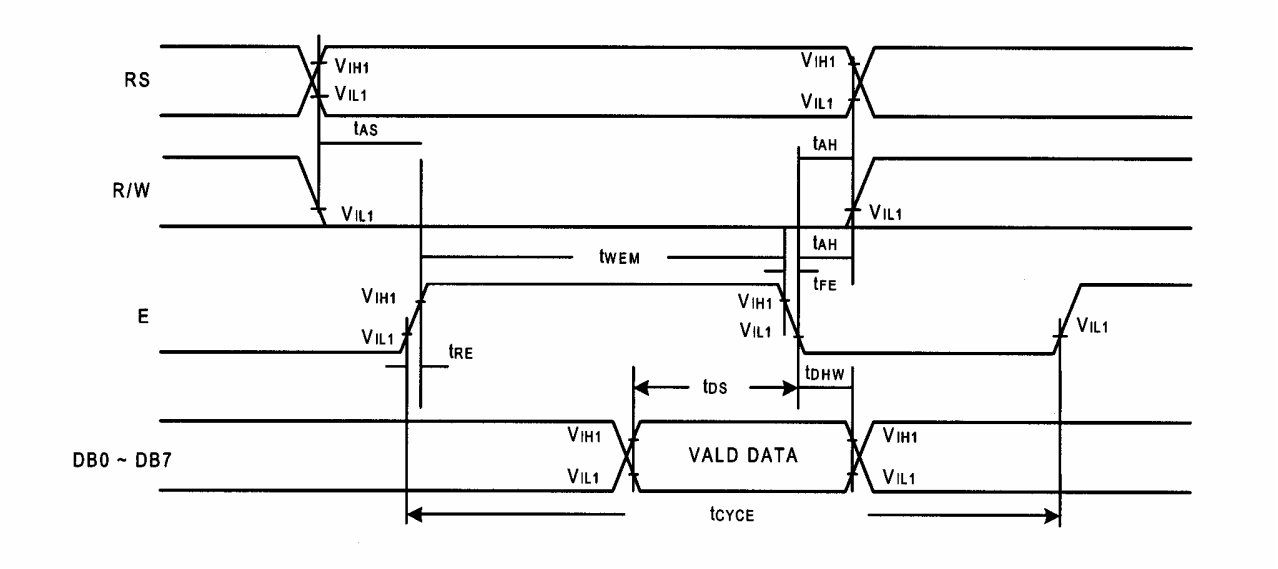

Figure 2: Bus write operation sequence (Writing data from MPU to NT3881D).

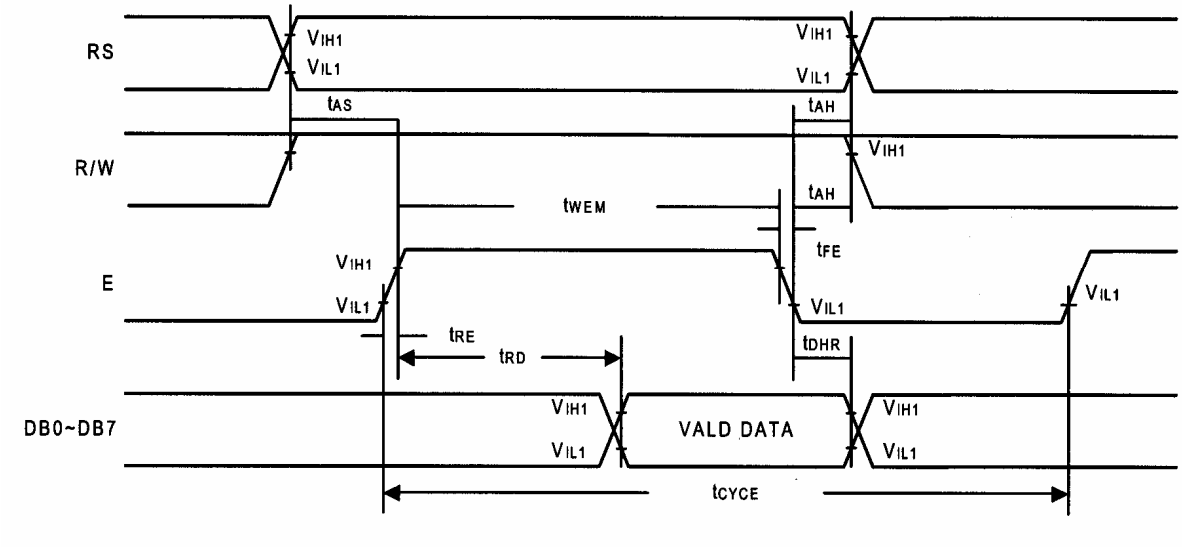

Figure 3: Bus read operation sequence (Reading out data from NT3881D to MPU).

5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

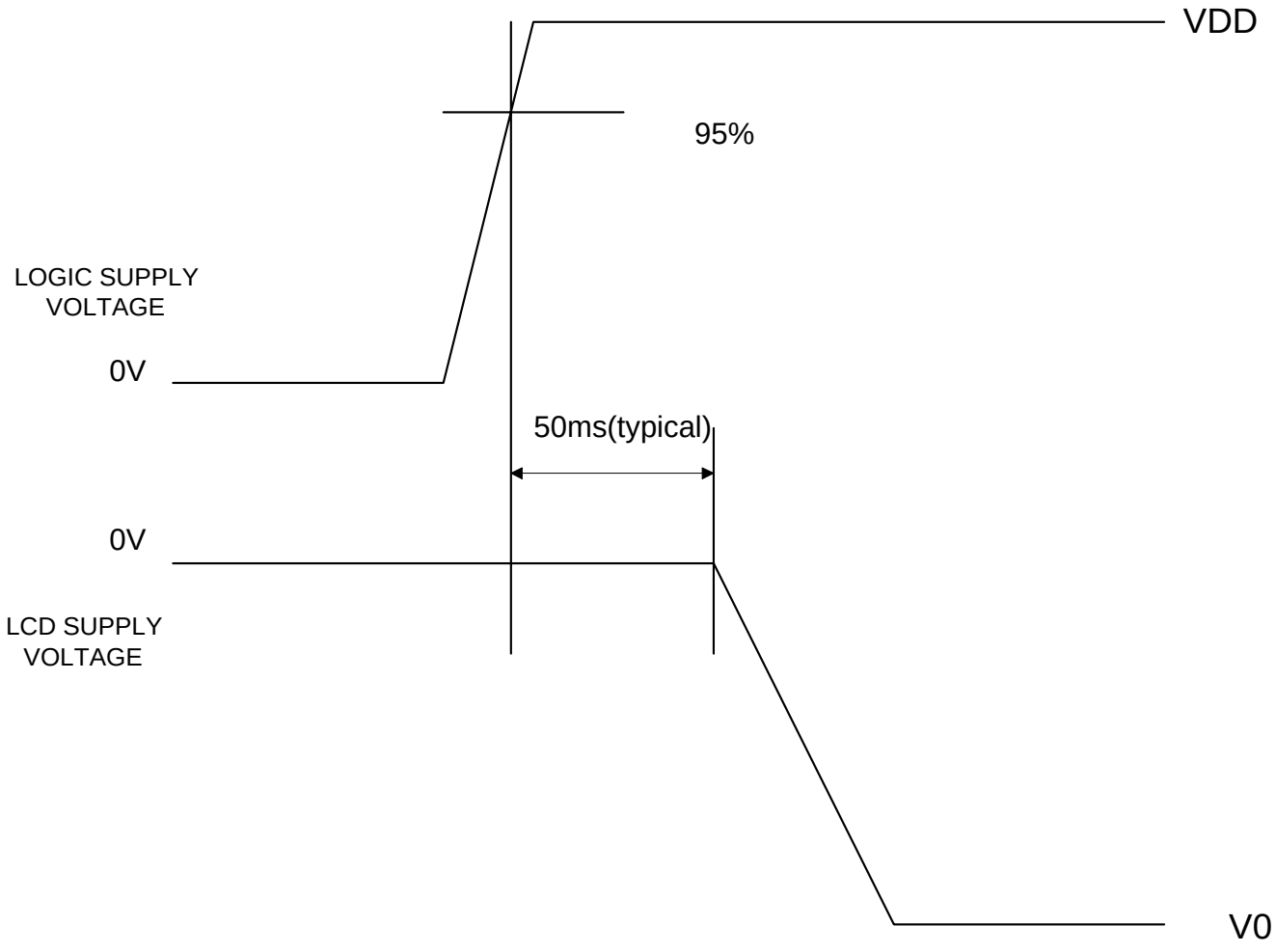

Figure 4: Timing diagram of VDD against V0.

6. Correspondence between Character Codes and Character Patterns (NOVATEK Standard NT3881D-01)

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

7. Instruction Set

Instruction	Code										Function	Execution time (max) (f_{osc} = 250KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DD RAM address 00H.	1.64ms
Display/ Cursor Home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00H.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify direction of cursor movement and display shift mode. This operation takes place after each data transfer (read/write).	40μs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D) cursor (C) and blinking of character at cursor position (B).	40μs
Display/ Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL), number of display line (N), and character font (F).	40μs
RAM Address Set	0	0	0	1	ACG						Load the address counter with a CG RAM address. Subsequent data access is for CG RAM data.	40μs
DD RAM Address Set	0	0	1	ADD							Load the address counter with a DD RAM address. Subsequent data access is for DD RAM data.	40μs
Busy Flag/ Address Counter Read	0	1	AC								Read Busy Flag (BF) and contents of Address Counter (AC).	40μs
CG RAM/ DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM.	40μs
CG RAM/ DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM.	40μs
	I/D = 1 : Increment S = 1 : Display Shift On D = 1 : Display On C = 1 : Cursor Display On B = 1 : Cursor Blink On S/C = 1 : Shift Display R/L = 1 : Shift Right DL = 1 : 8-Bit N = 1 : Dual Line F = 1 : 5x10 dots BF = 1 : Internal Operation BF = 1 : Ready for Instruction						I/D = 0 : Decrement S/C = 0 : Move Cursor R/L = 0 : Shift Left DL = 0 : 4-Bit N = 0 : Signal Line F = 0 : 5x8 dots				DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : Character Generator RAM Address ADD : Display Data RAM Address AC : Address Counter	

Note 1: Symbol "*" signifies an insignificant bit (disregard).
Note 2: Correct input value for "N" is predetermined for each model.

8. LCD Cosmetic Conditions

a.) Reference document follow VL-QUA-012B.

b.) LCD size of the product is small.

9. Remark:

a. Identification labels will be stuck on the module without obstructing the viewing area of display,

b. Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display.

"Varitronix Limited reserves the right to change this specification."

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