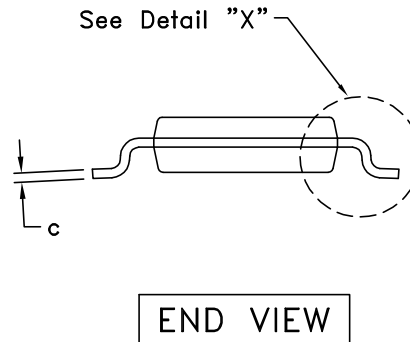
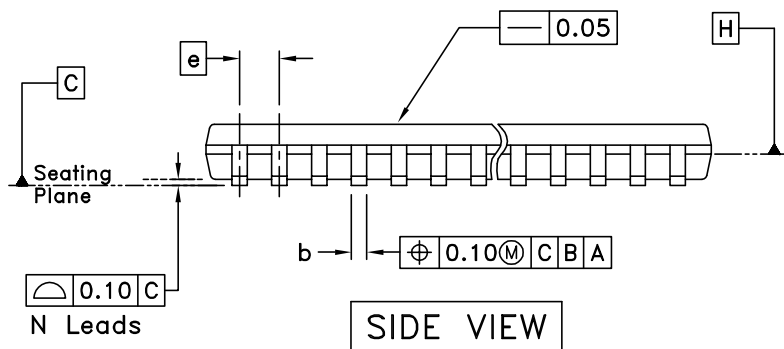


DIMENSION TABLE						
Symbol	14 Lead	16 Lead	20 Lead	24 Lead	28 Lead	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.10	0.10	0.10	0.10	0.10	+/- 0.05
A2	0.90	0.90	0.90	0.90	0.90	+/- 0.05
D	5.00	5.00	6.50	7.80	9.70	+/- 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/- 0.10
L	0.60	0.60	0.60	0.60	0.60	+/- 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
e	0.65	0.65	0.65	0.65	0.65	Basic



Drawing #: MDP0044

Rev: E

Date: 12/11/02

Units: mm

JEDEC Reg: MO-153



PACKAGE OUTLINE DRAWING
TSSOP (Thin-Shrink Small Outline Package) Family

élantec Semiconductor, Inc.
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Notes:

- (1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
- (2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
- (3) Dimensions "D" and "E1" are measured at datum plane H.
- (4) Dimensioning and tolerancing per ASME Y14.5M-1994.