

1. General Description

This ROM-Based 8-bit micro-controller uses a fully static CMOS design technology combines higher speed and smaller size with the low power and high noise immunity of CMOS.

On chip memory system includes 1.0 K bytes of ROM, and 32 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip ROM size : 1,024 words
- ◆ Internal RAM size : 32 bytes
- (25 general purpose registers, 7 special registers)
- ◆ 36 single word instructions
- ◆ 14-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.3V ~ 6.3 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Power edge-detector Reset
- ◆ Sleep Mode for power saving
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ 4 types of oscillator can be selected by programming option:
RC—Low cost RC oscillator

LFXT—Low frequency crystal oscillator

XTAL—Standard crystal oscillator

HFXT—High frequency crystal oscillator

- ◆ 4 oscillator start-up time can be selected by programming option:
150 μ s, 20 ms, 40 ms, 80 ms
- ◆ On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- ◆ Pull up resistors for the following pins :
PA0~PA3, PB0~PB7, /MCLR, RTCC
- ◆ Pull down resistors for the following pins :
PA0~PA3, PB0~PB7, RTCC
- ◆ 12 I/O pins with their own independent direction control

3. Applications

The application areas of this MDT1010 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

PA2	1	18	PA1
PA3	2	17	PA0
RTCC	3	16	OSC1
/MCLR	4	15	OSC2
V _{ss}	5	14	V _{dd}
PB0	6	13	PB7
PB1	7	12	PB6
PB2	8	11	PB5
PB3	9	10	PB4

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5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V _{dd}		Power supply
V _{ss}		Ground

6. Memory Map

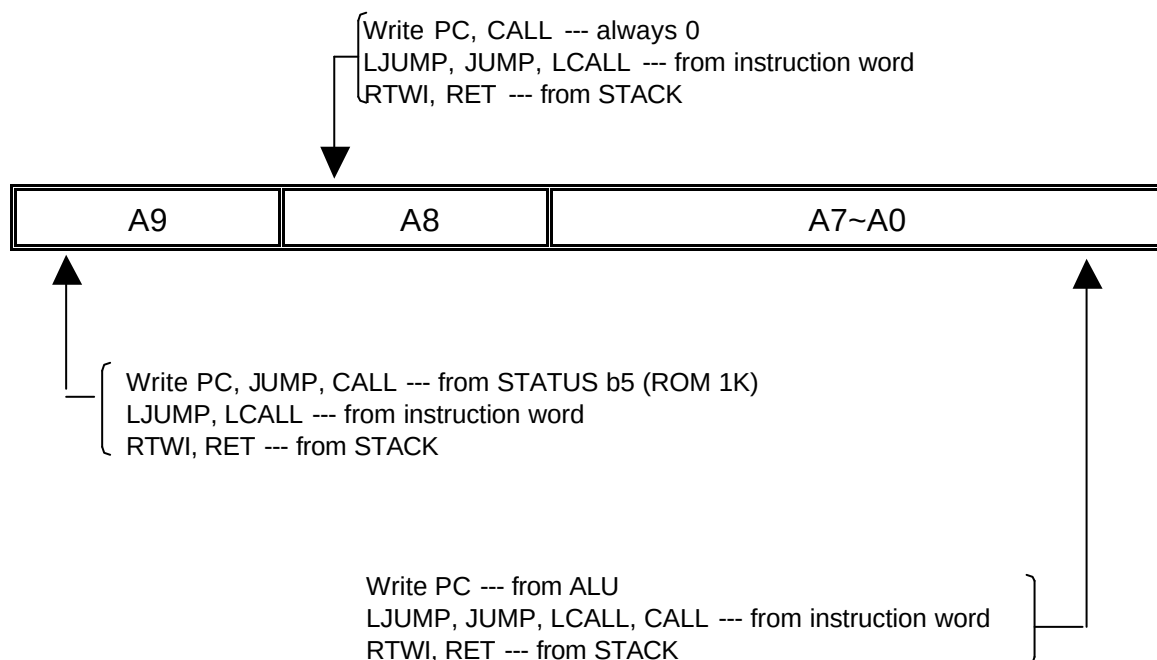
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	Port A
06	Port B
07~1F	Internal RAM, General Purpose Register

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
5	page 0	Page select bit : 0 : 000H --- 1FFH 1 : 200H --- 3FFH
6—7	—	General purpose bit

(5) MSR (Memory Select Register) : R4

(6) PORT A : R5

PA3~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		

(9) CPIO A, CPIO B (Control Port I/O Mode Register)

The CPIO register is "write-only"

= "0", I/O pin in output mode;

= "1", I/O pin in input mode.

(10) Configuration ROM :

Bit 1	Bit 0	Oscillator Type
0	0	RC Oscillator
0	1	LFXT Oscillator
1	0	XTAL Oscillator
1	1	HFXT Oscillator

Bit 3	Bit 2	Oscillator Start-up Time
0	0	150 μ s
0	1	20 ms
1	0	40 ms
1	1	80 ms

Bit 4	Watchdog Timer control
0	Watchdog timer disable all the time
1	Watchdog timer enable all the time

Bit 5	Power Edge-detector
0	Disable
1	Enable

(B) Program Memory

Address	Description
000-3FF	Program memory
3FF	The starting address of the power on, external reset or WDT

7. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset
CPIO A	--	1111 1111	1111 1111
CPIO B	--	1111 1111	1111 1111
TMR	--	--11 1111	--11 1111
IAR	00h	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
MSR	04h	111x xxxx	111u uuuu
PORT A	05h	- - - - xxxx	- - - - uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu

Note : u=unchanged, x=unknown, - =unimplemented, read as “0”

=value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiii	LDWI I	Load immediate to W	I→W	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
010111 trrrrrrr	SWAPR R, t	Swap halves register	$[R(0\sim3) \leftrightarrow R(4\sim7)] \rightarrow t$	None
011001 trrrrrrr	INCR R, t	Increment register	$R + 1 \rightarrow t$	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	$R + 1 \rightarrow t$	None
011011 trrrrrrr	ADDWR R, t	Add W and register	$W + R \rightarrow t$	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	$R - W \rightarrow t$ ($R+W+1 \rightarrow t$)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	$R - 1 \rightarrow t$	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	$R - 1 \rightarrow t$	None
010010 trrrrrrr	ANDWR R, t	AND W and register	$R \cap W \rightarrow t$	Z
110100 iiiiii	ANDWI i	AND W and immediate	$i \cap W \rightarrow W$	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	$R \cup W \rightarrow t$	Z
110101 iiiiii	IORWI i	Inclu. OR W and immediate	$i \cup W \rightarrow W$	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	$R \oplus W \rightarrow t$	Z
110110 iiiiii	XORWI i	Exclu. OR W and immediate	$i \oplus W \rightarrow W$	Z
011111 trrrrrrr	COMR R, t	Complement register	$\neg R \rightarrow t$	Z
010110 trrrrrrr	RRR R, t	Rotate right register	$R(n) \rightarrow R(n-1)$, C $\rightarrow R(7)$, $R(0) \rightarrow C$	C
010101 trrrrrrr	RLR R, t	Rotate left register	$R(n) \rightarrow r(n+1)$, C $\rightarrow R(0)$, $R(7) \rightarrow C$	C
010000 1xxxxxxx	CLRW	Clear working register	$0 \rightarrow W$	Z
010001 0rrrrrrr	CLRR R	Clear register	$0 \rightarrow R$	Z
0000bb brrrrrrr	BCR R, b	Bit clear	$0 \rightarrow R(b)$	None
0010bb brrrrrrr	BSR R, b	Bit set	$1 \rightarrow R(b)$	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if $R(b)=0$	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if $R(b)=1$	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	$n \rightarrow PC$, $PC+1 \rightarrow \text{Stack}$	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	$n \rightarrow PC$	None
110000 nnnnnnnn	CALL n	Call subroutine	$n \rightarrow PC$, $PC+1 \rightarrow \text{Stack}$	None
110001 iiiiii	RTWI i	Return, place immediate to W	$\text{Stack} \rightarrow PC$, $i \rightarrow W$	None
11001n nnnnnnnn	JUMP n	JUMP to address	$n \rightarrow PC$	None

Note :

W	: Working register	b	: Bit position
WT	: Watchdog timer	t	: Target
TMODE	: TMODE mode register	0	: Working register
CPIO	: Control I/O port register	1	: General register
TF	: Timer overflow flag	R	: General register address
PF	: Power loss flag	C	: Carry flag
PC	: Program Counter	HC	: Half carry
OSC	: Oscillator	Z	: Zero flag
Inclu.	: Inclusive 'U'	/	: Complement
Exclu.	: Exclusive '⊕'	x	: Don't care
AND	: Logic AND '∩'	i	: Immediate data (8 bits)
		n	: Immediate address

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9. Electrical Characteristics

(A) Operating Voltage & Frequency

V_{dd} : 2.3 V ~ 6.3 V

Frequency : 0 Hz ~ 20 MHz

(B) Input Voltage

@ $V_{dd}=5.0$ V, Temperature = 25 °C

	Port	Min.	Max.
V_{il}	PA, PB	V_{ss}	1.0 V
	RTCC, /MCLR	V_{ss}	0.8 V
V_{ih}	PA, PB	2.0 V	V_{dd}
	RTCC, /MCLR	3.5 V	V_{dd}

* Threshold Voltage :

Port A, Port B $V_{th}=1.54$ V

RTCC, /MCLR $V_{il}=1.35$ V, $V_{ih}=2.85$ V (Schmitt Trigger)

(C) Output Voltage :

@ $V_{dd}=5.0\text{ V}$, Temperature = $25\text{ }^{\circ}\text{C}$, the typical value as followings :

PA, PB Port	
$I_{oh} = -20.0\text{ mA}$	$V_{oh} = 3.50\text{ V}$
$I_{ol} = 20.0\text{ mA}$	$V_{ol} = 0.60\text{ V}$
$I_{oh} = -5.0\text{ mA}$	$V_{oh} = 4.60\text{ V}$
$I_{ol} = 5.0\text{ mA}$	$V_{ol} = 0.25\text{ V}$

(D) Leakage Current

@ $V_{dd}=5.0\text{ V}$, Temperature = $25\text{ }^{\circ}\text{C}$, the typical value as followings :

I_{il}	$- 1.0\text{ }\mu\text{A (Max.)}$
I_{ih}	$+ 1.0\text{ }\mu\text{A (Max.)}$

(E) Sleep Current

@ **WDT—Disable**, Temperature = $25\text{ }^{\circ}\text{C}$, the typical value as followings :

$$V_{dd}=2.3\text{ V} \sim 6.3\text{ V} \quad I_{dd} < 1.0\mu\text{A}$$

@ **WDT—Enable**, Temperature = $25\text{ }^{\circ}\text{C}$, the typical value as followings :

$V_{dd}=2.3\text{ V}$	$I_{dd} < 1.0\text{ }\mu\text{A}$
$V_{dd}=3.0\text{ V}$	$I_{dd} = 1.2\text{ }\mu\text{A}$
$V_{dd}=4.0\text{ V}$	$I_{dd} = 4.0\text{ }\mu\text{A}$
$V_{dd}=5.0\text{ V}$	$I_{dd} = 12.0\text{ }\mu\text{A}$
$V_{dd}=6.3\text{ V}$	$I_{dd} = 20.0\text{ }\mu\text{A}$

(F) Operation Current

Temperature = $25\text{ }^{\circ}\text{C}$, the typical value as followings :

(i) OSC Type = RC ; WDT—Enable; @ $V_{dd}=5.0\text{ V}$

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	10.26 M	1.35 m
	10.0 K	6.00 M	790.0 μ
	47.0 K	1.476 M	230.0 μ
	100.0 K	724.4 K	135.0 μ
	300.0 K	242.4 K	70.0 μ
	470.0 K	151.6 K	60.0 μ
20P	4.7 K	5.12 M	680.0 μ
	10.0 K	2.774 M	390.0 μ
	47.0 K	640.0 K	125.0 μ
	100.0 K	307.6 K	78.0 μ
	300.0 K	101.2K	55.0 μ
	470.0 K	63.68 K	50.0 μ
100P	4.7 K	1.53 M	240.0 μ
	10.0 K	781.2 K	140.0 μ
	47.0 K	172.4.0K	65.0 μ
	100.0 K	82.0 K	50.0 μ
	300.0 K	27.0 K	47.0 μ
	470.0 K	17.0 K	45.0 μ
300P	4.7 K	633.6 K	125.0 μ
	10.0 K	322.4 K	85.0 μ
	47.0 K	69.60 K	55.0 μ
	100.0 K	33.04 K	50.0 μ
	300.0 K	10.8 K	45.0 μ
	470.0 K	6.84 K	43.0 μ

(ii) OSC Type=LF (C=20 p); WDT—Disable; PED-Disable

Voltage/Frequency	32 K	455 K	1 M	Sleep
2.3 V	4.0 μ A	X	X	<1.0 μ A
3.0 V	6.0 μ A	50.0 μ A	80.0 μ A	<1.0 μ A
4.0 V	15.0 μ A	70.0 μ A	125.0 μ A	<1.0 μ A
5.0 V	30.0 μ A	120.0 μ A	200.0 μ A	<1.0 μ A
6.3 V	40.0 μ A	180.0 μ A	250.0 μ A	<1.0 μ A

(iii) OSC Type=XT (C=10 p); WDT—Enable; PED-Disable

Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	65.0 μ A	210.0 μ A	480.0 μ A	<1.0 μ A
3.0 V	130.0 μ A	360.0 μ A	760.0 μ A	1.2 μ A
4.0 V	220.0 μ A	620.0 μ A	1.25 mA	4.0 μ A
5.0 V	330.0 μ A	980.0 μ A	1.80 mA	12.0 μ A
6.3 V	530.0 μ A	1.7 mA	2.70 mA	20.0 μ A

(iv) OSC Type=HF (C=10 p); WDT—Enable; PED-Disable

Voltage/Frequency	4 M	10 M	20 M	Sleep
2.1 V	190.0 μ A	420.0 μ A	@2.3v900.0 μ A	<0.1 μ A
3.0 V	350.0 μ A	740.0 μ A	1.40 mA	1.2 μ A
4.0 V	670.0 μ A	1.3 mA	2.2 mA	4.0 μ A
5.0 V	1.1 mA	2.0 mA	3.2 mA	12.0 μ A
6.3 V	1.9 mA	3.0 mA	4.7 mA	20.0 μ A

(G) Pull Resistance

@ Input Mode : $V_{dd}=3.0$ V

PORT	Pull-High Resistance	$R_{hi}=300.0$ KOhm
	Pull-Low Resistance	$R_{lo}=300.0$ KOhm
RTCC	Pull-High Resistance	$R_{hi}=280.0$ KOhm
	Pull-Low Resistance	$R_{lo}=280.0$ KOhm
/MCLR	Pull-High Resistance	$R_{hi}=150.0$ KOhm

@ Input Mode : $V_{dd}=5.0$ V

PORT	Pull-High Resistance	$R_{hi}=100.0$ KOhm
	Pull-Low Resistance	$R_{lo}=100.0$ KOhm
RTCC	Pull-High Resistance	$R_{hi}=110.0$ KOhm
	Pull-Low Resistance	$R_{lo}=110.0$ KOhm
/MCLR	Pull-High Resistance	$R_{hi}=100.0$ KOhm

p.s. : It is only a reference value for the Pull High/Low Resistance, and the accurate

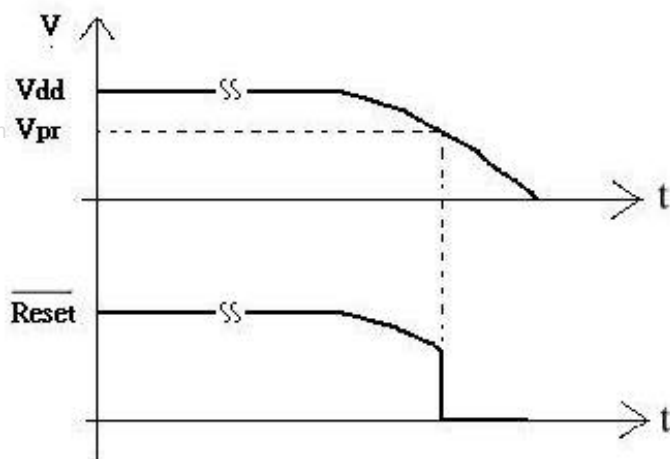
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value of the Resistance depends on the various parameter of the Process. But the variation of the value will be not more than 20%.

(H) Power Edge-detector Reset Voltage (Not in Sleep Mode), @ $V_{dd}=5.0\text{ V}$

$$V_{pr} \leq 1.1\sim 1.3\text{ V}$$

$V_{pr} : V_{dd}$ (Power Supply)



(I) The basic WDT time-out cycle time

Temperature = 25 °C, the typical value as followings :

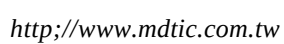
Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	34.00
3.0	27.60
4.0	23.20
5.0	20.40
6.3	18.00

(J) MCLR Filter : @ $V_{dd}=5.0\text{v}$

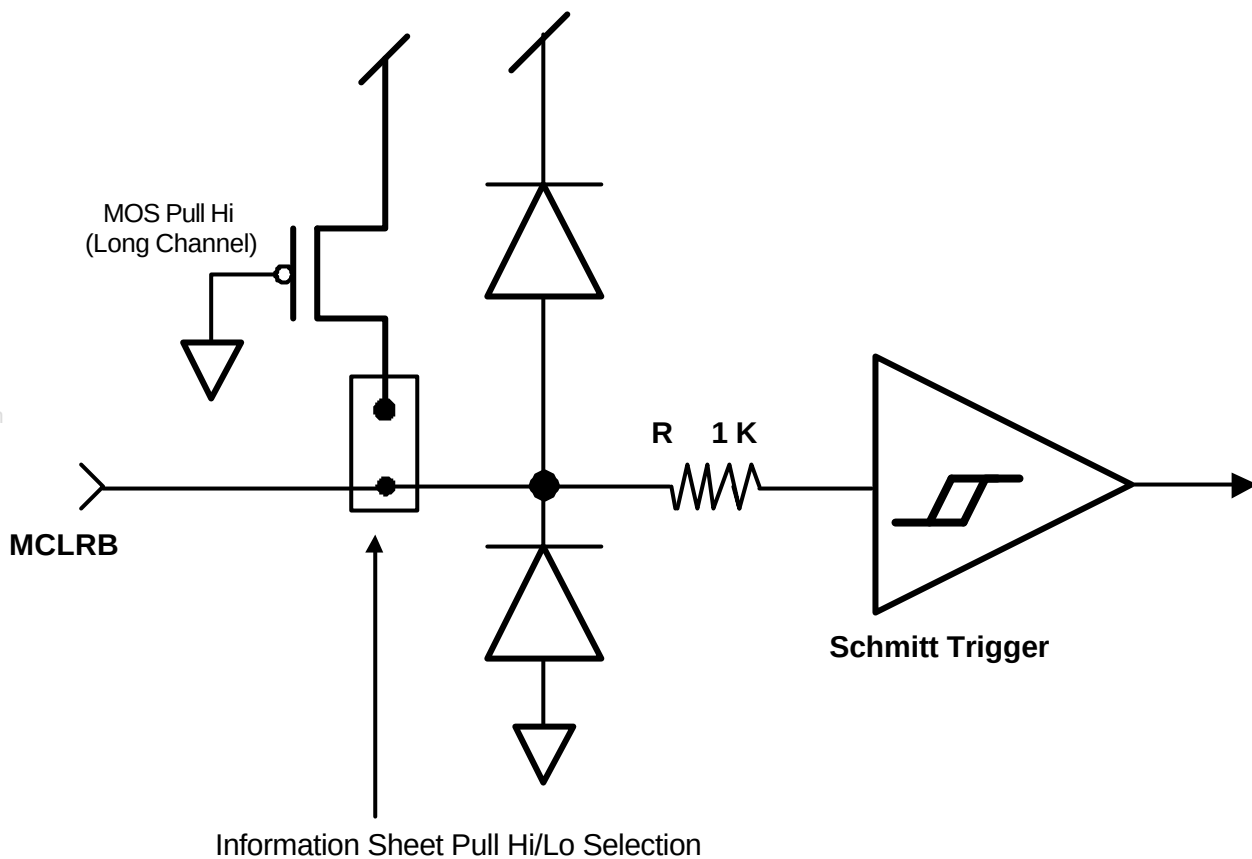
$$W_m \geq 1.2\mu\text{s}$$

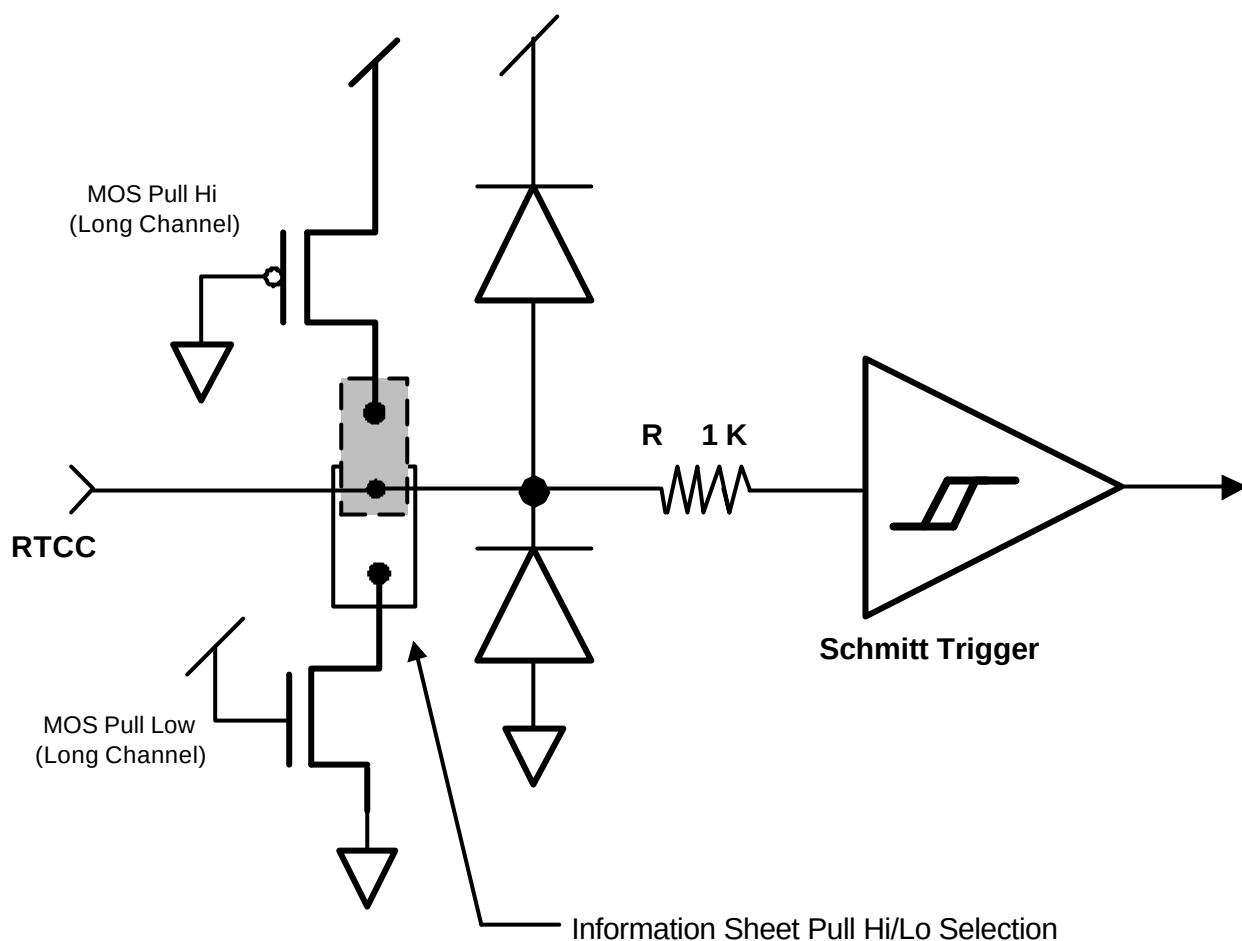
W_m : Filter pulse width (low) in /MCLR pin.

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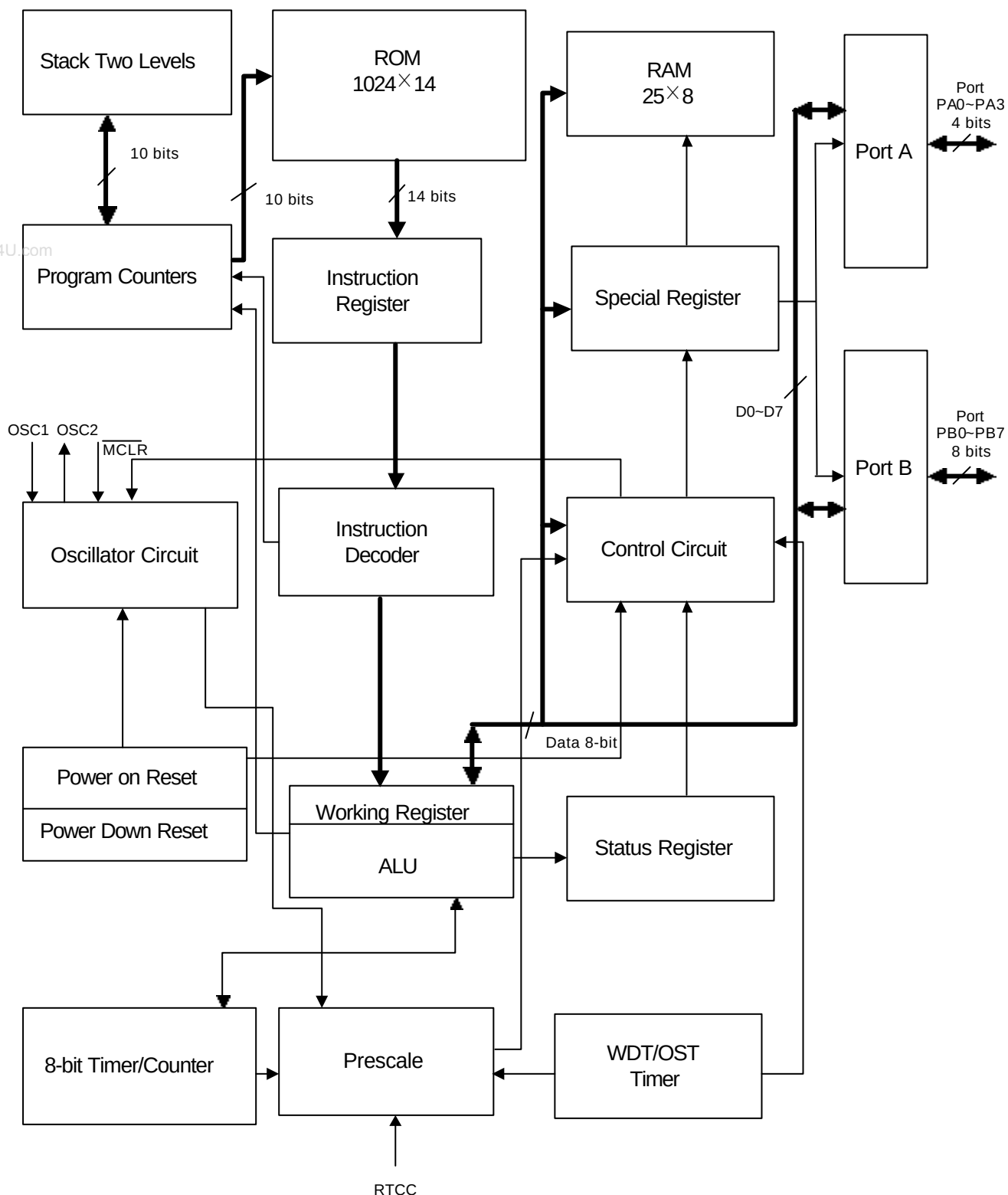


11. MCLRB and RTCC Input Equivalent Circuit





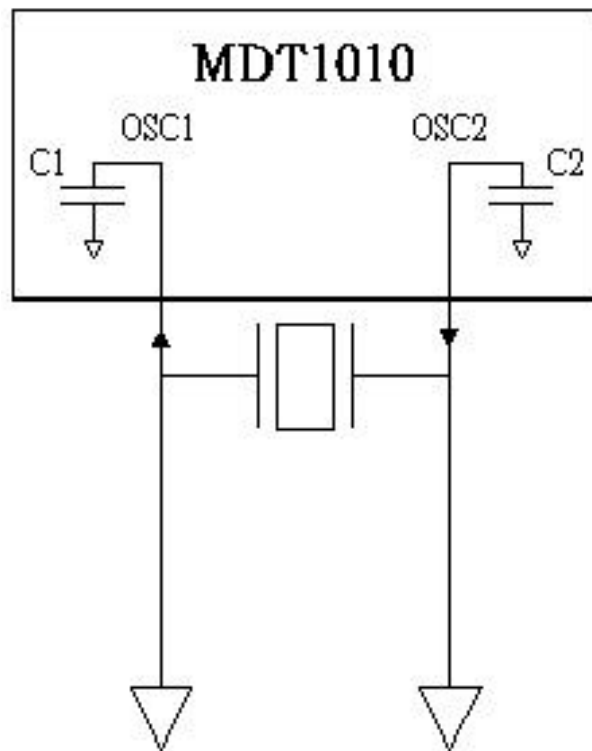
12. Block Diagram



13. Capacitor Selection For Crystal Oscillator

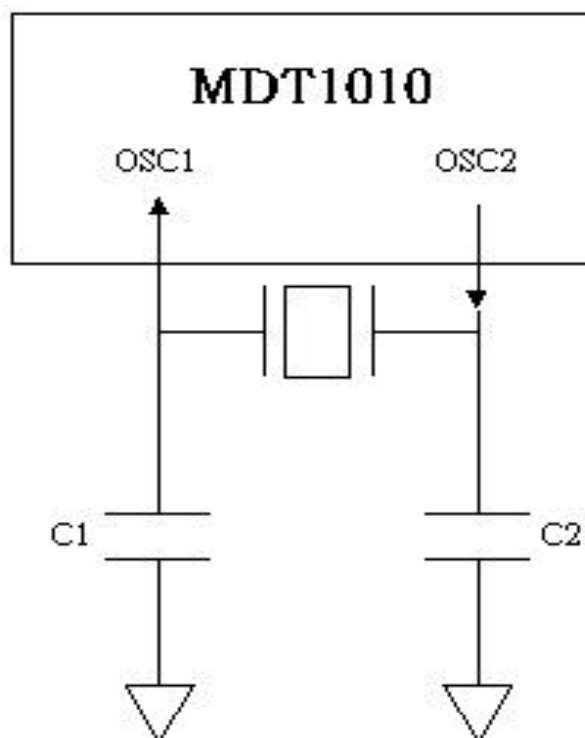
(a) With built-in Oscillation Capacitors (Default for HF,XT,LF)

@ $V_{dd} = 2.3V \sim 5.5 V$, $C1 = C2 = 10P \sim 15P$



(b) Without built-in Oscillation Capacitors@ $V_{dd} = 3.0\text{ V} \sim 5.0\text{ V}$

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	5 pF ~10 pF	10 pF~30 pF
	10 MHz	10 pF ~50 pF	20 pF ~100 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor range are recommended, but the higher capacitance will increase the start-up time.
There do not have built-in Oscillation Capacitors for RC type.

