RoHS Compliant

MagnaChip

MDU5593S

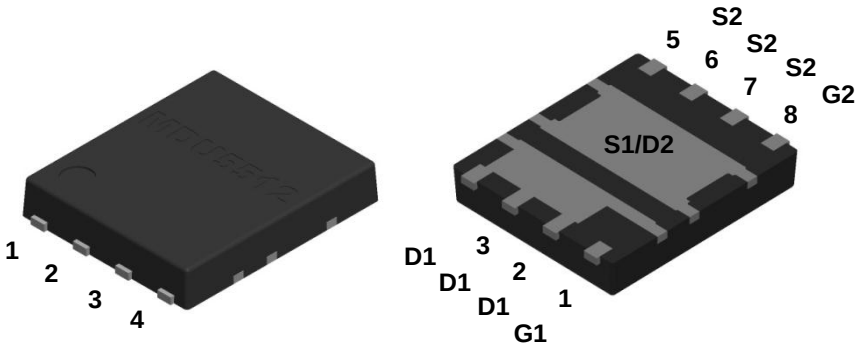
Dual Asymmetric N-channel Trench MOSFET 30V

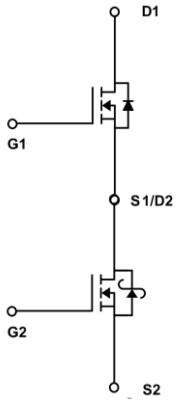
General Description

The MDU5593S uses advanced MagnaChip's MOSFET Technology, which provides high performance in on-state resistance, fast switching performance and excellent quality. MDU5593S is suitable for DC/DC converter and general purpose applications.

Features

	FET1	FET2
▫	V_{DS} = 30V	V_{DS} = 30V
▫	I_D = 34A	I_D = 40A @V_{GS} = 10V
▫	$R_{DS(ON)}$	
	< 8.0mΩ	< 3.3mΩ @V_{GS} = 10V
	< 11.0mΩ	< 5.0mΩ @V_{GS} = 4.5V
▫	100% UIL Tested	
▫	100% Rg Tested	





Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	FET1	FET2	Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current (1)	T_C=25°C (Silicon Limited)	I_D	52	95	A
	T_C=25°C (Package Limited)		34	40	
	T_A=25°C		13	21	
Pulsed Drain Current		I_{DM}	40	100	A
Power Dissipation	T_C=25°C	P_D	35.7	44.6	W
	T_A=25°C		2.2	2.5	
Single Pulse Avalanche Energy (2)		E_{AS}	60	60	mJ
Junction and Storage Temperature Range		T_J, T_{stg}	-55~150		°C

Thermal Characteristics

Characteristics	Symbol	FET1	FET2	Unit
Thermal Resistance, Junction-to-Ambient (1)	$R_{\theta JA}$	57	50	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.5	2.8	

Ordering Information

Part Number	Temp. Range	Package	Packing	RoHS Status
MDU5591SVRH	-55~150°C	Dual PDFN56	Tape & Reel	Halogen Free

FET1 Electrical Characteristics (Ta =25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.8	3.0	
Drain Cut-Off Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	-	-	1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±0.1	
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	-	5.1	8.0	mΩ
		V_{GS} = 4.5V, I_D = 11A	-	7.2	11.0	
Forward Transconductance	g_{fs}	V_{DS} = 5V, I_D = 13A	-	35	-	S
Dynamic Characteristics						
Total Gate Charge	$Q_{g(10V)}$	V_{DS} = 15.0V, I_D = 10A, V_{GS} = 10V	-	18.0	-	nC
Total Gate Charge	$Q_{g(4.5V)}$		-	9.5	-	
Gate-Source Charge	Q_{gs}		-	3.2	-	
Gate-Drain Charge	Q_{gd}		-	3.2	-	
Input Capacitance	C_{iss}	V_{DS} = 15.0V, V_{GS} = 0V, f = 1.0MHz	-	1,142	-	pF
Output Capacitance	C_{oss}		-	446	-	
Reverse Transfer Capacitance	C_{rss}		-	83	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=15V, I_D=10A, R_g=3Ω	-	9.9	-	ns
Rise Time	t_r		-	12.1	-	
Turn-Off Delay Time	$t_{d(off)}$		-	28.5	-	
Fall Time	t_f		-	6.9	-	
Gate Resistance	Rg	f=1 MHz	-	1.0	-	Ω
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	I_S = 1A, V_{GS} = 0V	-	0.7	1.0	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10A, dI/dt = 100A/μs	-	31.8	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	29.4	-	nC

Note :

1. Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at T_C=25℃ is silicon limited.
2. E_{AS} is tested at starting T_j = 25℃, L = 0.5mH, I_{AS} = 15.5A, V_{DD} = 27V, V_{GS} = 10V. And 100% UIL Test at L = 0.1mH, I_{AS} = 18.0A.

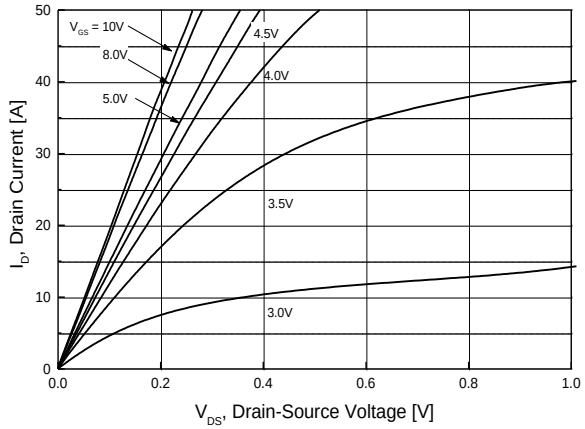


Fig.1 On-Region Characteristics

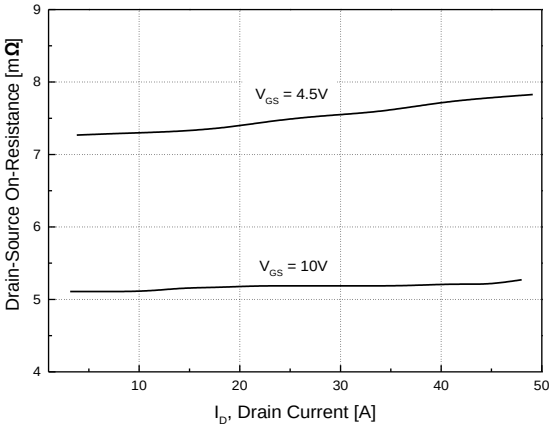


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

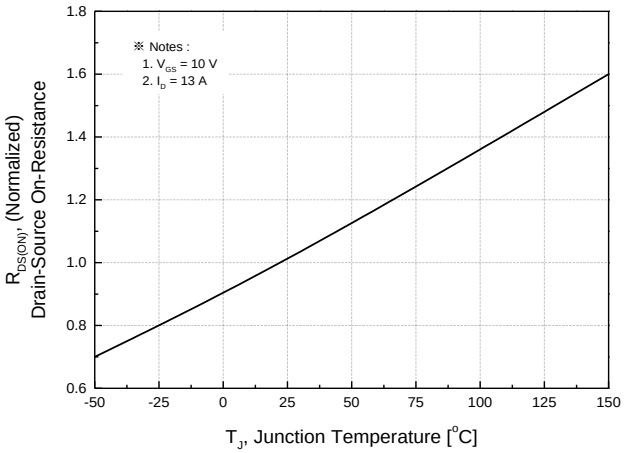


Fig.3 On-Resistance Variation with

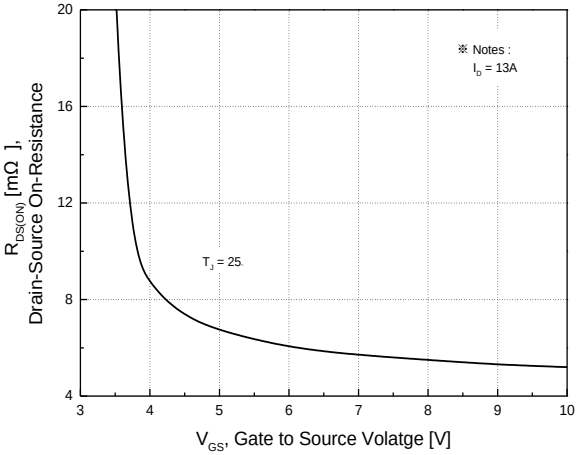


Fig.4 On-Resistance Variation with Gate to Source Voltage

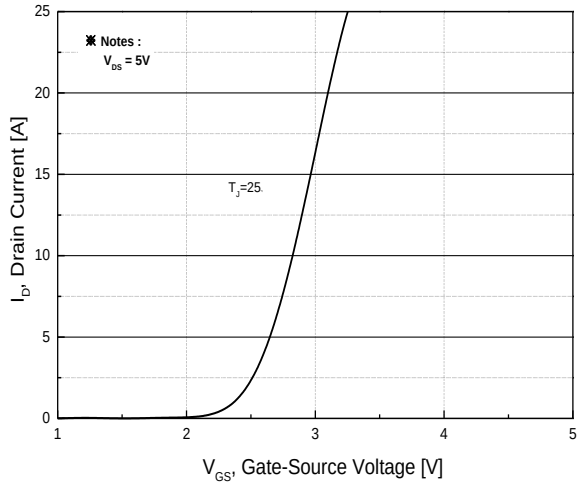


Fig.5 Transfer Characteristics

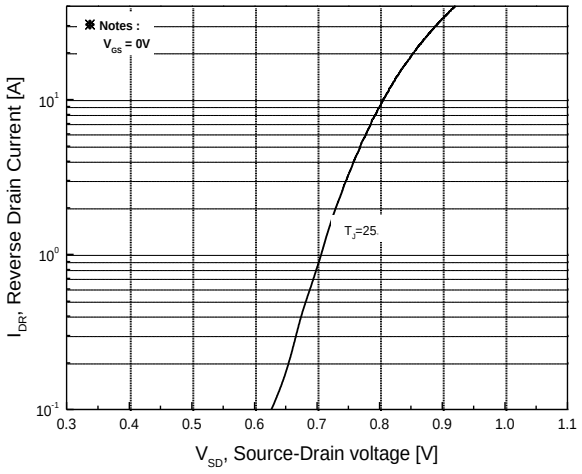


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

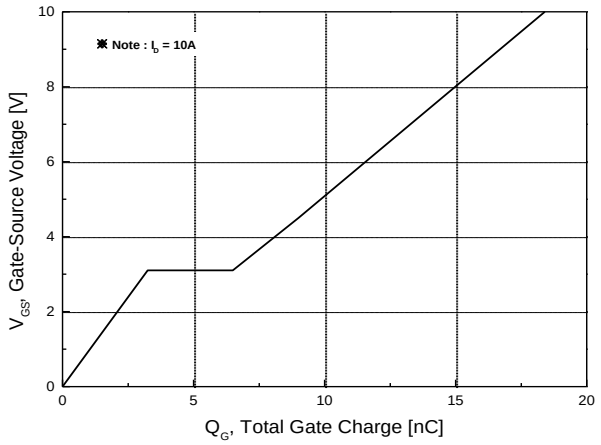


Fig.7 Gate Charge Characteristics

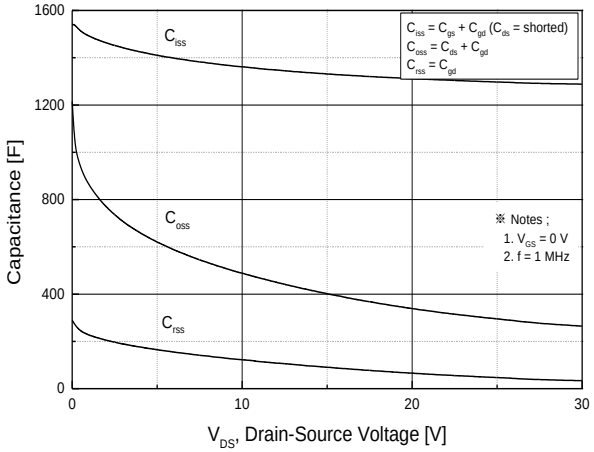


Fig.8 Capacitance Characteristics

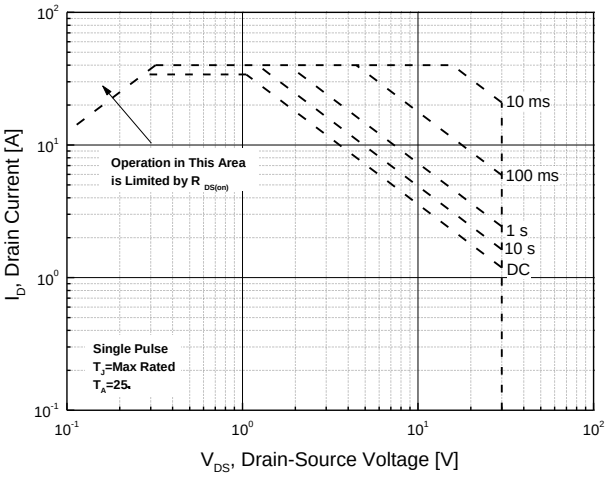


Fig.9 Maximum Safe Operating Area

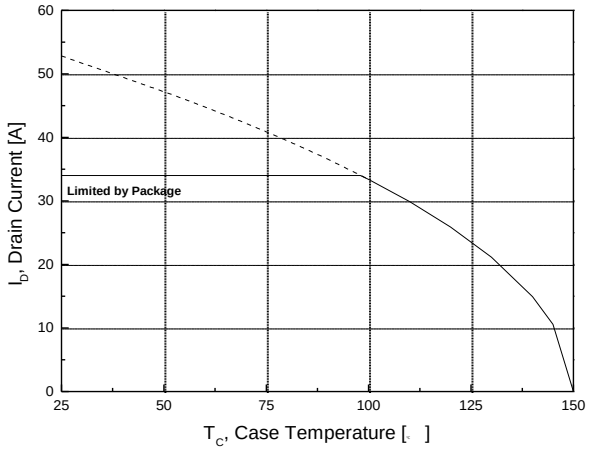


Fig.10 Maximum Drain Current vs. Case Temperature

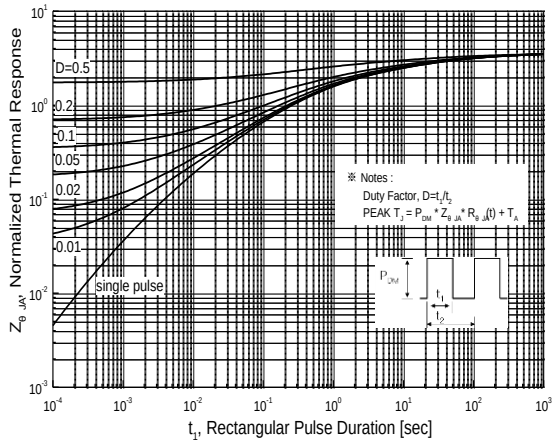


Fig.11 Transient Thermal Response Curve

FET2 Electrical Characteristics (Ta =25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.8	3.0	
Drain Cut-Off Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	-	-	500	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±0.1	
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 27A	-	2.8	3.3	mΩ
		V_{GS} = 4.5V, I_D = 21A	-	4.0	5.0	
Forward Transconductance	g_{fs}	V_{DS} = 5V, I_D = 21A	-	46	-	S
Dynamic Characteristics						
Total Gate Charge	$Q_{g(10V)}$	V_{DS} = 15.0V, I_D = 20A, V_{GS} = 10V	-	26.1	-	nC
Total Gate Charge	$Q_{g(4.5V)}$		-	12.6	-	
Gate-Source Charge	Q_{gs}		-	4.5	-	
Gate-Drain Charge	Q_{gd}		-	4.2	-	
Input Capacitance	C_{iss}	V_{DS} = 15.0V, V_{GS} = 0V, f = 1.0MHz	-	1785	-	pF
Output Capacitance	C_{oss}		-	652	-	
Reverse Transfer Capacitance	C_{rss}		-	98	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=15V, I_D=20A, R_g=6Ω	-	11.9	-	ns
Rise Time	t_r		-	8.9	-	
Turn-Off Delay Time	$t_{d(off)}$		-	45.5	-	
Fall Time	t_f		-	14.5	-	
Gate Resistance	Rg	f=1 MHz	-	1.0	-	Ω
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	I_S = 1.0A, V_{GS} = 0V	-	0.4	0.7	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 27A, dI/dt = 150A/μs	-	33.2	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	28.5	-	nC

Note :

1. Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at T_C=25℃ is silicon limited.
2. E_{AS} is tested at starting T_j = 25℃, L = 0.5mH, I_{AS} = 15.5A, V_{DD} = 27V, V_{GS} = 10V. And 100% UIL Test at L = 0.1mH, I_{AS} = 18.0A.

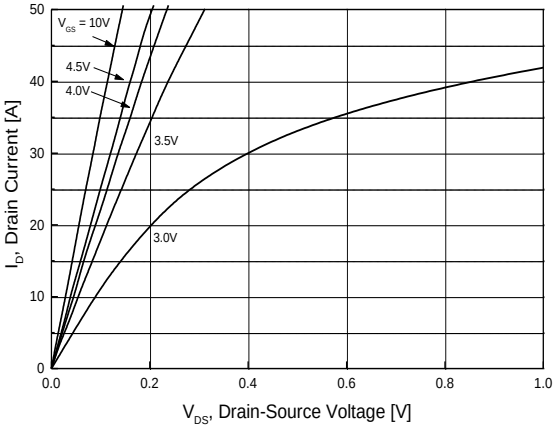


Fig.1 On-Region Characteristics

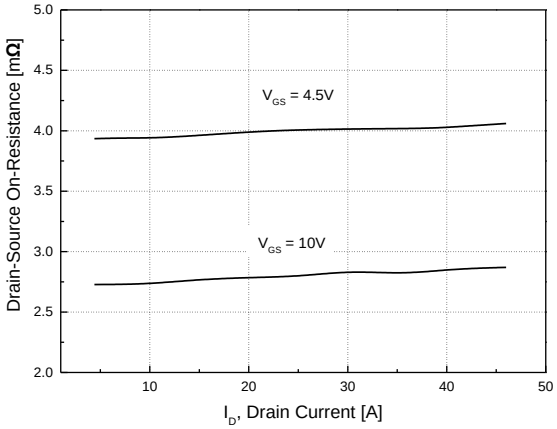


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

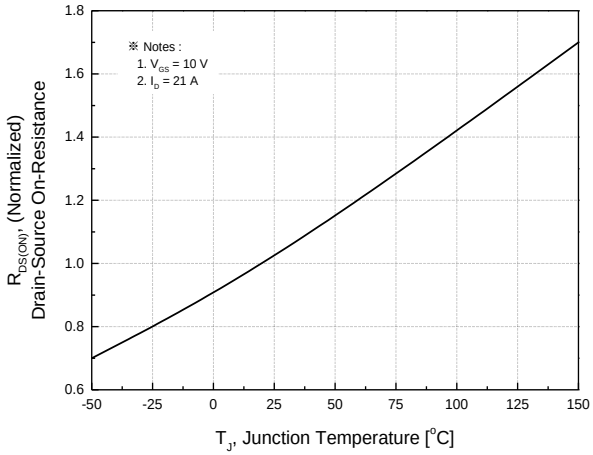


Fig.3 On-Resistance Variation with

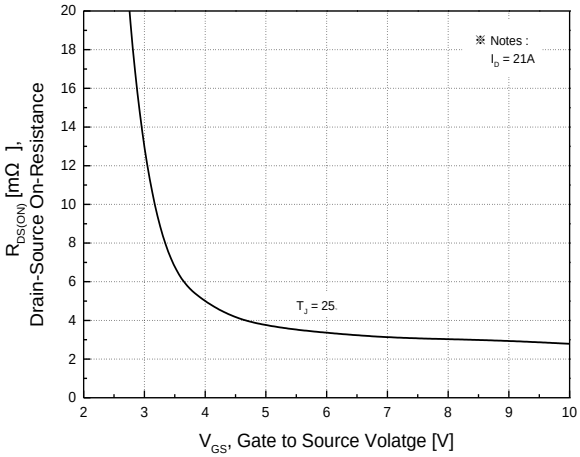


Fig.4 On-Resistance Variation with Gate to Source Voltage

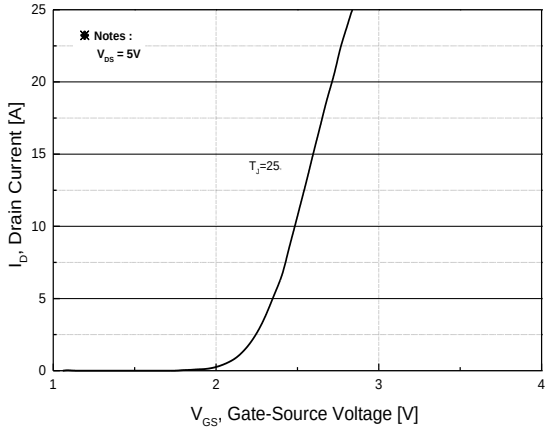


Fig.5 Transfer Characteristics

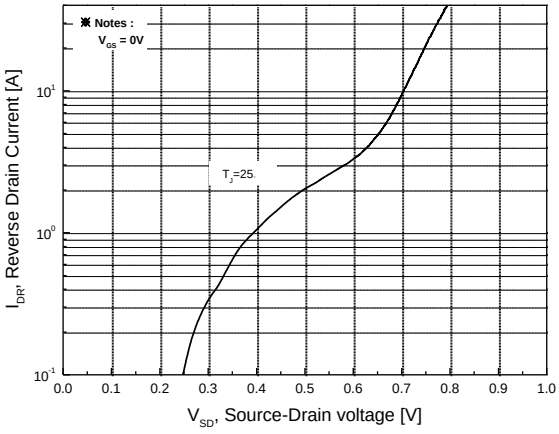


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

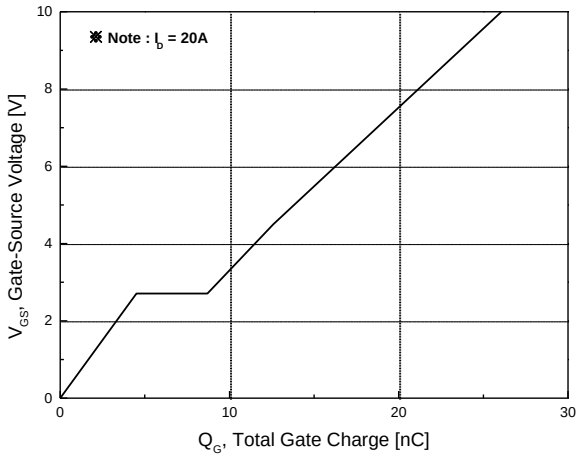


Fig.7 Gate Charge Characteristics

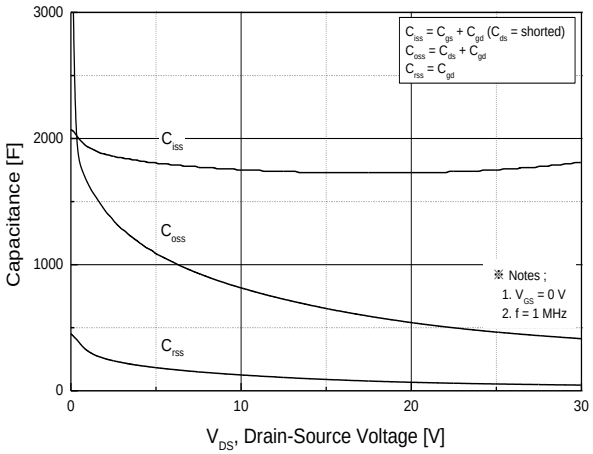


Fig.8 Capacitance Characteristics

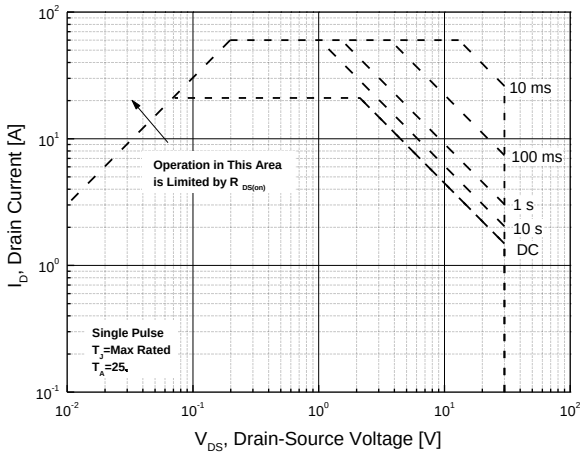


Fig.9 Maximum Safe Operating Area

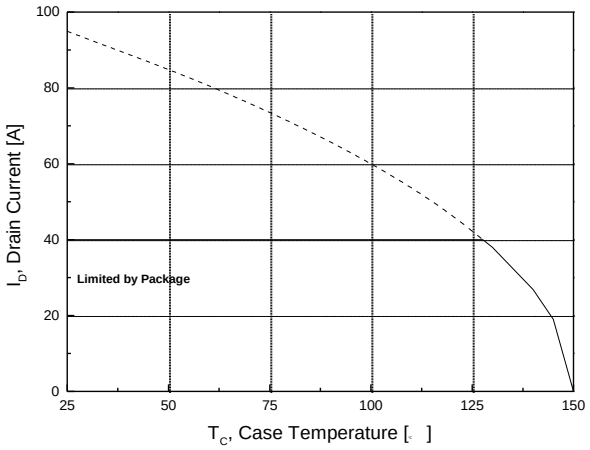


Fig.10 Maximum Drain Current vs. Case Temperature

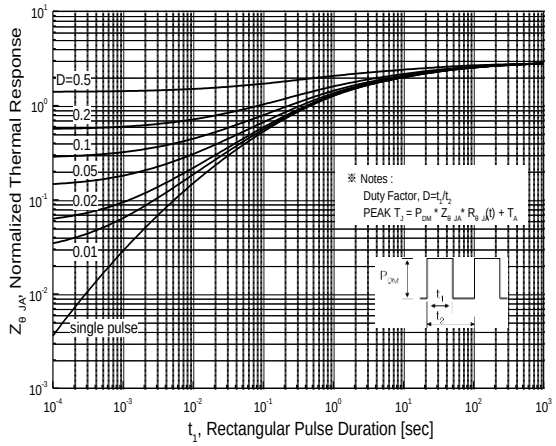
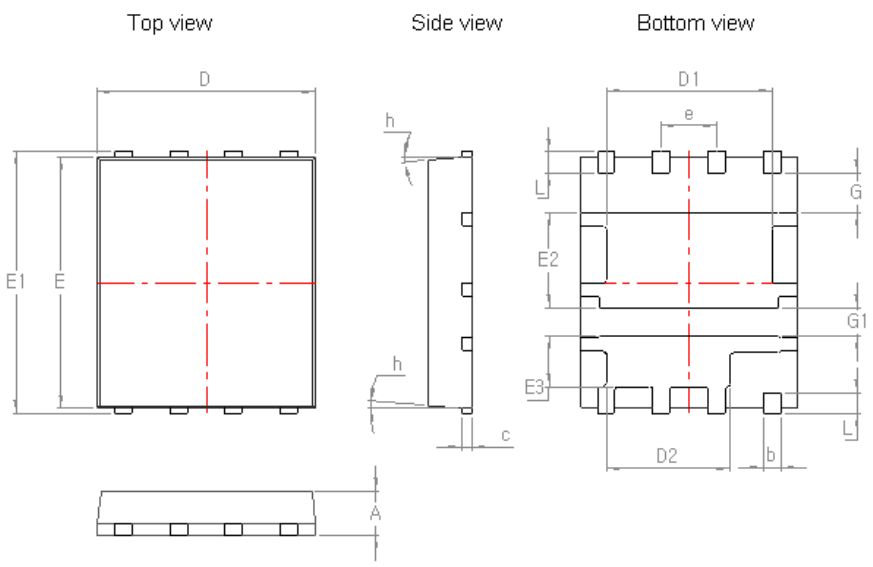


Fig.11 Transient Thermal Response Curve

Package Dimension

Dual PDFN56 (5x6mm)

Dimensions are in millimeters, unless otherwise specified



Symbol	Dimension [mm]		
	Min	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D	4.80	5.00	5.20
D1	3.60	3.80	4.00
D2	2.64	2.84	3.04
E	5.70	5.75	5.80
E1	5.90	6.00	6.10
E2	2.00	2.25	2.50
E3	1.10	1.20	1.30
e	1.27 BSC		
G	0.50	-	-
G1	0.40	0.60	0.80
h	0 °	-	12 °
L	0.38	0.55	0.71

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.