SPECIFICATION

DVBS TUNER Revision:1.0

1.SCOPE

The MDVBS2-6613 supports QPSK in DIRECTV and DVB-S legacy transmission (1 to 45 Mbauds), plus 8PSK in DVB-S2 transmissions (1 to 45 Mbauds). DVB-S2 demodulation uses robust symbols probust by the transmission to ensure efficient carrier tracking. Carrier and timing recovery loops are fully digital and tunable. Carrier-to-noise ratio (CNR) calculation and constellation display are also supported.

2.GENERAL SPECIFICATIONS

2-1. Receiving Frequency : 950~2150 MHz

2-2. RF Input Impedance : 75 OHM

2-3. RF Loop out Impedance : 75 OHM

2-4. LO PLL Synthesizer IC : Built in PLL
(I²C Bus: SPHE6010A)

2-5. RF Input Connector : F Type (Female)

2-6. RF Loop out Connector : F Type (Female)

2-7. PLL Step Size : 1MHz

2-8. Operating Voltage .LNB Power :DC By PASS to RF IN 20V/400mA max
.Supply Voltage
1)Supply voltage for Tuner IC and DMIC:B2, 3.3V
2)Supply voltage for DMIC : B1, 1.2V

Pin No.	Min.	Typ.	Max.
6	3.1V	3.3V	3.5V
4	1.15V	1.2V	1.32V

2-9. Temperature Range
Storage Temperature : -20°C ~ + 80°C
Operation Temperature : 0°C ~ + 50°C

3-0. Weight :24.4g

3.TEST CONDITIONS

3-1. Test conditions : All data held under following conditions
: +25+/-2°C / Humidity : 45 ~ 65% RH

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4.ELECTRICAL SPECIFICATION OF THE RF TUNER

Test Condition	1.Supply Voltage 1-1 Supply Voltage (B2) : 3.3V +/- 0.1V DC 1-2 Supply Voltage (B1) : 1.2V +/- 0.05V DC 2.Ambient Temperature : 25°C +/- 5°C 3.Ambient Humidity : 65% +/- 10%

Parameter	Conditions	Min	Typ	Max	Units
RF front-end					
Operating Frequency Range		950		2150	MHz
Overall Voltage Gain	Max. at VAGC=0.5			96	dB
	Min. at VAGC=2.5	-2			dB
Input Return Loss	Reference to 75Ω	-7	-10		dB
Noise Figure	Maximum Gain		7	8	dB
RF AGC Gain Control Range	VAGC from GND to VDD		74		dB
RF AGC input impedance			100k		Ohm
Out-band IIP3	Input power = -25dBm		5		dBm
IIP2	Input power = -25dBm		20		dBm
LO 2nd harmonic rejection			50		dBc
LO leakage to RF input			-70		dBm
Baseband Output					
I/Q output load (diff.)		1k			Ohm
				10	pF
Differential I/Q output voltage			1		Vpp
Differential I/Q output impedance	AC Coupling Case		50		Ohm
	SIP Case		400		Ohm

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Parameter	Conditions	Min	Typ	Max	Units
Channel filter 3dB BW	1MHz per step	5		40	MHz
Channel filter BW accuracy			+/- 2.5	+/- 5	%
Group delay	BW=5MHz			110	ns
High-pass 3dB frequency	Normal mode		500		Hz
Quadrature Gain match		-1		1	dB
Quadrature Phase match		-3		3	Deg.
I/Q output DC offset			8		mV
I/Q channel in band ripple				1	dB
Baseband Gain control range	2dB per step by I2C		20		dB
Synthesizer					
Crystal Oscillator Frequency	+/- 50 ppm		16		MHz
Phase Noise (Single Side Band, Close Loop)	10KHz Offset 100KHz Offset 1MHz Offset		-95 -93 -115		dBc/Hz dBc/Hz dBc/Hz
LOOP THROUGH PATH					
Gain		-2		2	dB
NF	Reference to 50Ohm		8		dB
OIP3			10		dBm
OIP2			10		dBm
Output return loss	Reference to 75Ohm	6	7		dB
2-WIRE SERIAL OUTPUT					
2-Wire Serial Interface Clock				400	kHz

Current Consumption

Pin No.	Parameter	Min.	Typ.	Max.
6	B2 3.3V(DVBS)		324	mA
	B2 3.3V(DVBS2)		324	mA
4	B1 1.2V (DVBS)		192	mA
	B1 1.2V (DVBS2)		215	mA

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DVB-S/S2 BASEBAND DEMODULATOR

1.GENERAL DESCRIPTION

1.1. Introduction

SPHE6613A is the a single-chip QPSK/8PSK satellite demodulator, which is compliant with DVB-S (as defined in ETS 300 421 specification) and DVB-S2 (as defined in ETS 302 307 specification). It can support different symbol rates from 1 MHz to 45 MHz.

The device integrates dual high performance 8-bit A/D converters. The sampling rates can be generated from different clock sources: either. It may be from a 27 MHz crystal or anthe external clock (4/10/10.11/15/16 MHz from tuner). and cChanginge the setting ofin the relative register can to achieve the target sampling rate.

The QPSK/8PSK demodulator can do the channel blind search and confirmed the channel by the lock criteria. Inner channel decoders includes Viterbi decoder and LDPC decoder. Viterbi decoder can detect the code rate automatically without any extra information. LDPC decoder needs the code rate information from the previous processing to complete the decoding. BesidesExcept that, the FEC part can provide users many helpful information including pre-Viterbi/pre-LDPC BER and post-Viterbi/post-LDPC BER. Users also can define the capture range for BER calculation. Serial or parallel MPEG transport stream output can be interfaced to all commercial processor chips.

Through an I2C-like serial bus, programming can be done by using the command interface. Because the RF tuner module is noise-sensitive, the host processor can control the RF tuner module through this chip to reduce the noise interference.

The Base band controller controls all blind channel scan, acquisition and tracking operations.

The SPHE6613A has been designed with not only the latest technology but also the full service and support of Sunplus.

1.2. Terms

Abbreviation	Definition
BER	Bit Error Rate
CFO	Center Frequency Offset
CRL	Carrier Recovery Loop
DAGC	Digital Auto Gain Control
DVB-S	Digital Video Broadcasting - Satellite
EQU	Equalizer
FEC	Forward Error Corrector
IF	Intermediate Frequency
ITP	Digital Interpolator
LNB	Low Noise Block Down Converter
NCO	Numeric Control Oscillator
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SIGD	Signal Detection
SRD	Symbol Rate Detector
SRRC	Square-Root Raised Cosine
TRL	Timing Recovery Loop

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2.FEATURES

- Architecture
  - On-chip 8 bits dual ADC (sampling rate up to 92MHz)
  - Embedded PLL to provide clock, only need external crystal
  - DVB-S Demodulator compliant with EN300421
  - DVB-S Channel decoder compliant with EN300421
  - DVB-S2 Demodulator compliant with EN302307
  - DVB-S2 Channel decoder compliant with EN302307
  - DiSEqCTM v2.2 receive/transmit for the control of LNB, dish and other components
  - Single AGC interface
  - Parallel or serial transport stream interface
- I2C Controller
  - Two interfaces: to RF tuner and to MPEG2 decoder chip respectively
  - Master and slave modes
  - Slave transmit/receive modes
  - Programmable clock speed while in the master mode
- Base-band Controller
  - H/W accelerator for blind channel scan
  - H/W accelerator for auto re-acquisition
- QPSK/8PSK Demodulator
  - DC removal up to 20% DC offset
  - Cover I/Q imbalance - amplitude 3dB and phase 10 degree
  - Digital SAW filter reducing the analog complexity and enhancing the co-channel performance
  - Fast acquisition and robust tracking utilizing blind and decision based techniques
  - Automatic pre/post echo detection and smart equalizer which is capable of multi-path rejection from -5 symbol to +10 symbol time
  - Carrier acquisition range of 25% symbol rate
  - Automatic digital timing recovery up to 10000ppm (no VCO required)
  - Integrated de-interleaver memory supporting maximum required depths
  - Interface provided for front-end analogue to digital converter with AGC loop control
  - Automatic code rate detection in Viterbi decoder
  - Automatic inverse compensation in Reed Solomon decoder
  - PL header parsing for LDPC code rate and constellation
  - Supportsed symbol rate from 1 ~ 45Msps for DVB-S and DVB-S2 8PSK
  - Supported received modes for DVB-S2:

System Configuration	Case	Supported
QPSK	1/4, 1/3, 2/5	No
	1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10	Yes
8PSK	3/5, 2/3, 3/4, 5/6, 8/9, 9/10	Yes
16APSK	2/3, 3/4, 4/5, 5/6, 8/9, 9/10	No
32APSK	3/4, 4/5, 5/6, 8/9, 9/10	No
CCM		Yes
VCM		No
ACM		No
FEC FRAME (normal)		Yes
FEC FRAME (short)		No
Single Transport Stream		Yes
Multiple Transport Stream		Yes
Single Generic Stream		No
Multiple Generic Stream		No
Combined Single Generic & Single Transport Stream		No
Roll-Off Factor	0.35, 0.25, 0.2	Yes
ISSY		No
Null Packet Detection		No
Dummy Frame Insertion		No
SOF & NCR Synchronization		No

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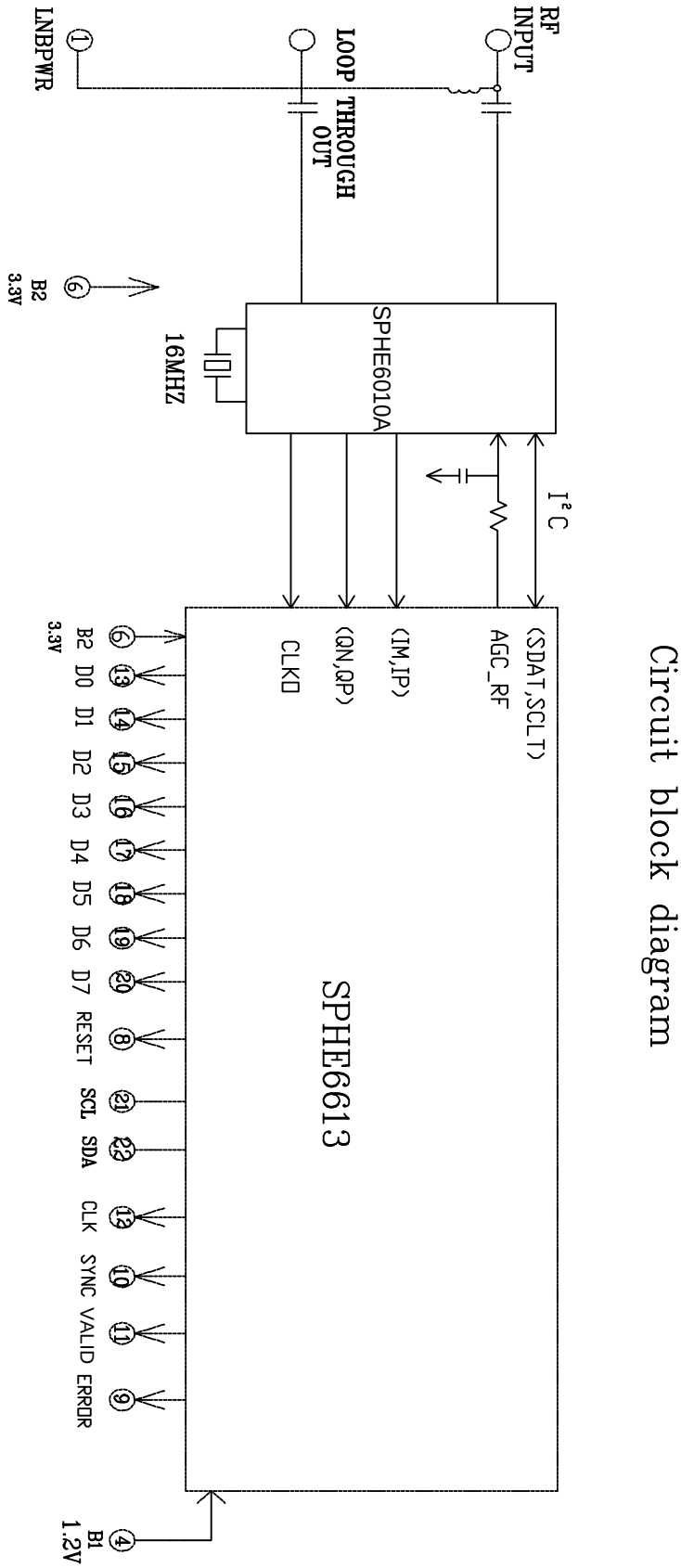

Circuit block diagram

4.FUNCTIONAL DESCRIPTIONS

4.1. ADC

SPHE6613A integrates dual high-performance 8-bit A/D converters. The sampling rates are derived from different clock sources which may be either a 27 MHz crystal or an external clock (4/10/10.11/15/16 MHz from tuner). Properly programming relative registers may achieve the target sampling rate.

4.2. DFE (Digital Front End)

The DFE is the kernel part of the SPHE6613A. It can do the channel blind search and confirm the channel by the lock criteria. In this block, the television signals are processed with advanced digital signal technology to remove the noise and distortions, thus forming a demodulated and decoded data stream.

4.2.1. TRL (Timing Recovery Loop)

This block provides an NCO (Numeric Control Oscillator) and a loop integrator so that the timing phase value and the sample clock for interpolation can be generated. Besides, the block also corrects timing offsets in the sample clock by the use of the interpolation between incoming data samples. The effective output sampling rate of the ITP (digital interpolator) block is as twice as the symbol rate.

4.2.2. DAGC (Digital Auto Gain Control)

Thise block keeps the signal at the right level in order to compensate the effect of the following digital filter.

4.2.3. SRRC (Square-Root Raised Cosine)

The SRRC block is a 128-tap digital filter which is used to match the transmitted pulse. Parallel processing for in-phase and quad-phase parts is are adopted.

4.2.4. SRD (Symbol Rate Detector)

Thise block executes the symbol rate estimation relying on the SRRC output. It can be handled by either the **host** driver or the H/W state machine. When controlled by H/W, the speed of the blind channel search can be accelerated around ten times.

4.2.5. PS (Peak Search)

Thise block performs the detection of frame's boundary by using the header correlation. The pilot signal detection is also done here.

4.2.6. AFC (Center Frequency Offset)

Thise block estimates the offset of the center frequency based on the output of SRRC. Like SRD, this module can be controlled by either the host driver or the H/W state machine.

4.2.7. NCO (Numeric Control Oscillator)

The NCO will generate sine/cosine values depending on the input frequency compensation.

4.2.8. PLC (PiLot Check)

For DVB-S2 transmission, pilot signal insertion is optional can be inserted or not. Thise block can detects the existence of the pilot signal and then remove itthe pilot from the frame.

4.2.9. EQU (Equalizer)

Thise block performs the echo cancellation ranging from -5 symbols to +10 symbols.

4.2.10. PLS Processor

Thise block can decode the header information includinges LDPC code rate and QPSK/8PSK mode, t. Then demap the incoming samples from the symbol into the corresponding constellation. If **DVB-S** is used, this block only implementsdo the demapping process and then directly passes the data to the FEC directly.

4.3. FEC

In particular, a proposed FEC (Forward Error Corrector) design is implemented here with a Reed-Solomon decoder and a Viterbi decoder for DVB-S, a BCH decoder and a LDPC decoder for DVB-S2. Besides, the FEC part provides users helpful information including pre-Viterbi/pre-LDPC BER and post-Viterbi/post-LDPC BER. Users also can define the capture range for BER calculation.

4.3.1. Viterbi Decoder

Thise block detects code rates automatically. The code rates are defined in the DVB-S specification.

4.3.2. Reed-Solomon Decoder

It is fully compliant with the DVB channel coding requirements for satellite broadcast and uses a version of a RS(255,239) code that is shortened to a RS(204,188) code.

4.3.3. LDPC Decoder

The supported code rate is defined in the Chap. 2. The popular LDPC decoding algorithms are:

(i) Sum-Product Algorithm (SPA) - Best performance (bound)

(ii) Min-Sum Algorithm (MS) - Lowest implementation complexity

(iii) Min-Sum with Correction (MSC) - Compensation for Min-Sum

approximation

Considering the complexity, we adopt the method (iii) in this project. In order to compensate the disadvantage, some modifications are also is used in this project:

(i) Multiple Scaling - In min-sum algorithm, the most minimum and second minimum are applying different scaling factors.

(ii) Early termination of scaling - Inspired by proposed varying scaling factor, it can further improve decoding performance in last several iteration, and scaling method may not be needed.

4.3.4. BCH Decoder

BCH is a kind of block code. The Its error correction capability is shown in the following:

4.4. P2S

This block serves as an MPEG formatter. It can process the data stream decoded by the QPSK/8PSK Demodulator into serial or parallel MPEG2 transport stream. This data then can be interfaced to almost all commercial MPEG2 decoder chips.

4.5. I2C Controller

The I2C controller provides two serial bus interfaces respectively to the RF tuner and to the host processor in the MPEG2 decoder. Through the I2C bus, the SPHE66130A can be controlled and programmed by the host processor. The control to the RF tuner module from the host processor can also be relayed by the I2C interface in order to reduce the noise interference.

Besides, it can work in both master and slave modes. While in the master mode, its clock speed is programmable.

4.6. Base-Band Controller

A base-band controller is included in the SPHE6613A to control all blind channel search, acquisition and tracking operations.

Table 5a: coding parameters (for normal FECFRAME n_{ldpc} = 64 800)

LDPC code	BCH Uncoded Block K_{bch}	BCH coded block N_{bch} LDPC Uncoded Block k_{ldpc}	BCH t-error correction	LDPC Coded Block n_{ldpc}
1/4	16 008	16 200	12	64 800
1/3	21 408	21 600	12	64 800
2/5	25 728	25 920	12	64 800
1/2	32 208	32 400	12	64 800
3/5	38 688	38 880	12	64 800
2/3	43 040	43 200	10	64 800
3/4	48 408	48 600	12	64 800
4/5	51 648	51 840	12	64 800
5/6	53 840	54 000	10	64 800
8/9	57 472	57 600	8	64 800
9/10	58 192	58 320	8	64 800

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5. ELECTRICAL SPECIFICATION OF THE CHANNEL

Eb/NO THRESHOLOD PERFORMANCE

MODE	CODE RATE	C/N (Max.)	Unit
DVB.S	1/2	4.2	
	2/3	4.8	
	3/4	5.8	
	5/6	6.9	
	7/8	7.6	
DSS	2/3	4.5	
	6/7	6.7	
DVB.S2 (LDPC+BCH QPSK)	1/2	1.0	dB
	3/5	2.3	
	2/3	3.1	
	3/4	4.1	
	4/5	4.7	
	5/6	5.2	
	8/9	6.2	
	9/10	6.5	
DVB.S2 (LDPC+BCH 8PSK)	3/5	5.5	
	2/3	6.6	
	3/4	7.9	
	5/6	9.4	
	8/9	10.7	
	9/10	11.0	

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Symbol Rate	LDPC/BCH QPSK	1		45	MSps
	LDPC/BCH 8PSK	1		45	MSps
	DVB-S QPSK	1		45	MSps
	DTV Legacy		20		MSps
Carrier Acquisition	Range		5		+/-MHz

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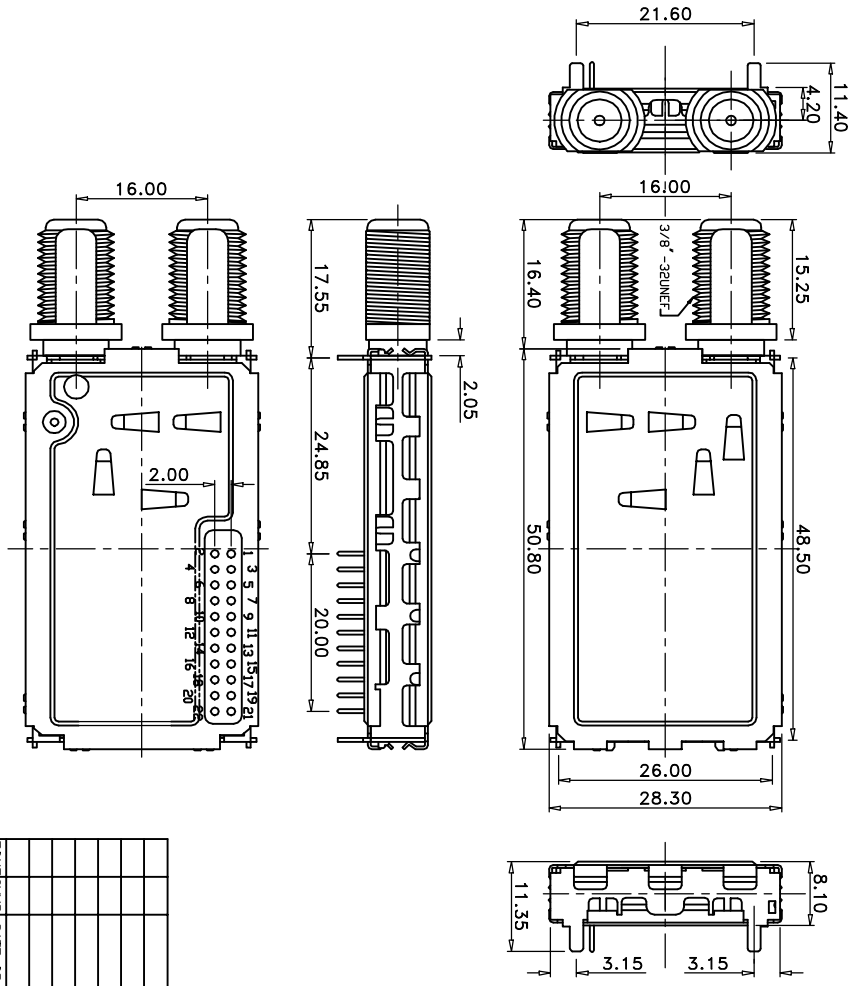
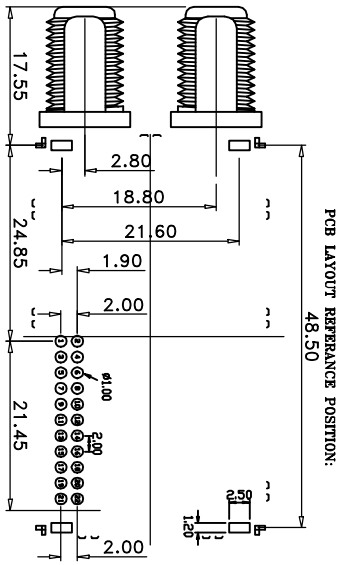


NOTE 1.TOLERANCES ARE ±0.5.
UNLESS OTHERWISE SPECIFIED.

Pin No	Connection	Pin No	Connection
1	LNBPWR	15	TS_D2
2	LNB_22K_TX	16	TS_D3
3	LNB DC	17	TS_D4
4	B1 +1.2V	18	TS_D5
5	NC	19	TS_D6
6	B2 +3.3V	20	TS_D7
7	GND	21	I2C_SCL
8	RESET	22	I2C_SDA
9	TS_ERROR		
10	TS_SYNC		
11	TS_VALID		
12	TS_CLK		
13	TS_D0		
14	TS_D1		



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