N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME25N06 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$≦200mΩ@V_{GS}=10V
- $R_{DS(ON)}$≦260mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

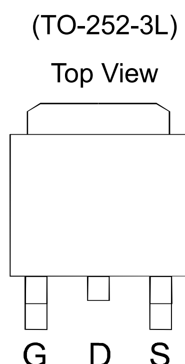
APPLICATIONS

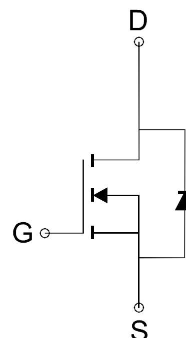
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME06N10 (Pb-free)

ME06N10-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Tc=25℃	I_D	7.2	A
	Tc=70℃		5.7	
Pulsed Drain Current		I_{DM}	28.8	A
Maximum Power Dissipation	Tc=25℃	P_D	16.6	W
	Tc=70℃		10.6	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	7.5	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250 μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250 μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 3A		160	200	mΩ
		V_{GS}=4.5V, I_D=1A		200	260	
V_{SD}	Diode Forward Voltage	I_S=6.5A, V_{GS}=0V		0.9	1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=50V, V_{GS}=5V, I_D=6.5A		8.2		nC
Qgs	Gate-Source Charge			4.3		
Qgd	Gate-Drain Charge			5.3		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.1		Ω
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		396		pF
Coss	Output Capacitance			47		
Crss	Reverse Transfer Capacitance			30		
td(on)	Turn-On Delay Time	V_{DD}=50V, R_L =50Ω V_{GEN}=10V, R_G=2.5Ω		9.6		ns
tr	Turn-On Rise Time			4.2		
td(off)	Turn-Off Delay Time			25		
tf	Turn-Off Fall Time			3.2		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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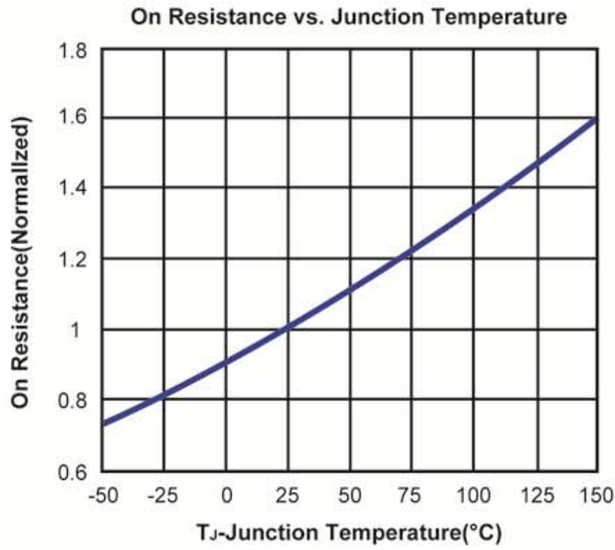
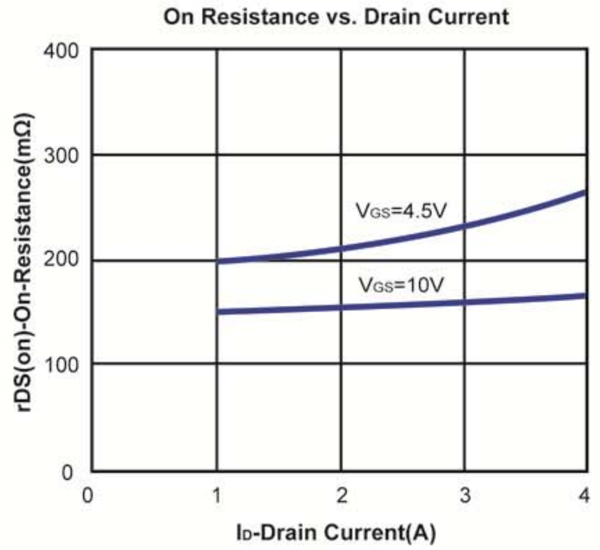
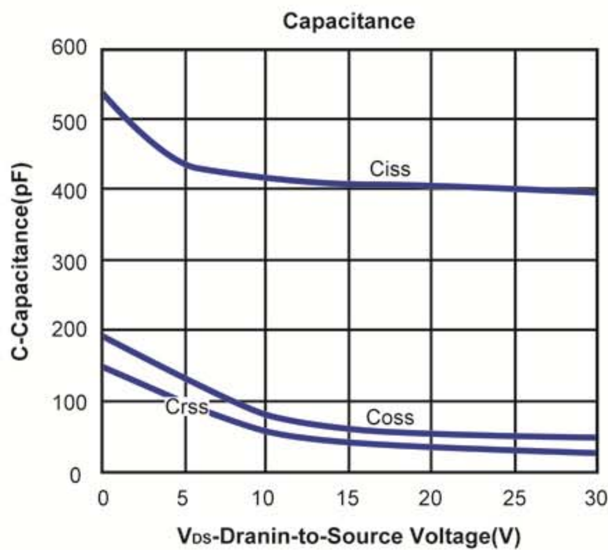
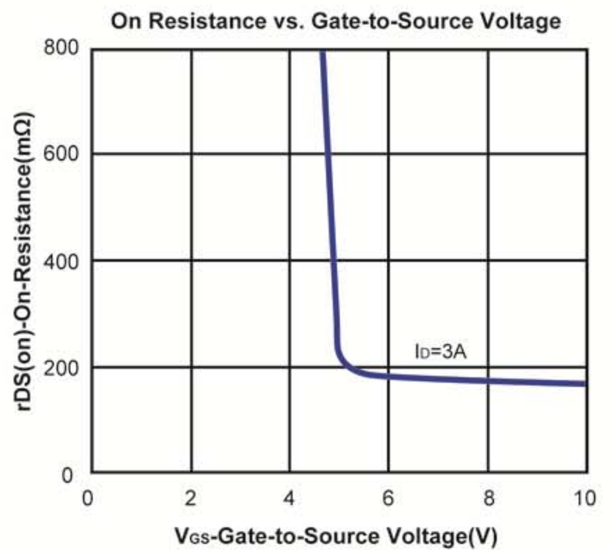
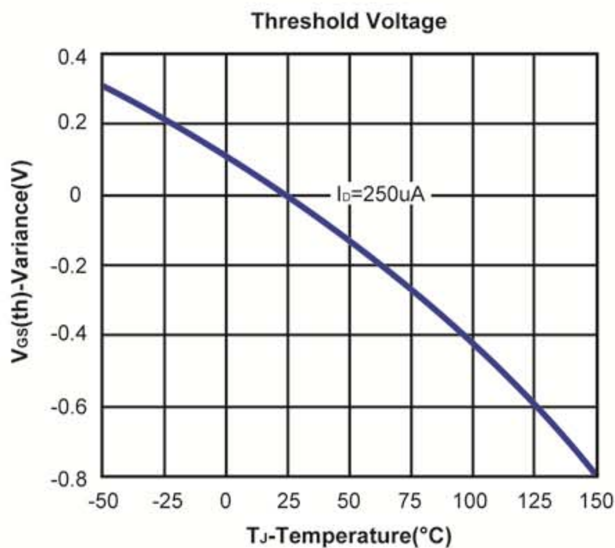
Typical Characteristics (T_J =25℃ Noted)

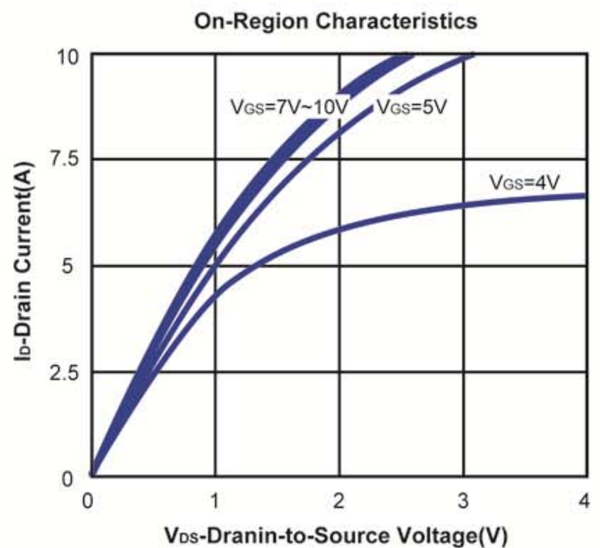












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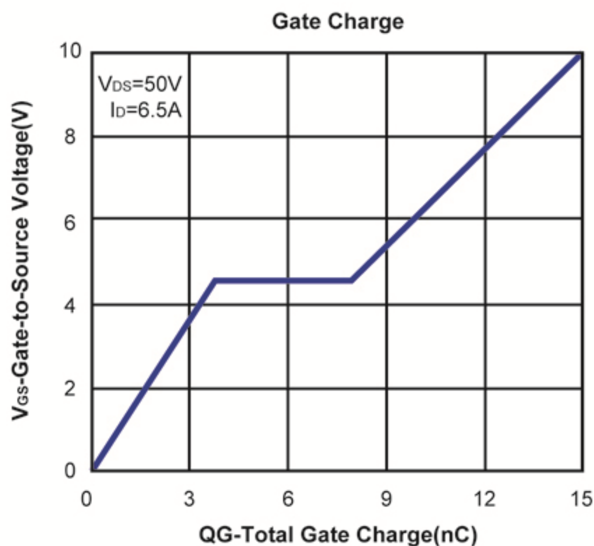
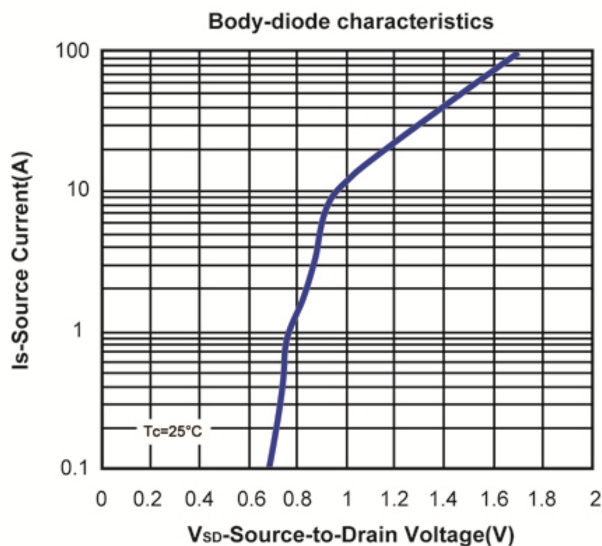
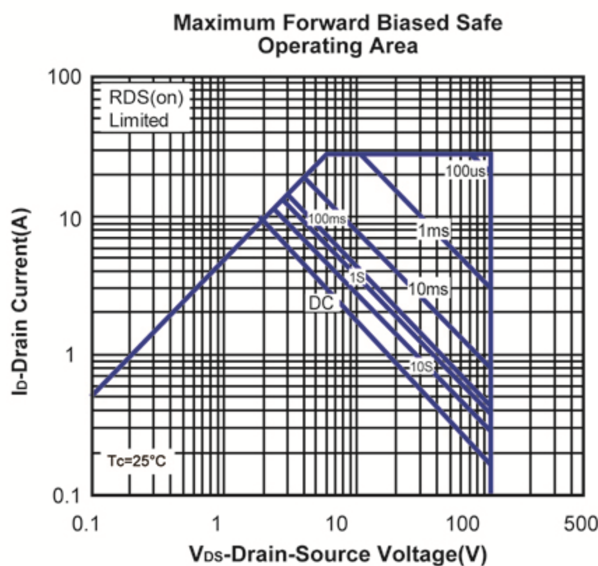
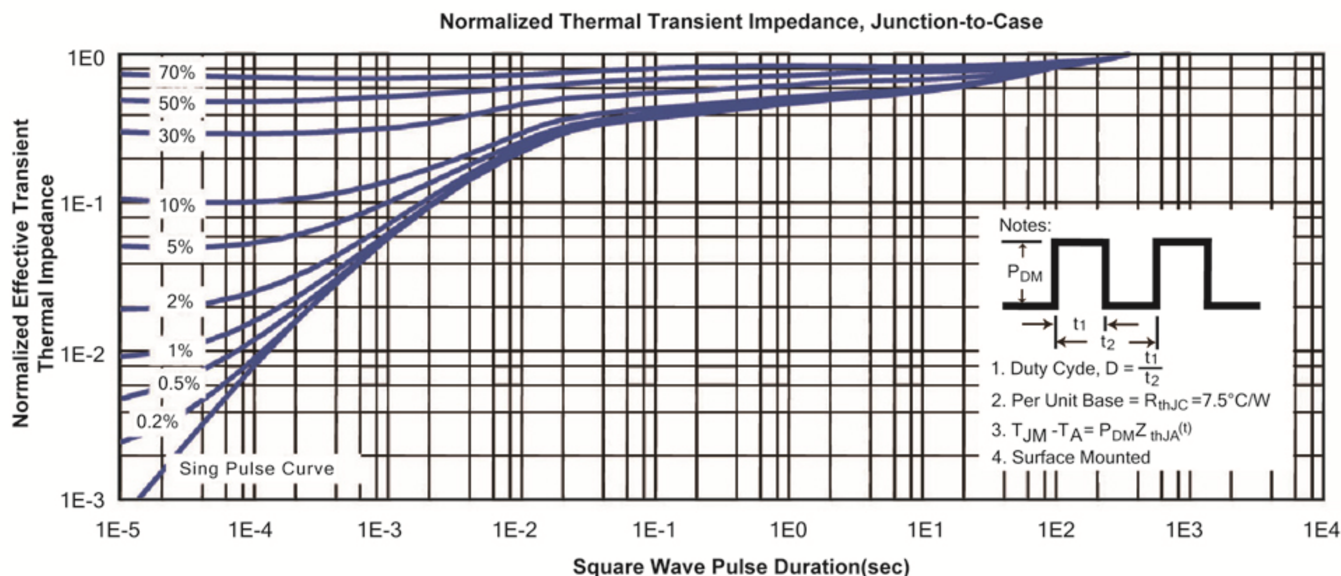
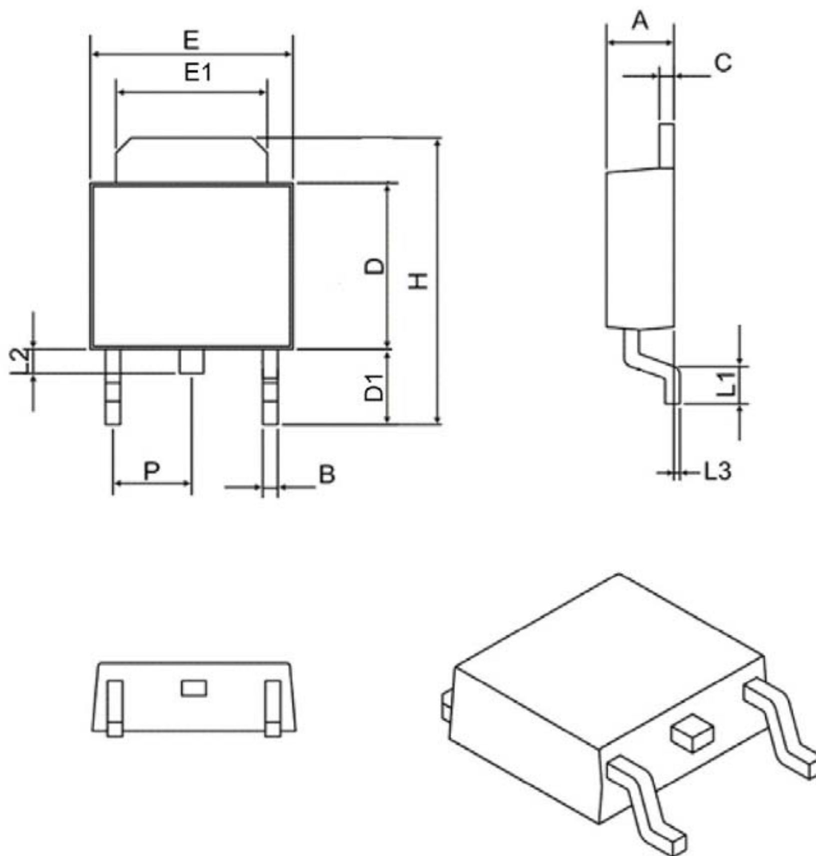








TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	