

N- Channel 200V (D-S) MOSFET

GENERAL DESCRIPTION

The ME08N20 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

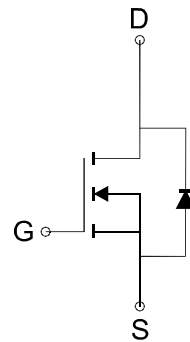
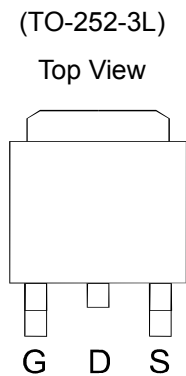
FEATURES

- $R_{DS(ON)} \leq 0.4\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- Secondary Synchronous Rectification

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME08N20 (Pb-free)

ME08N20-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter Sy		mbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS} 200		V
Gate-Source Voltage		$V_{GS} \pm 20$		V
Continuous Drain Current *	$T_c=25^\circ C$	I_D	9	A
	$T_c=70^\circ C$		7.2	
Pulsed Drain Current		I_{DM} 36		A
Maximum Power Dissipation	$T_c=25^\circ C$	P_D	74.9	W
	$T_c=70^\circ C$		47.9	
Operating Junction Temperature		T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case*		$R_{\theta JC}$ 1.67		$^\circ C/W$

* Notes: The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_c = 25°C Unless Otherwise Specified)

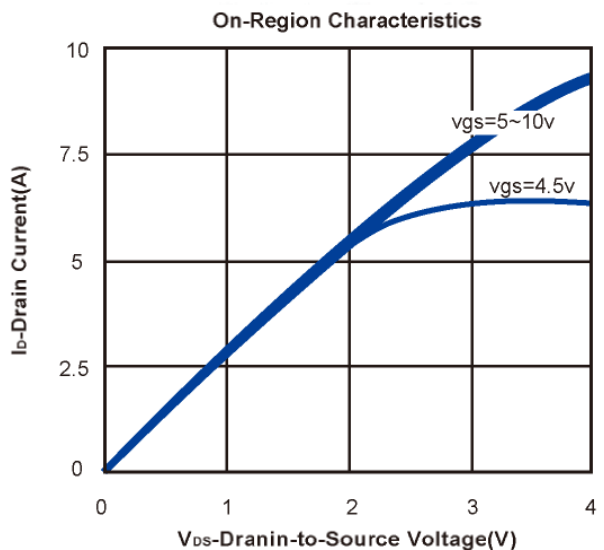
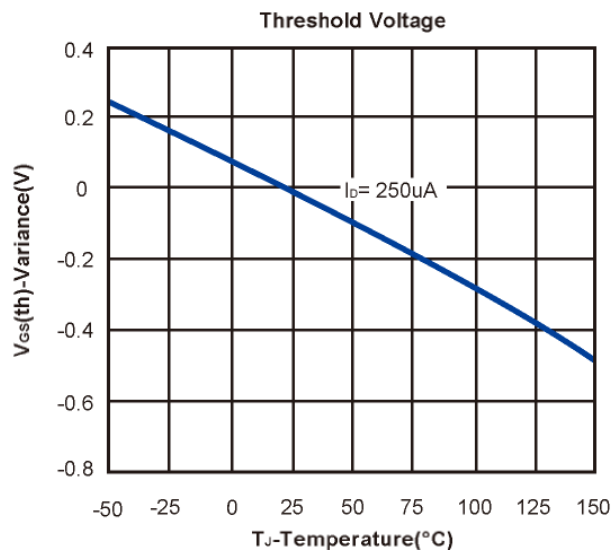
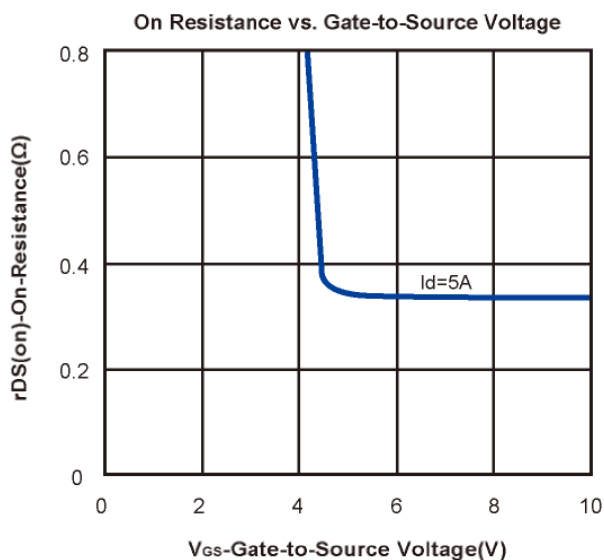
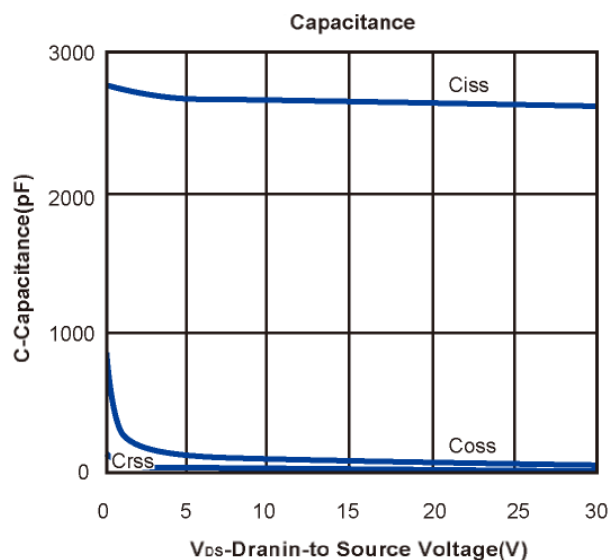
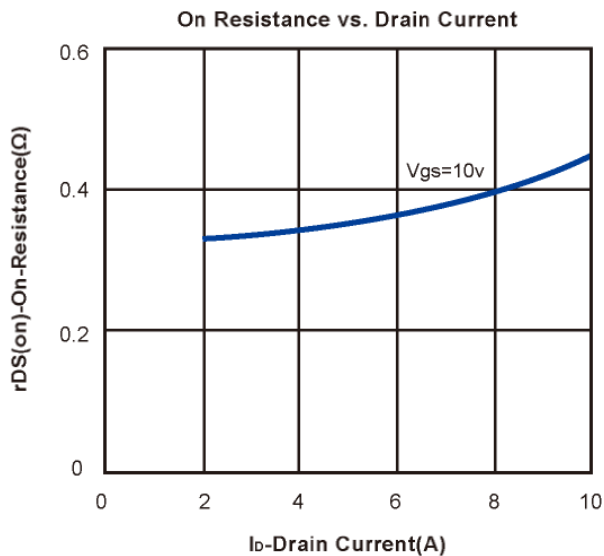
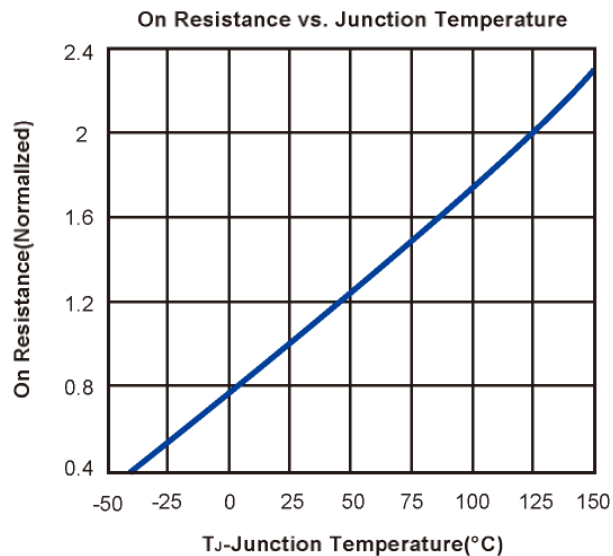
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA 200				V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA 2			4	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =200V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 5A		0.35	0.40	Ω
V _{SD}	Diode Forward Voltage	I _S =9A, V _{GS} =0V			1.5	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =160V, V _{GS} =10V, I _D =9A		51.7		nc
Q _{gs}	Gate-Source Charge			12.7		
Q _{gd}	Gate-Drain Charge			16.3		
C _{iss}	Input capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		2610		pF
C _{oss}	Output Capacitance			68		
C _{rss}	Reverse Transfer Capacitance			21		
t _{d(on)}	Turn-On Delay Time	V _{DS} =160V, V _{GS} =10V, R _G =4.7Ω, R _L =17.7Ω		26.9		ns
t _r	Turn-On Rise Time			37.2		
t _{d(off)}	Turn-Off Delay Time			63.5		
t _f	Turn-Off Fall Time			43.8		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

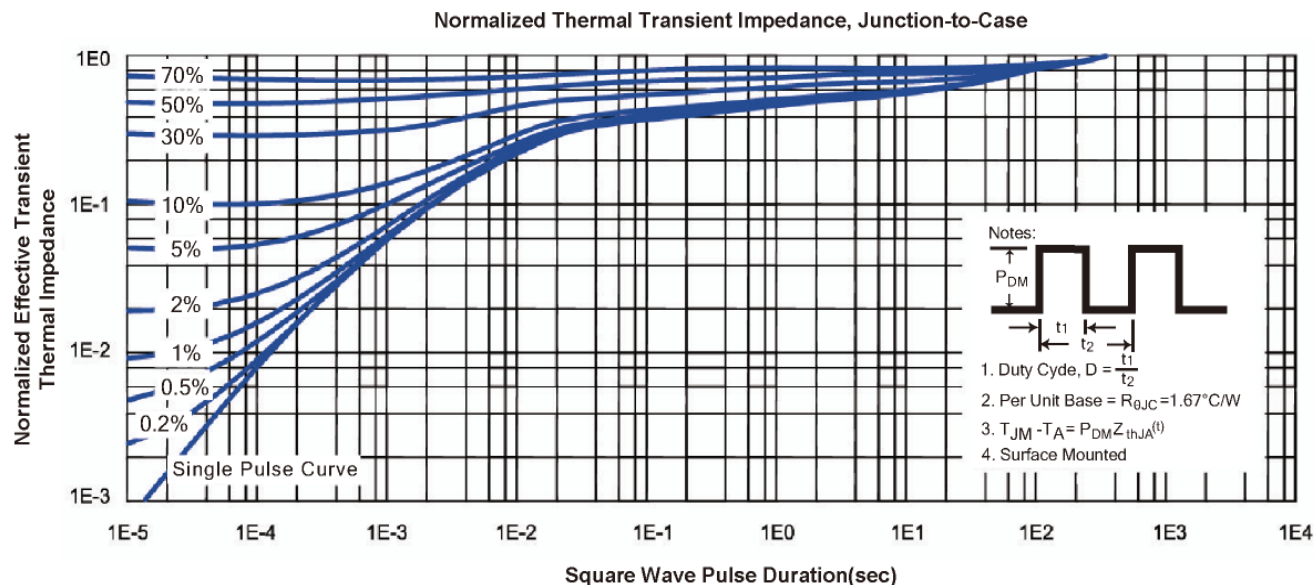
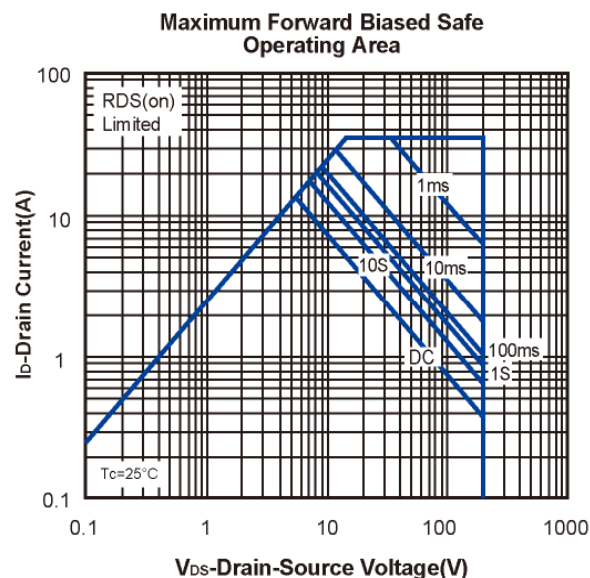
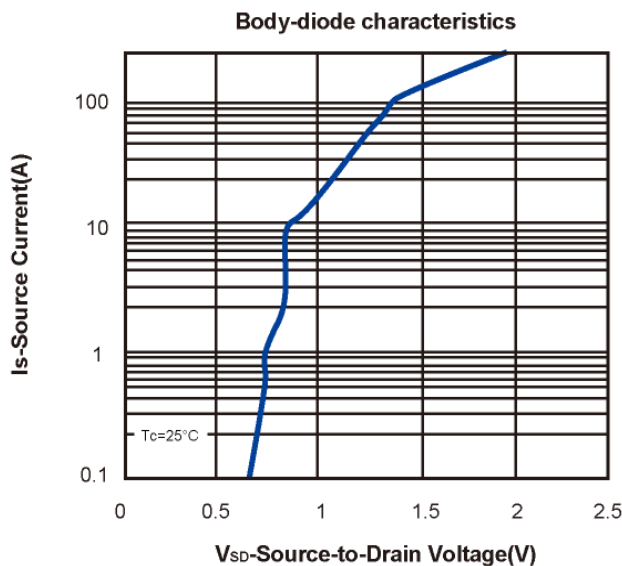
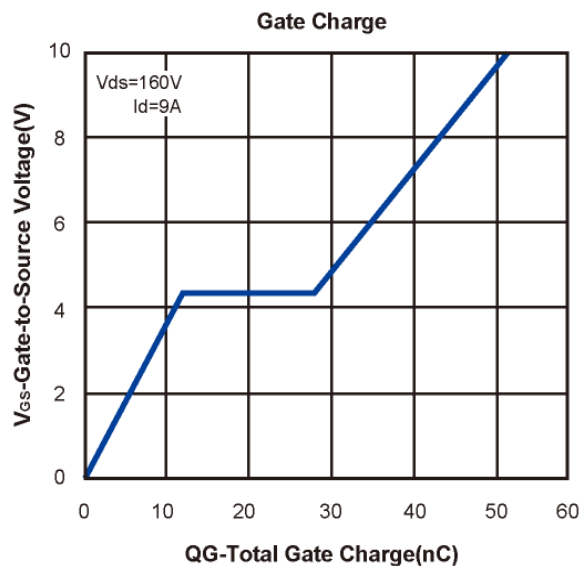
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Typical Characteristics (T_J = 25°C Noted)

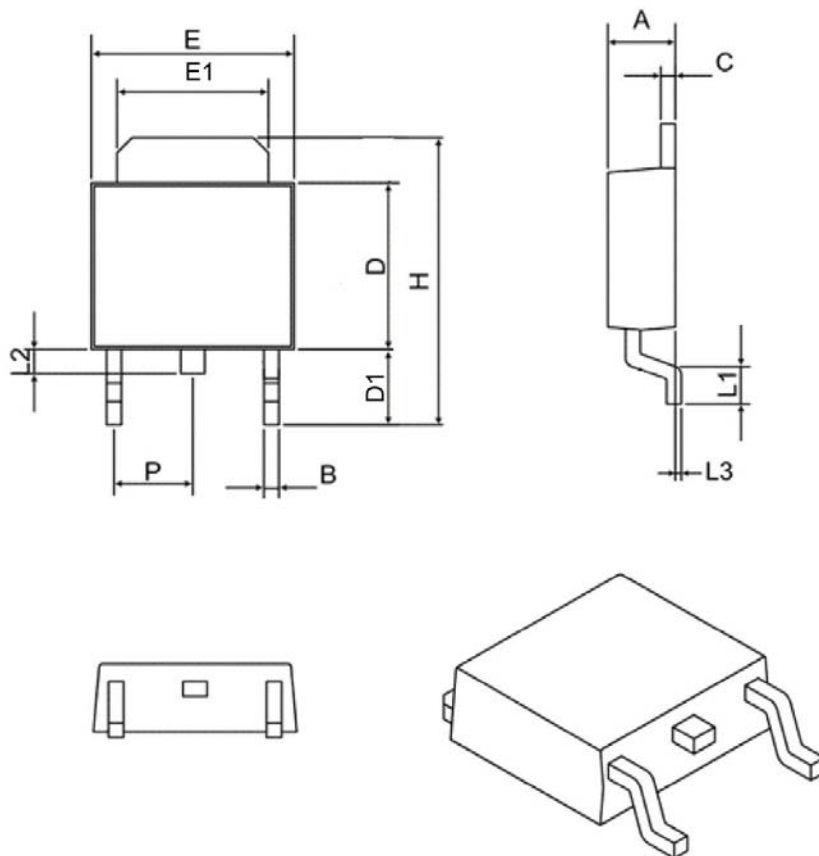


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TO-252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	