ME12N04/ME12N04-G

N- Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME12N04 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$=28mΩ@V_{GS}=10V (N-Ch)
- $R_{DS(ON)}$=52mΩ@V_{GS}=4.5V (N-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

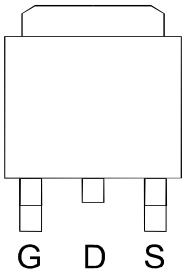
APPLICATIONS

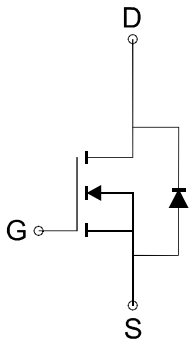
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME12N04 (Pb-free)

ME12N04-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current*	T_C=25℃	I_D	22	A
	T_C=70℃		18	
Pulsed Drain Current		I_{DM}	80	A
Maximum Power Dissipation	T_C=25℃	P_D	25	W
	T_C=70℃		16	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	42	℃/W
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	5	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N- Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

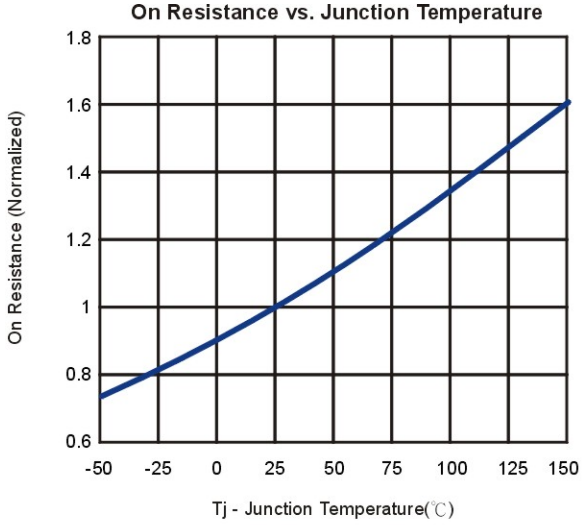
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	1.9	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
		V_{DS}=40V, V_{GS}=0V,T_J=55℃			10	
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 12A		22	28	mΩ
		V_{GS}=4.5V, I_D= 6A		40	52	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.78	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=4.5V, I_D=12A		8		nC
Qgs	Gate-Source Charge			4		
Qgd	Gate-Drain Charge			4		
Rg	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.7		Ω
Ciss	Input capacitance	V_{DS}=20V, V_{GS}=0V, F=1MHz		560		pF
Coss	Output Capacitance			72		
Crss	Reverse Transfer Capacitance			18		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω		11		ns
t_r	Turn-On Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			37		
t_f	Turn-On Fall Time			3.5		

Notes:a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

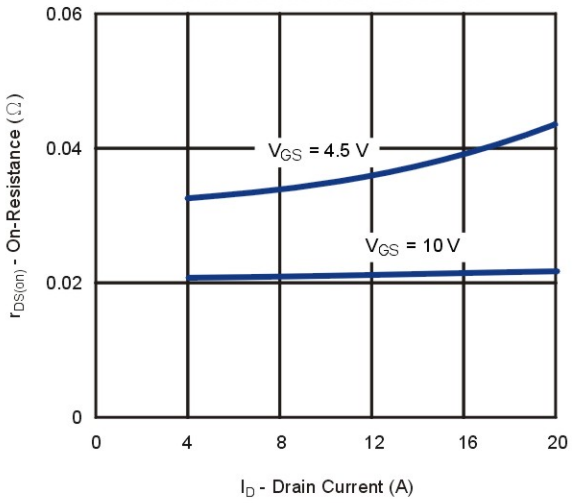
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J =25℃ Noted)

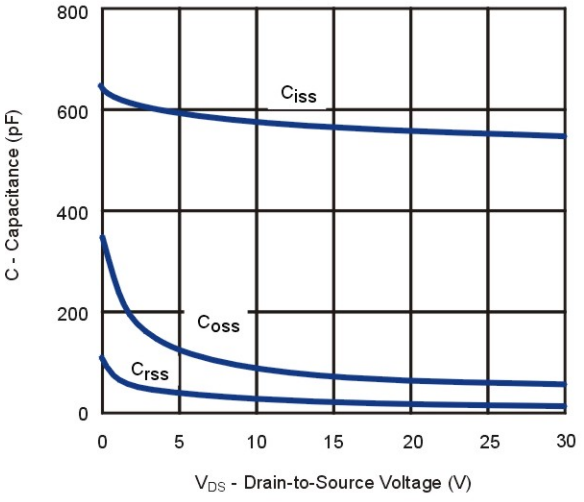
On Resistance vs. Junction Temperature



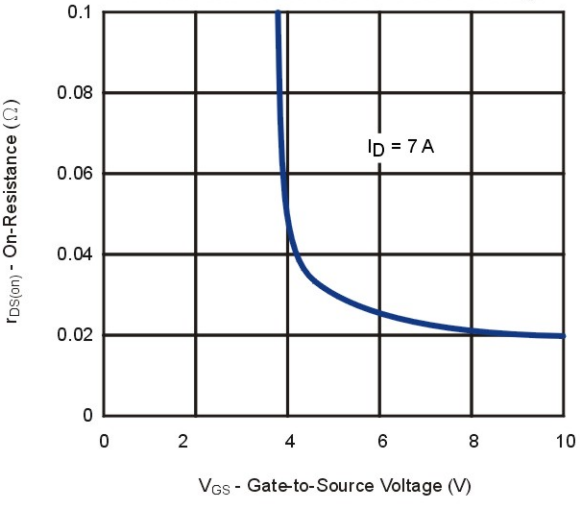
On-Resistance vs. Drain Current



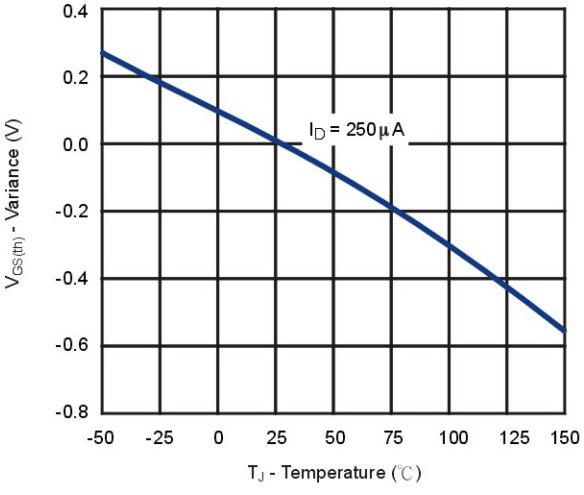
Capacitance



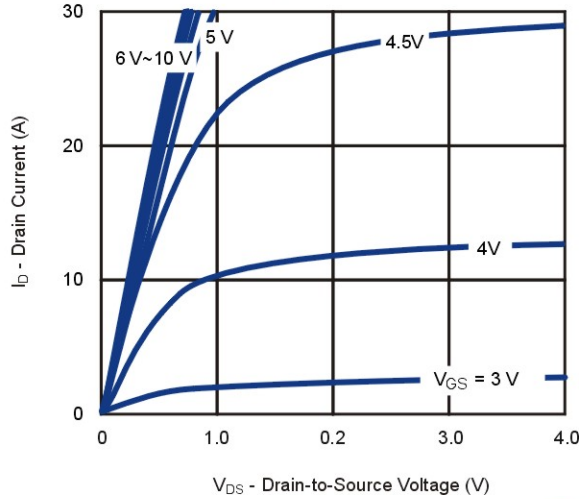
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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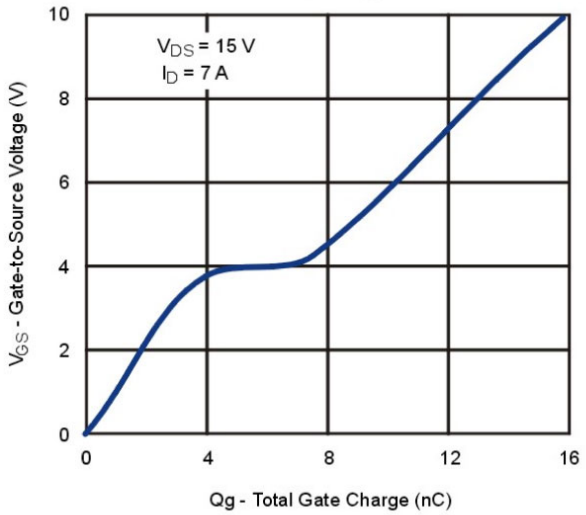
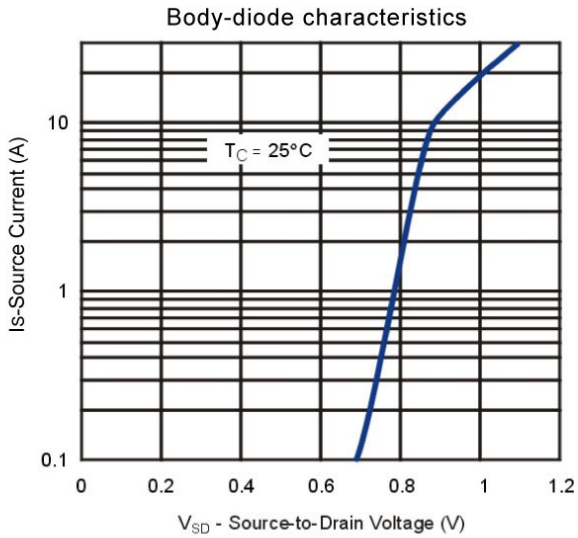
Typical Characteristics (T_J =25℃ Noted)

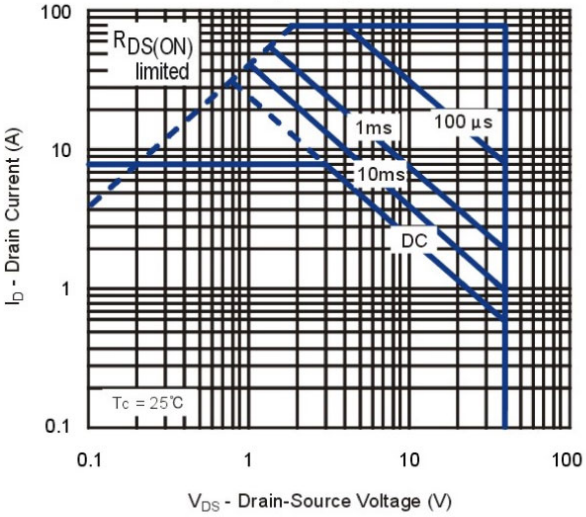
Gate Charge



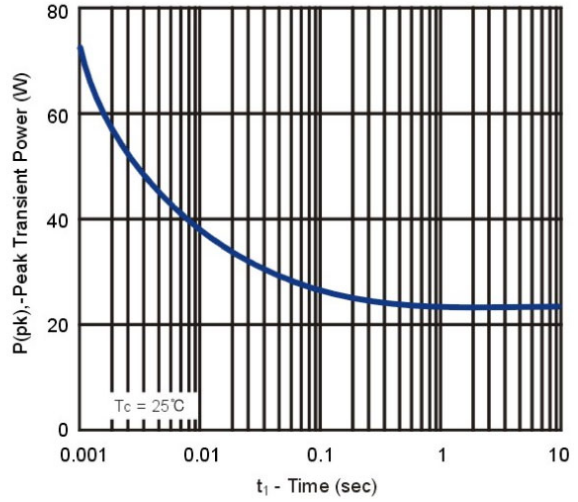
Body-diode characteristics



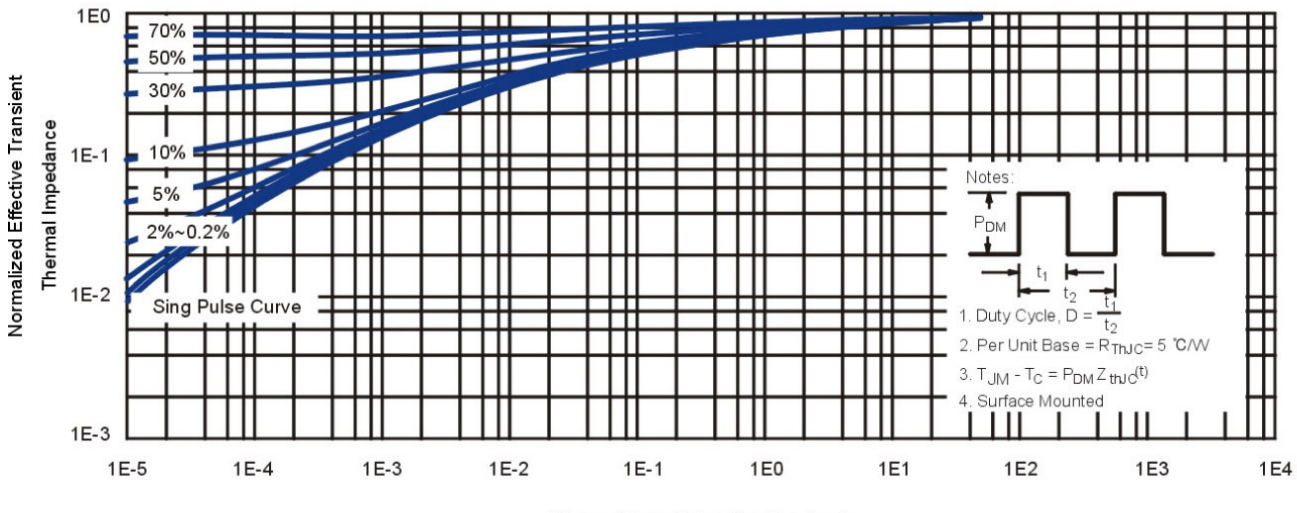
Maximum Forward Biased Safe Operating Area



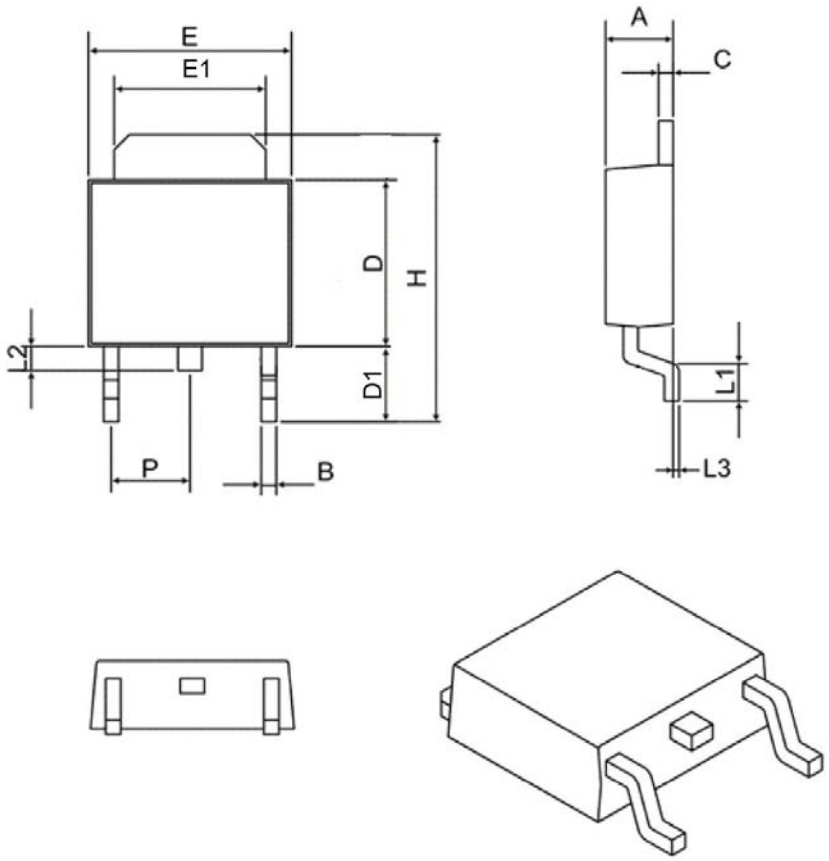
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Case



TO-252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	