P-Channel 20V (D-S) MOSFET

GENERAL DESCRIPTION

The ME1303S is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦95mΩ@V_{GS}=-4.5V
- $R_{DS(ON)}$ ≦120mΩ@V_{GS}=-2.5V
- $R_{DS(ON)}$ ≦180mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

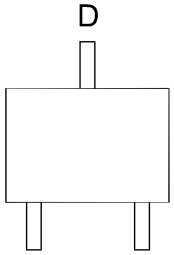
APPLICATIONS

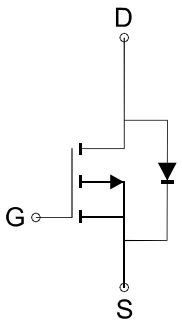
- Power Management in Note book
- Portable Equipment
- Load Switch
- DSC

PIN CONFIGURATION

(SOT-23)

Top View





P-Channel MOSFET

Ordering Information: ME1303S (Pb-free)

ME1303S-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current*	T_A=25℃	I_D	-2.6	A
	T_A=70℃		-2.1	
Pulsed Drain Current		I_{DM}	-10	A
Maximum Power Dissipation	T_A=25℃	P_D	1	W
	T_A=70℃		0.7	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	120	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.4		-0.9	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D= -3.4A		76	95	mΩ
		V_{GS}=-2.5V, I_D= -2.4A		97	120	
		V_{GS}=-1.8V, I_D= -1.7A		140	180	
V_{SD}	Diode Forward Voltage	I_S=-1.5A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-6V, V_{GS}=-4.5V, I_D=-2.8A		10		nC
Qgs	Gate-Source Charge			2.4		
Qgd	Gate-Drain Charge			2.2		
Ciss	Input Capacitance	V_{DS}=-6V, V_{GS}=0V, f=1MHz		1100		pF
Coss	Output Capacitance			200		
Crss	Reverse Transfer Capacitance			40		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L=15Ω V_{GEN}=-10V,R_G=6Ω		32		ns
t_r	Turn-On Rise Time			18		
$t_{d(off)}$	Turn-Off Delay Time			57		
t_f	Turn-On Fall Time			4.5		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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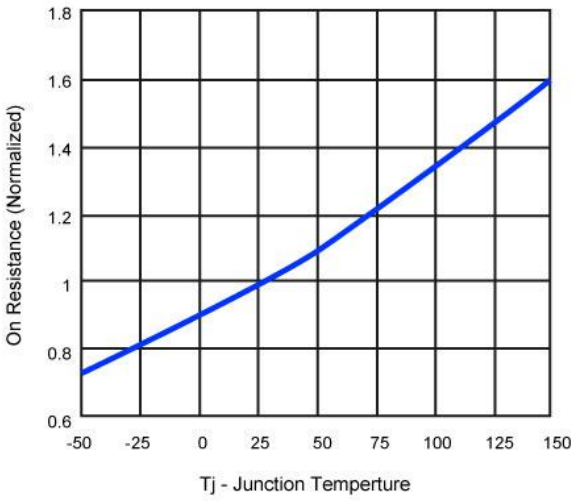
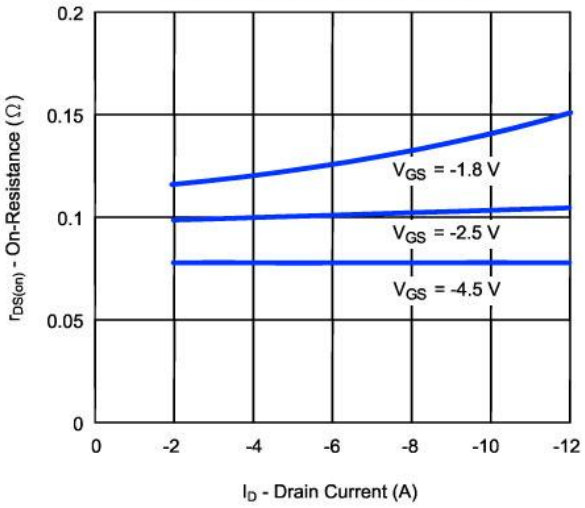
Typical Characteristics (T_J =25℃ Noted)

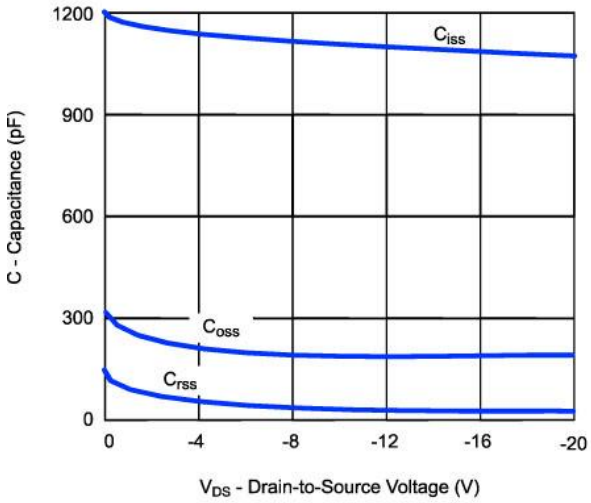
On Resistance vs. Junction Temperture



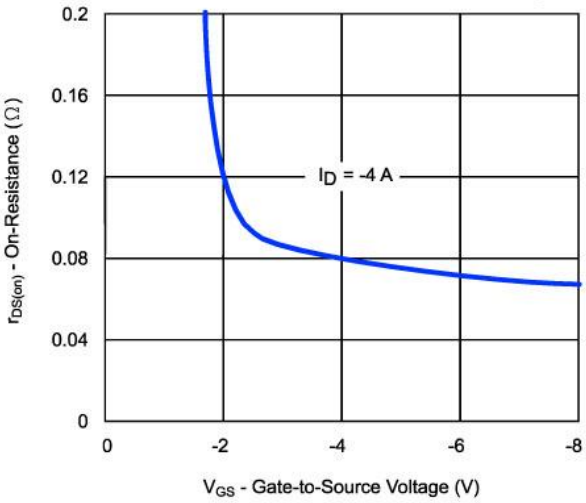
On-Resistance vs. Drain Current



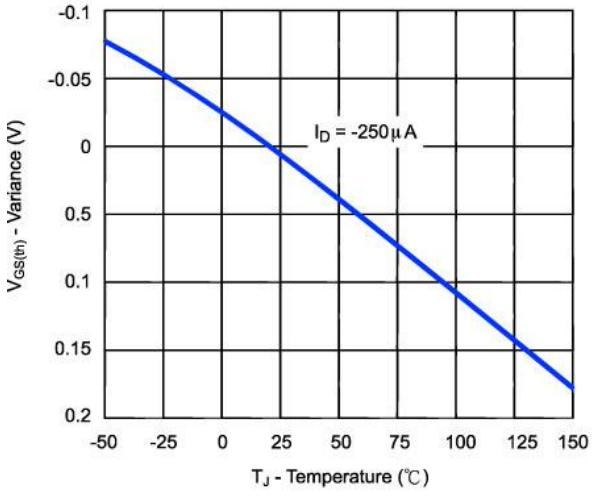
Capacitance



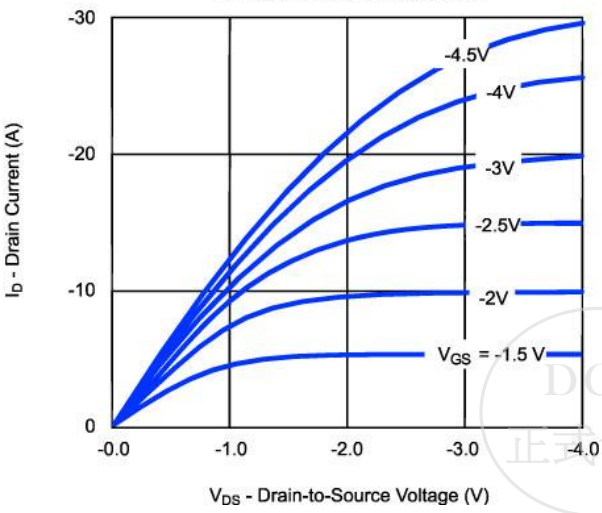
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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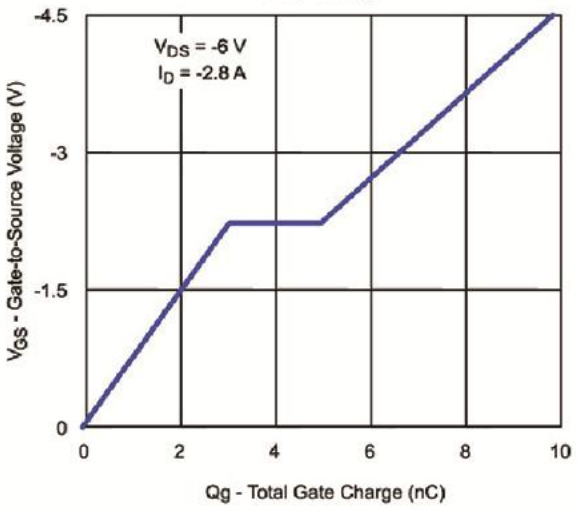
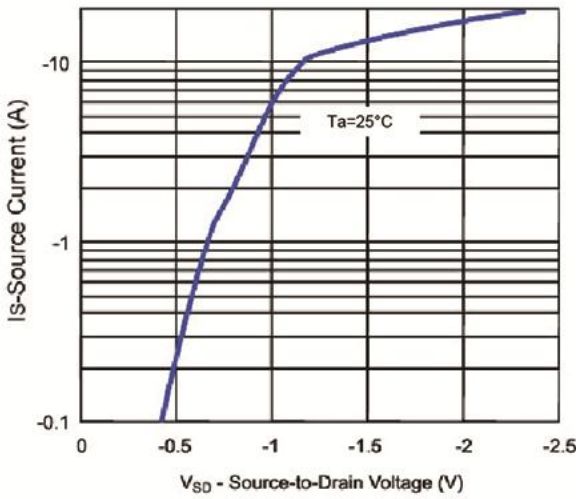
Typical Characteristics (T_J =25℃ Noted)

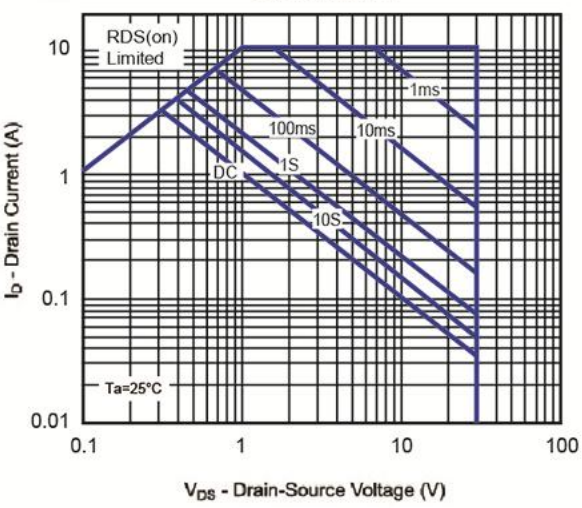
Gate Charge



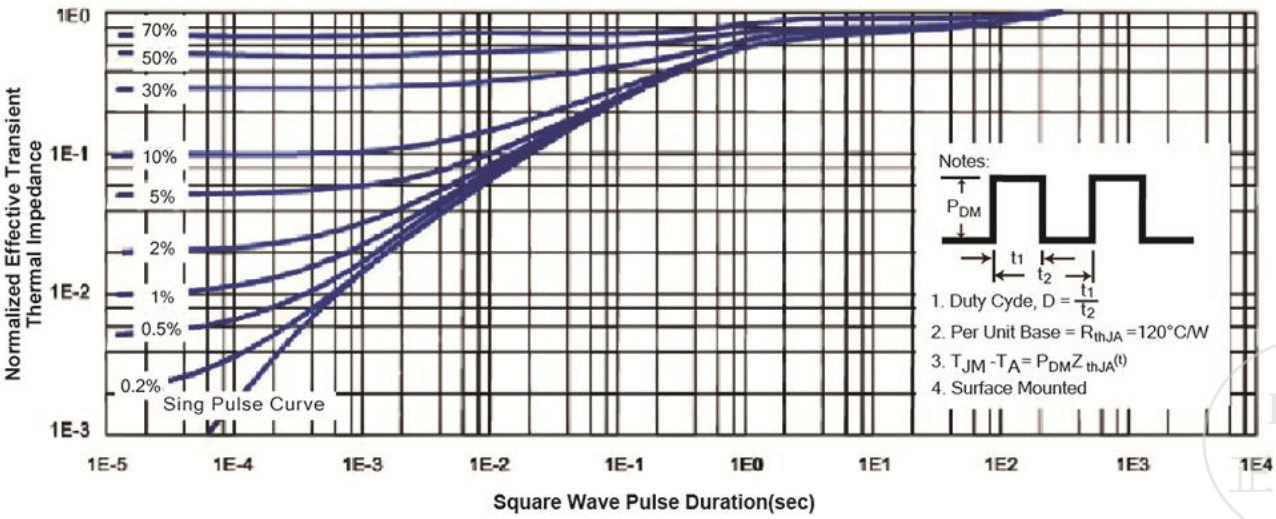
Body-diode characteristics



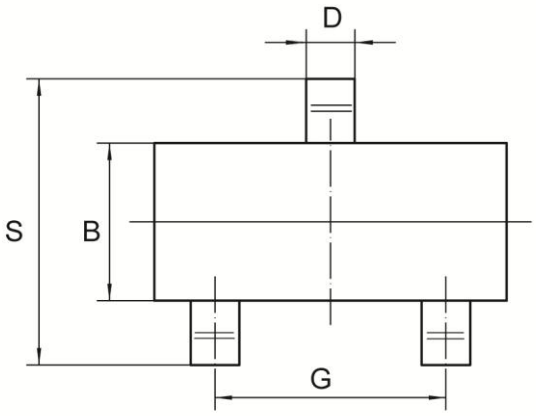
Maximum Forward Biased Safe Operating Area

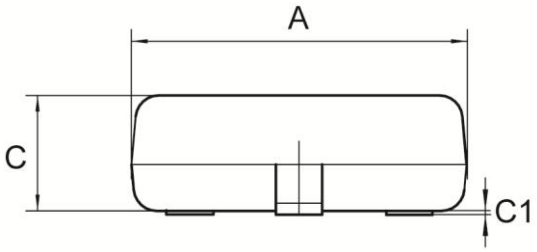


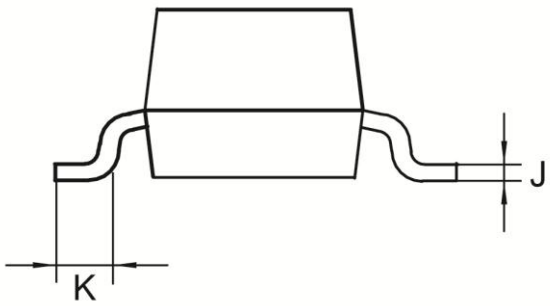
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







Symbol	MILLIMETERS	
	MIN	MAX
A	2.8	3.0
B	1.2	1.4
C	0.9	1.1
C1	-	0.1
D	0.3	0.5
G	1.90 REF	
J	0.05	0.15
K	0.2	-
S	2.2	2.6