

N-Channel 20-V (D-S) MOSFET

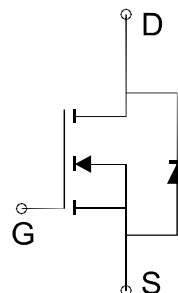
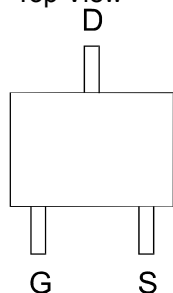
GENERAL DESCRIPTION

The ME1304AT3 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(SC70-3L)

Top View



FEATURES

- $R_{DS(ON)} \leq 65 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$
- $R_{DS(ON)} \leq 80 \text{ m}\Omega$ @ $V_{GS}=2.5\text{V}$
- $R_{DS(ON)} \leq 95 \text{ m}\Omega$ @ $V_{GS}=1.8\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Load Switch
- DSC

Ordering Information: ME1304AT3 (Pb-free)

ME1304AT3-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current($T_J=150^\circ\text{C}$)*	$T_A=25^\circ\text{C}$	I_D	1.8	A
	$T_A=70^\circ\text{C}$		1.5	
Pulsed Drain Current		I_{DM}	7	A
Maximum Power Dissipation*	$T_A=25^\circ\text{C}$	P_D	0.4	W
	$T_A=70^\circ\text{C}$		0.2	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	360	$^\circ\text{C/W}$

*The device mounted on 1in² FR4 board with 2 oz copper, $t \leq 10\text{S}$.



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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.4		1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±12V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =4.5V, I _D = 4.0A		52	65	mΩ
		V _{GS} =2.5V, I _D = 3.4A		60	80	
		V _{GS} =1.8V, I _D = 2.8A		75	95	
V _{SD}	Diode Forward Voltage	I _S =1.7A, V _{GS} =0V		0.8	1.2	V
DYNAMIC						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHZ		370		pF
C _{oss}	Output Capacitance			90		
C _{rss}	Reverse Transfer Capacitance			25		
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =2.8A		8.7		nC
Q _{gs}	Gate-Source Charge			1.5		
Q _{gd}	Gate-Drain Charge			3.5		
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =6Ω I _D =1.0A, V _{GEN} =10V R _G =6Ω		7.5		ns
t _r	Turn-On Rise Time			18		
t _{d(off)}	Turn-Off Delay Time			40		
t _f	Turn-Off Fall Time			3.5		

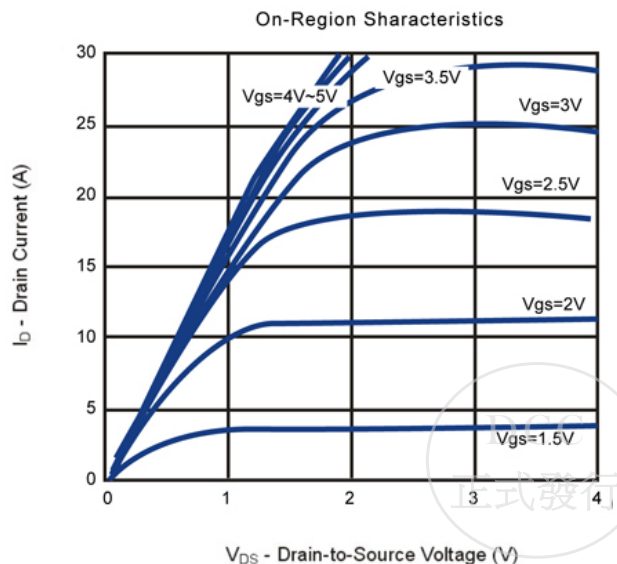
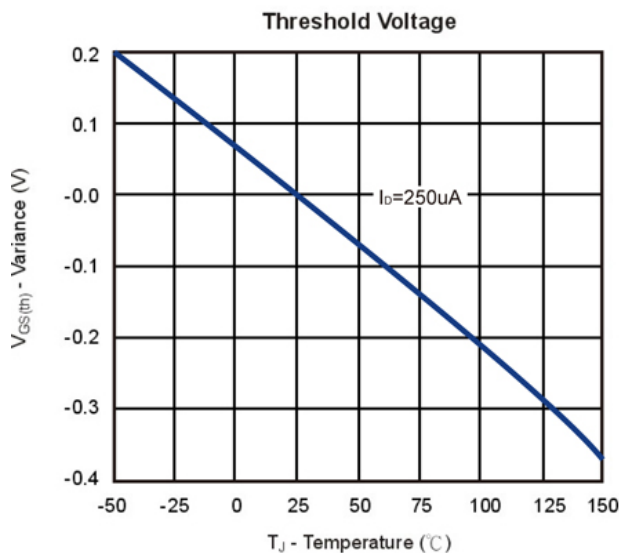
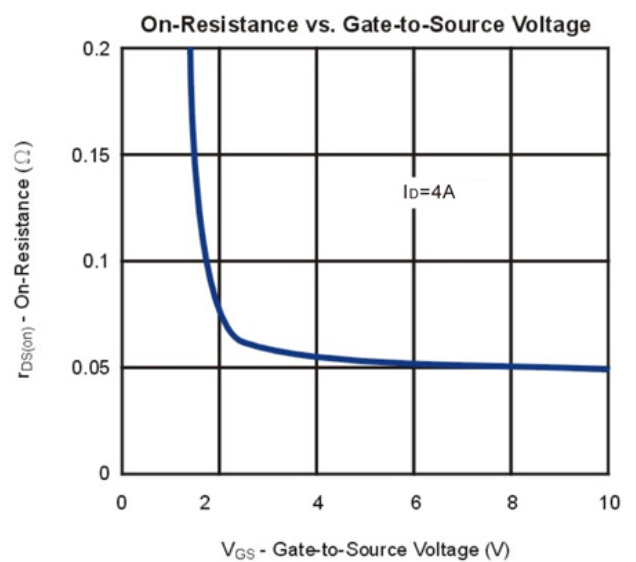
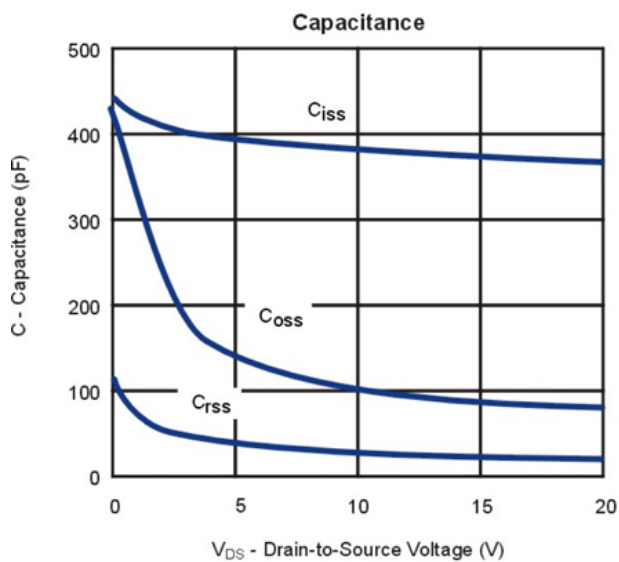
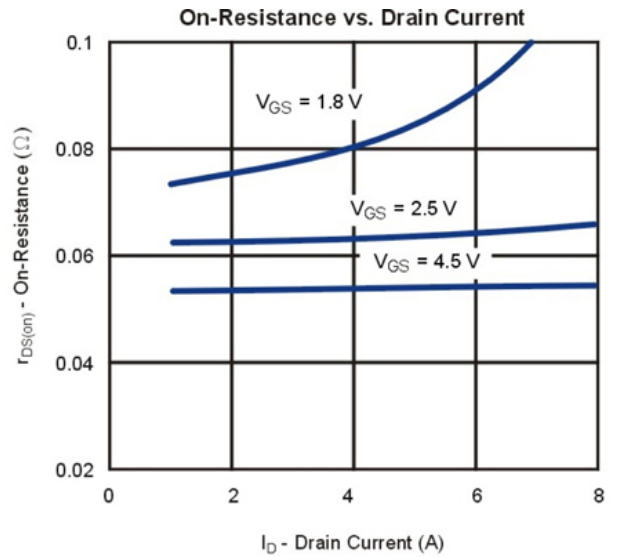
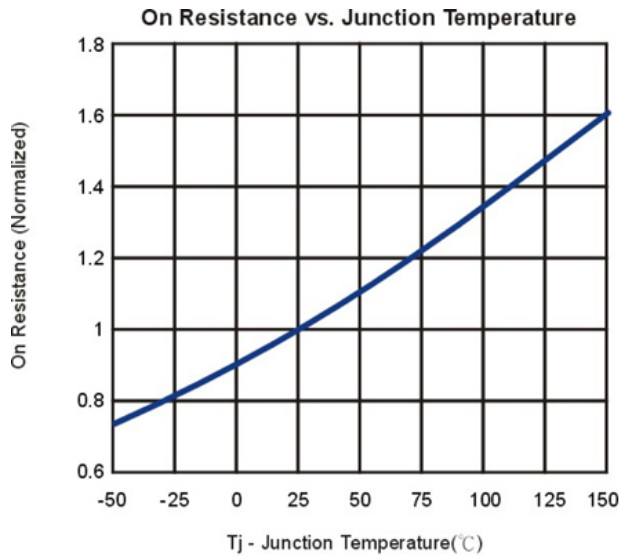
Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



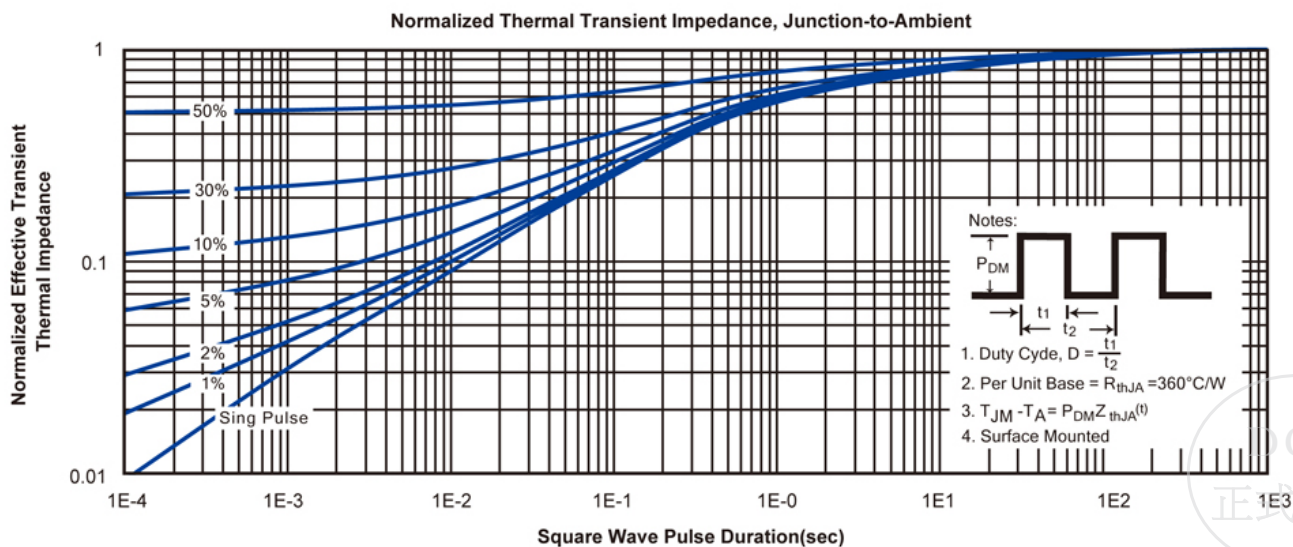
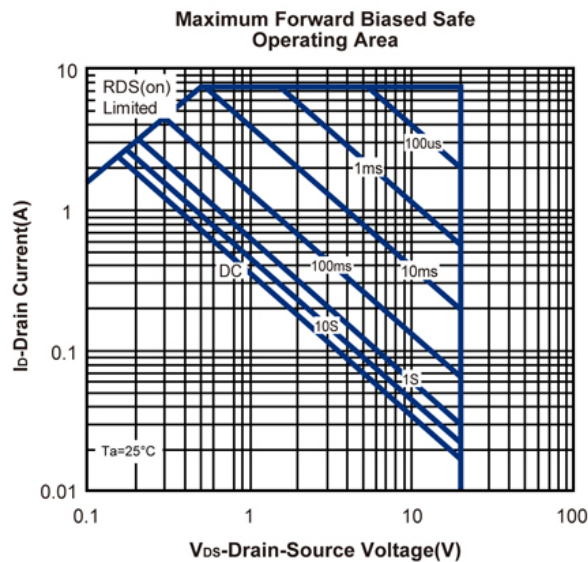
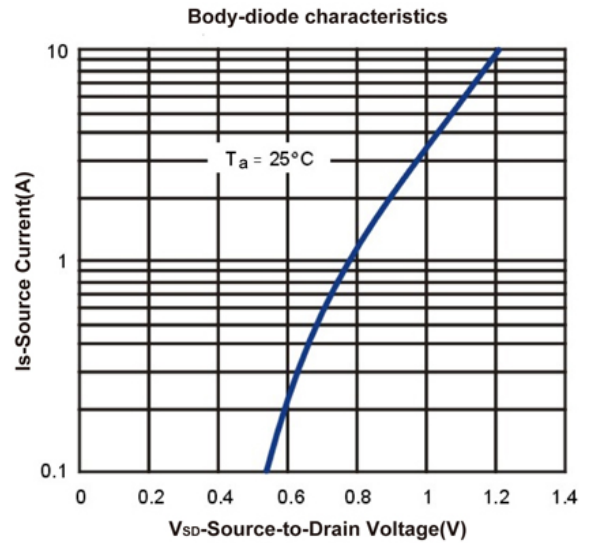
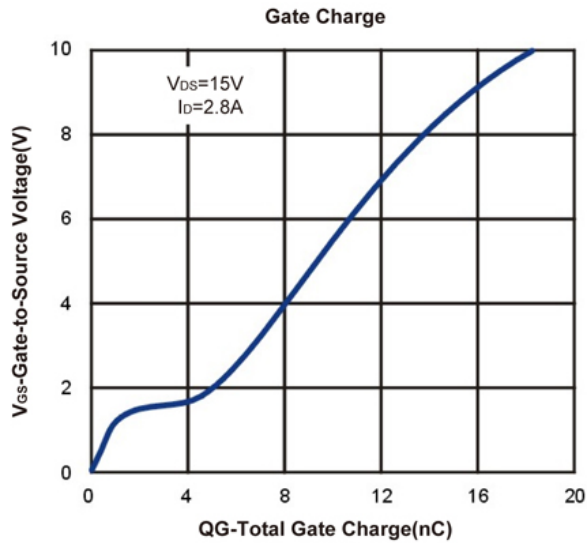
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Typical Characteristics (T_J = 25°C Noted)

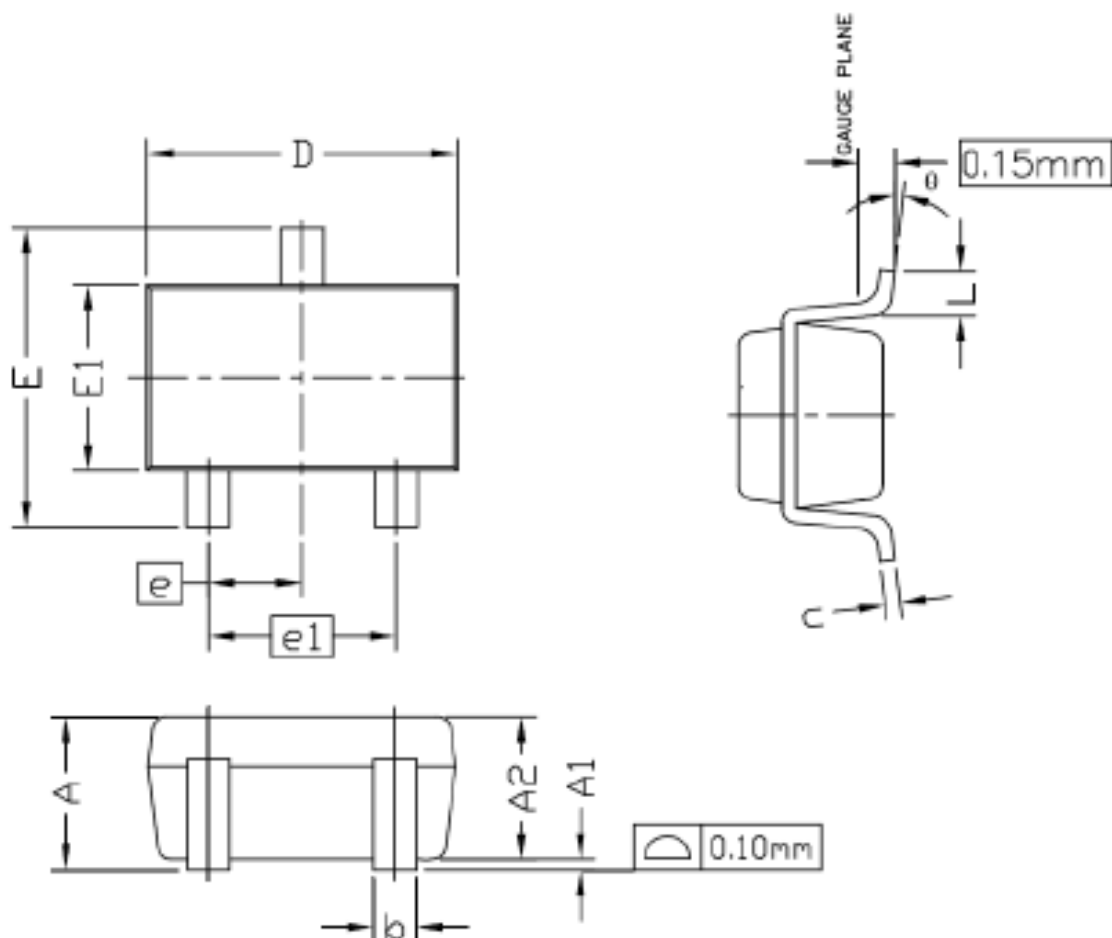


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Typical Characteristics (T_J = 25°C Noted)



SC-70-3L(SOT-323) Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.20	0.40
c	0.08	0.22
D	1.80	2.20
E	1.80	2.45
e	0.65 BSC	
e1	1.30 BSC	
E1	1.10	1.40
L	0.20	0.46
θ	0°	8°

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