

N- Channel 100V (D-S) MOSFET

GENERAL DESCRIPTION

The ME13N10A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

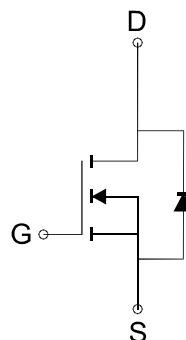
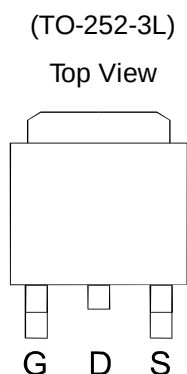
FEATURES

- $R_{DS(ON)} \leq 145m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- DC/DC Converter
- Load Switch
- LCD/ LED Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME13N10A (Pb-free)

ME13N10A-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	Tc=25°C	I_D	11.3	A
	Tc=70°C		9.0	
Pulsed Drain Current		I_{DM}	45.4	A
Maximum Power Dissipation	Tc=25°C	P_D	29.9	W
	Tc=70°C		19.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	4.17	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (Tc =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = $\pm$ 20V			$\pm$ 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 5A			145	m Ω
V _{SD}	Diode Forward Voltage	I _S =9A, V _{GS} =0V			1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _D =3A		16.4		nC
Q _{gs}	Gate-Source Charge			3.8		
Q _{gd}	Gate-Drain Charge			3.5		
C _{iss}	Input capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		524		pF
C _{oss}	Output Capacitance			55		
C _{rss}	Reverse Transfer Capacitance			32		
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, R _L =15 Ω V _{GS} =10V, R _{GEN} =2.5 Ω		11.7		ns
t _r	Turn-On Rise Time			10.9		
t _{d(off)}	Turn-Off Delay Time			27.3		
t _f	Turn-Off Fall Time			2.6		

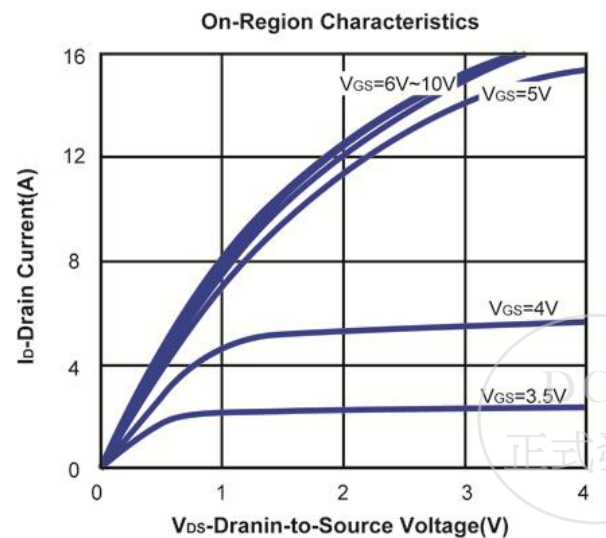
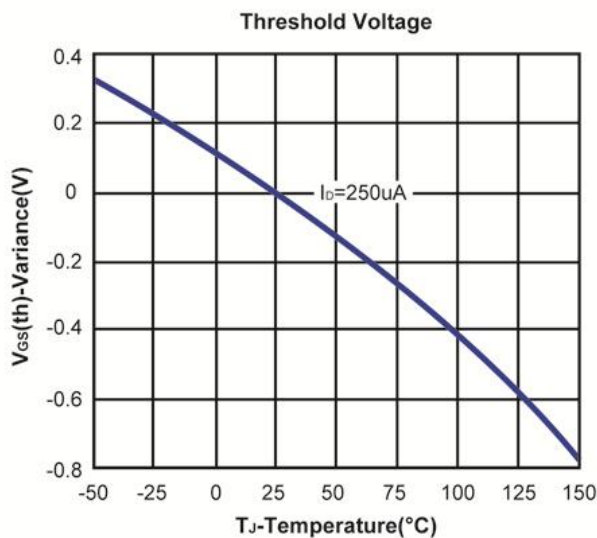
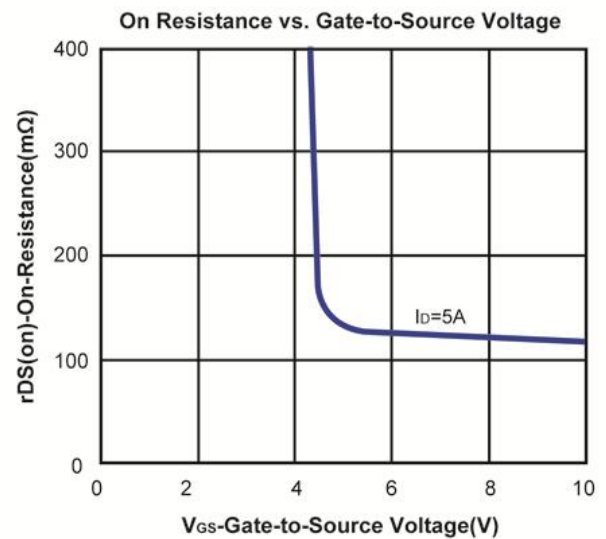
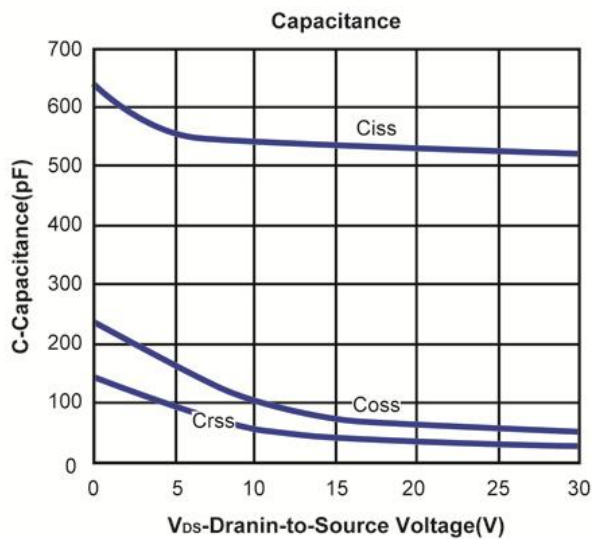
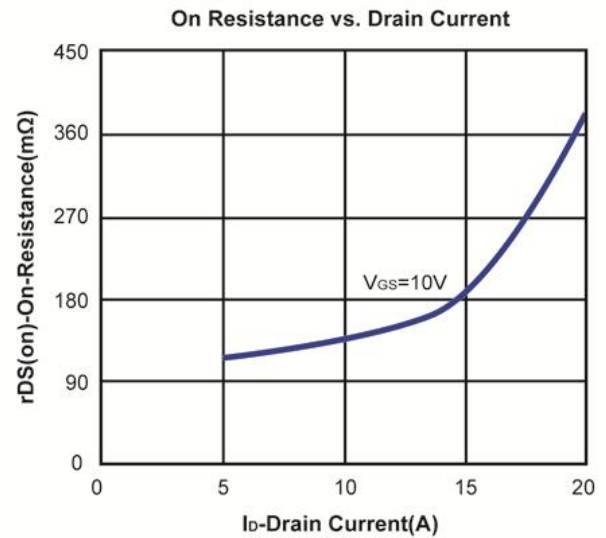
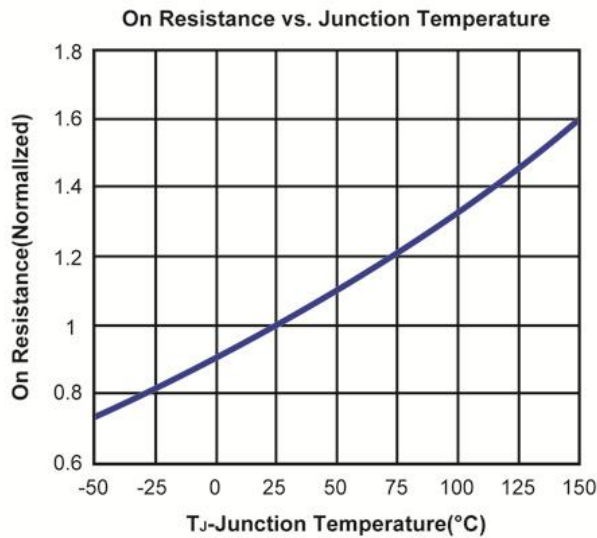
Notes: a. Pulse test: pulse width $\leq$ 300us, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



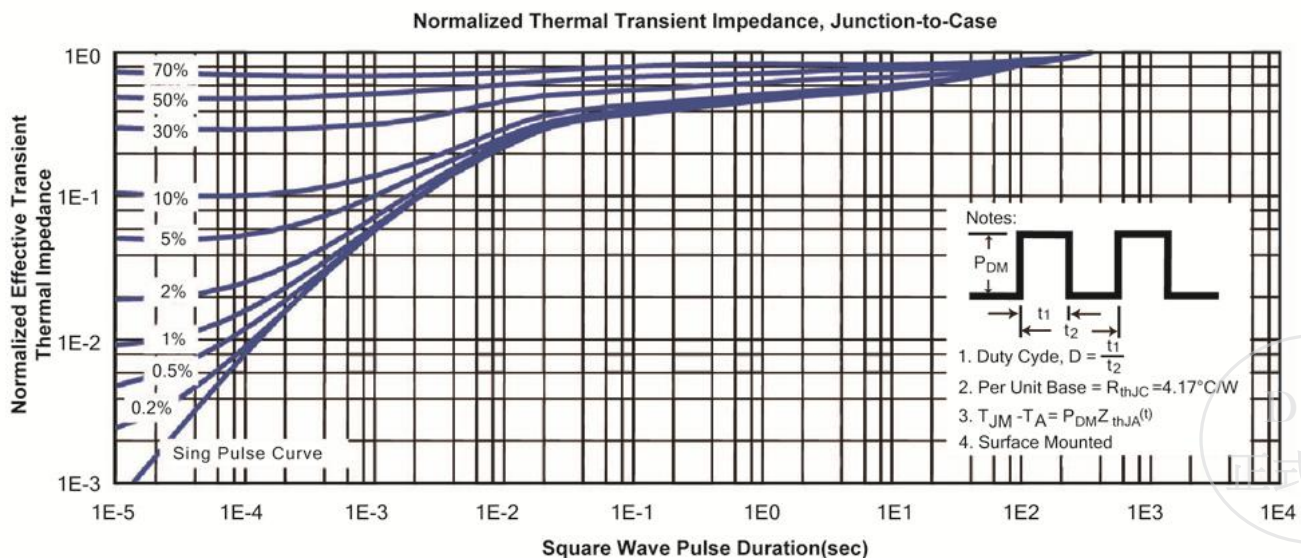
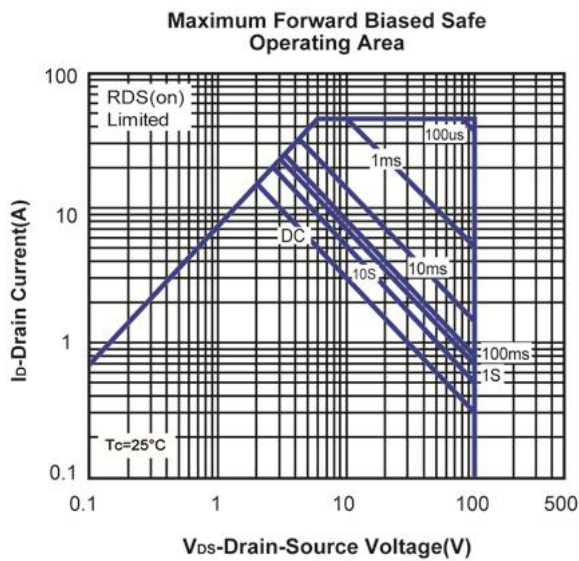
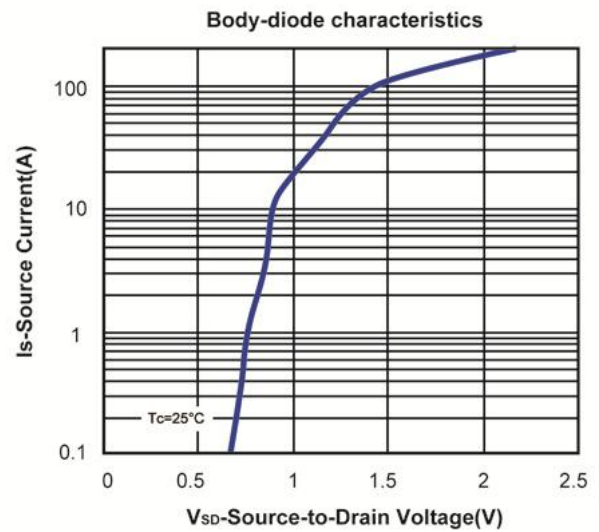
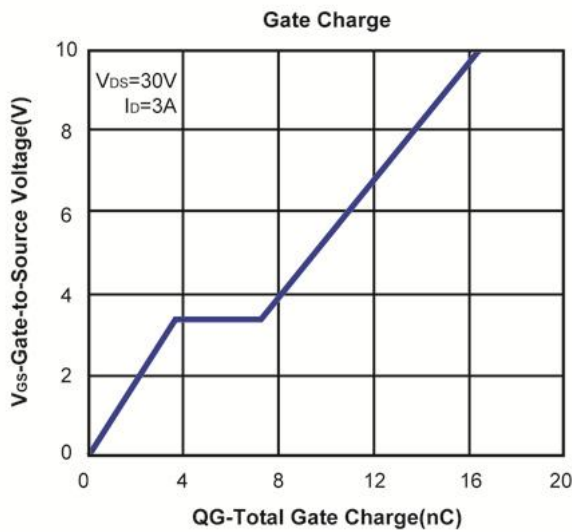
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Typical Characteristics (T_J =25°C Noted)

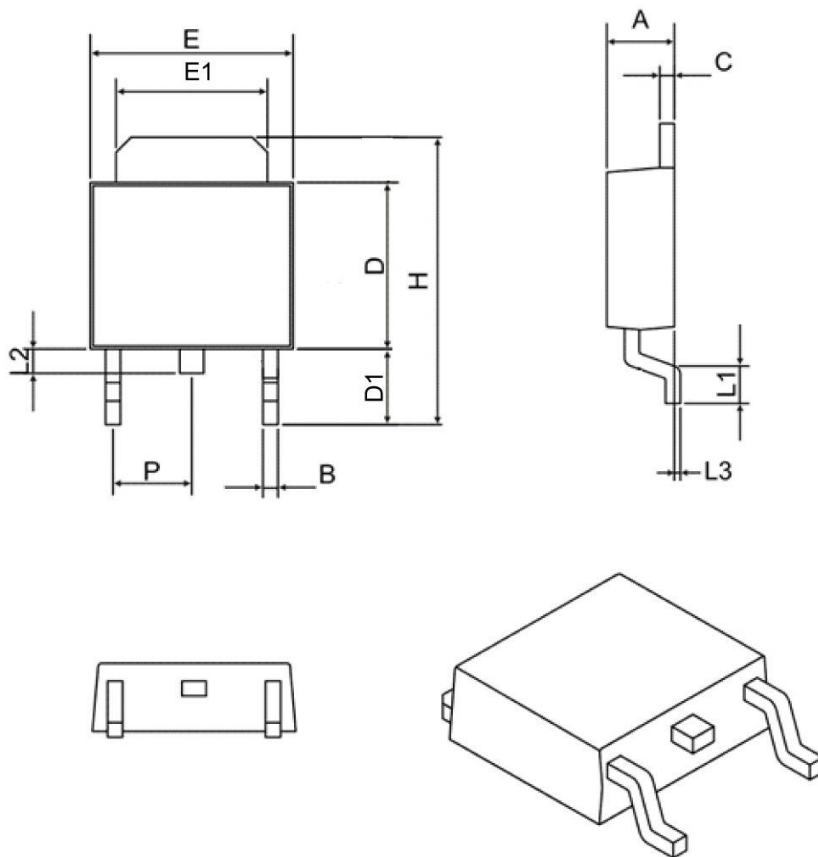


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Typical Characteristics (T_J =25°C Noted)



TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

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