

**N- Channel 250V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME15N25 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

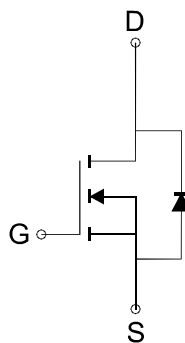
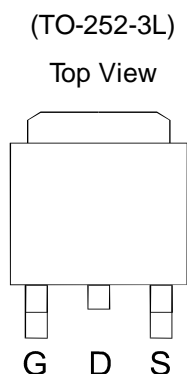
**FEATURES**

- $R_{DS(ON)} \leq 265m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- DC/DC Converter
- Load Switch
- LCD/ LED Display inverter

**PIN CONFIGURATION**



N-Channel MOSFET

Ordering Information: ME15N25 (Pb-free)

ME15N25-G (Green product-Halogen free )

**Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	250	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	Tc=25°C	17.1
		Tc=70°C	13.7
Pulsed Drain Current	$I_{DM}$	68.6	A
Maximum Power Dissipation	$P_D$	Tc=25°C	125
		Tc=70°C	80
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	°C
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	1	°C/W

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper



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Electrical Characteristics (Tc =25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	250			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	2		4	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±25V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> = 7A		220	265	mΩ
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.74	1	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =200V, V <sub>GS</sub> =10V, I <sub>D</sub> =14A		70.8		nC
Q <sub>gs</sub>	Gate-Source Charge			16.2		
Q <sub>gd</sub>	Gate-Drain Charge			23.9		
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		3480		pF
C <sub>oss</sub>	Output Capacitance			112		
C <sub>rss</sub>	Reverse Transfer Capacitance			51		
R <sub>g</sub>	Gate resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		2.3		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =125V, R <sub>L</sub> =18Ω V <sub>GEN</sub> =10V, R <sub>G</sub> =25Ω		53		ns
t <sub>r</sub>	Turn-On Rise Time			62.6		
t <sub>d(off)</sub>	Turn-Off Delay Time			198		
t <sub>f</sub>	Turn-Off Fall Time			83.5		

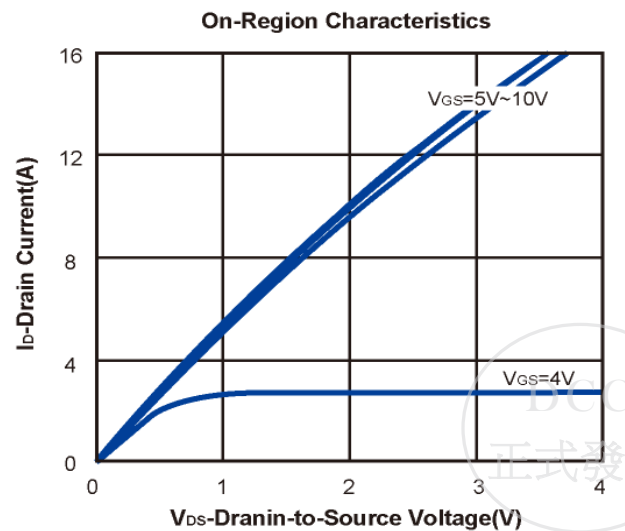
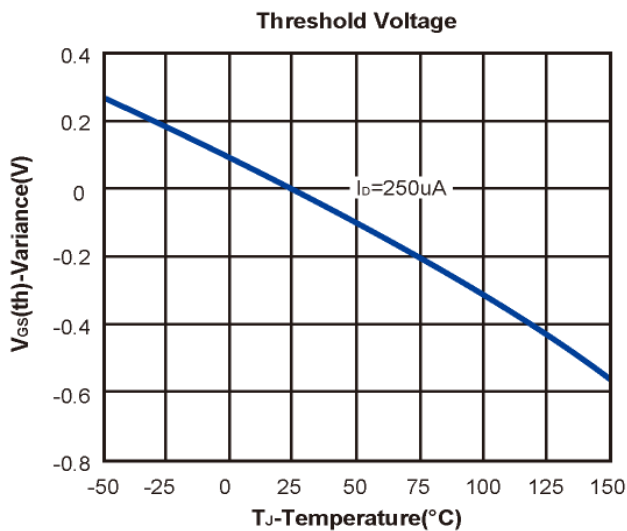
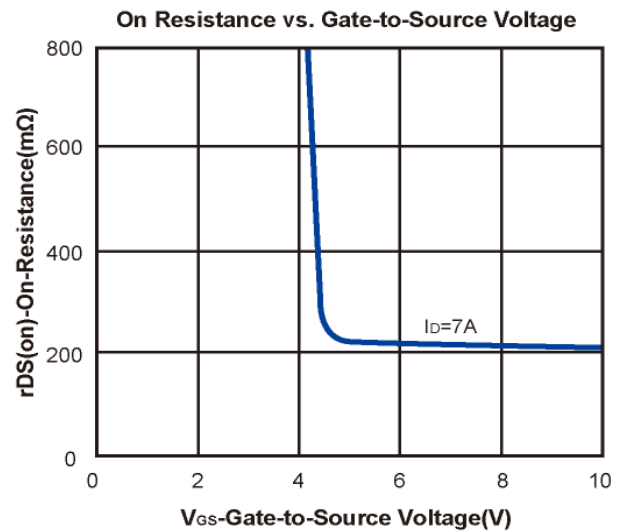
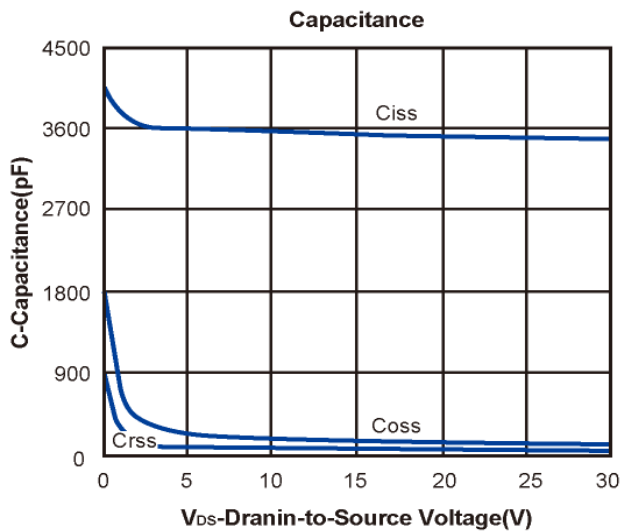
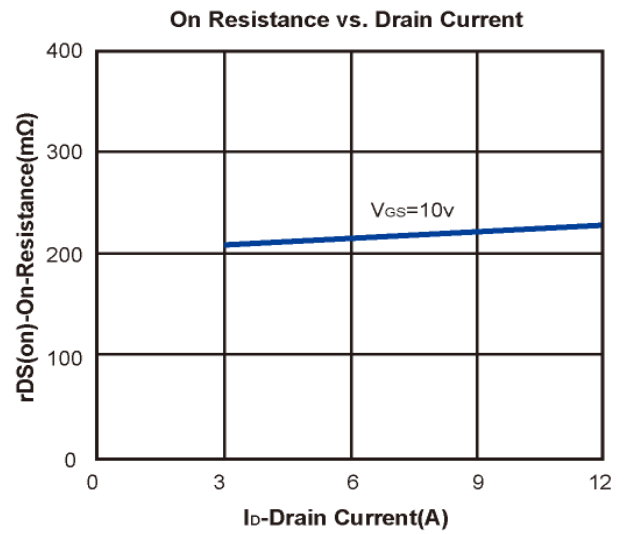
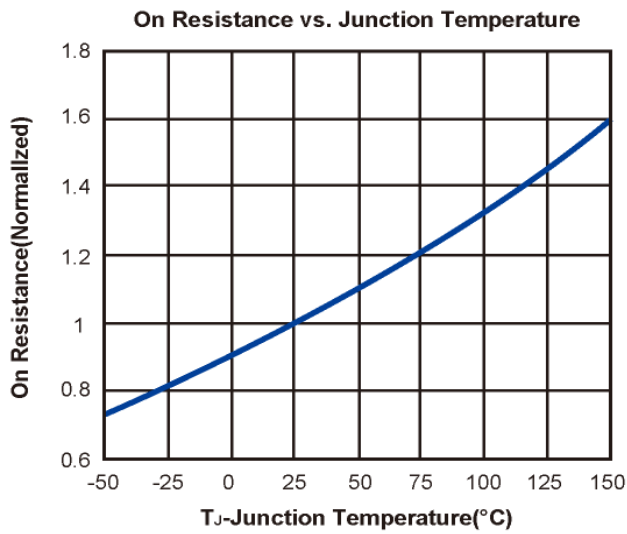
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



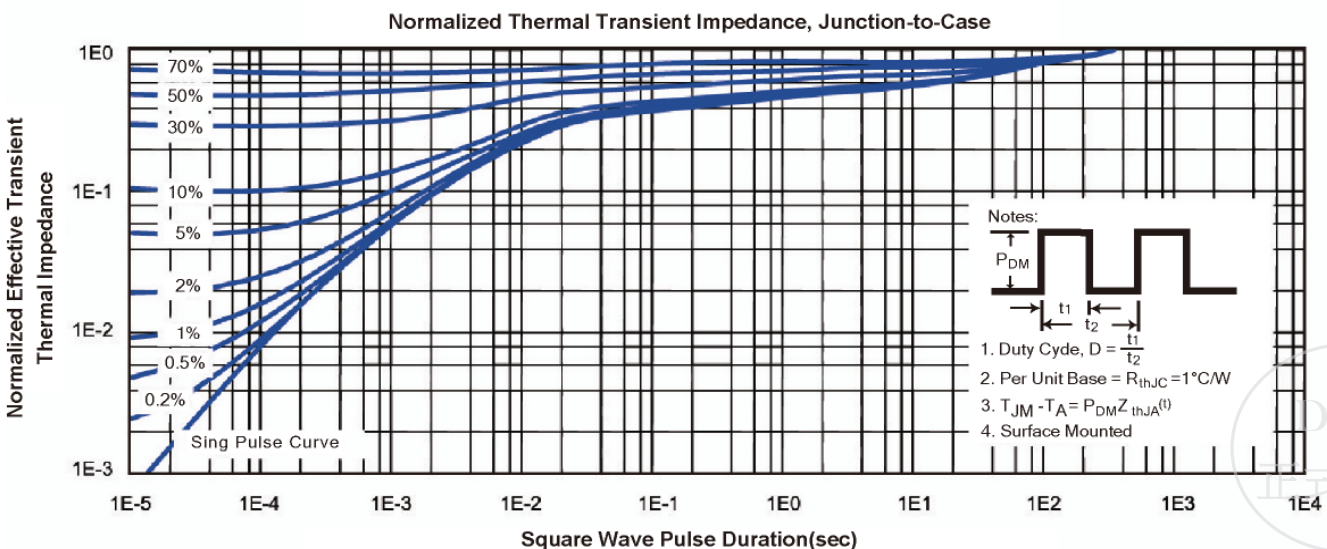
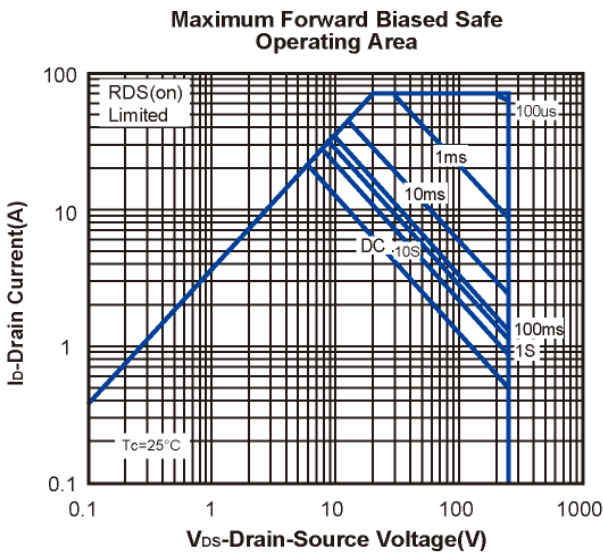
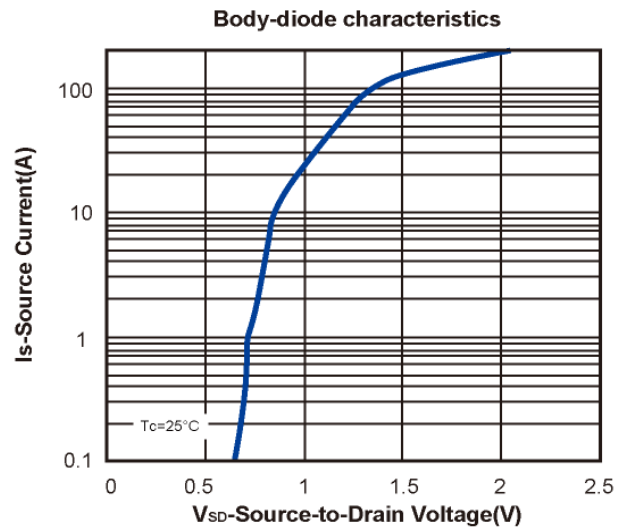
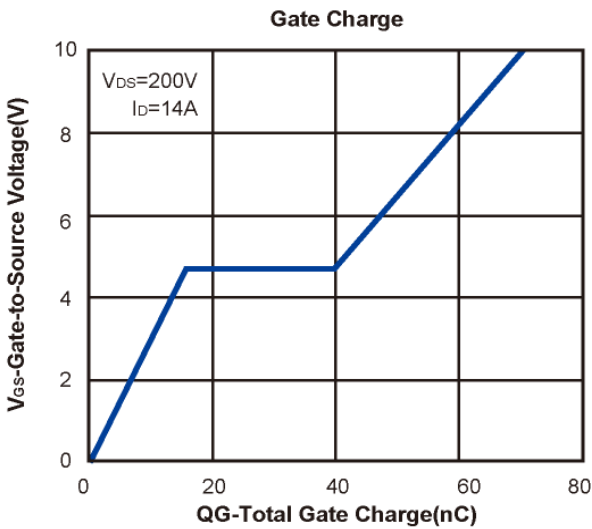
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Typical Characteristics (T<sub>J</sub> =25°C Noted)

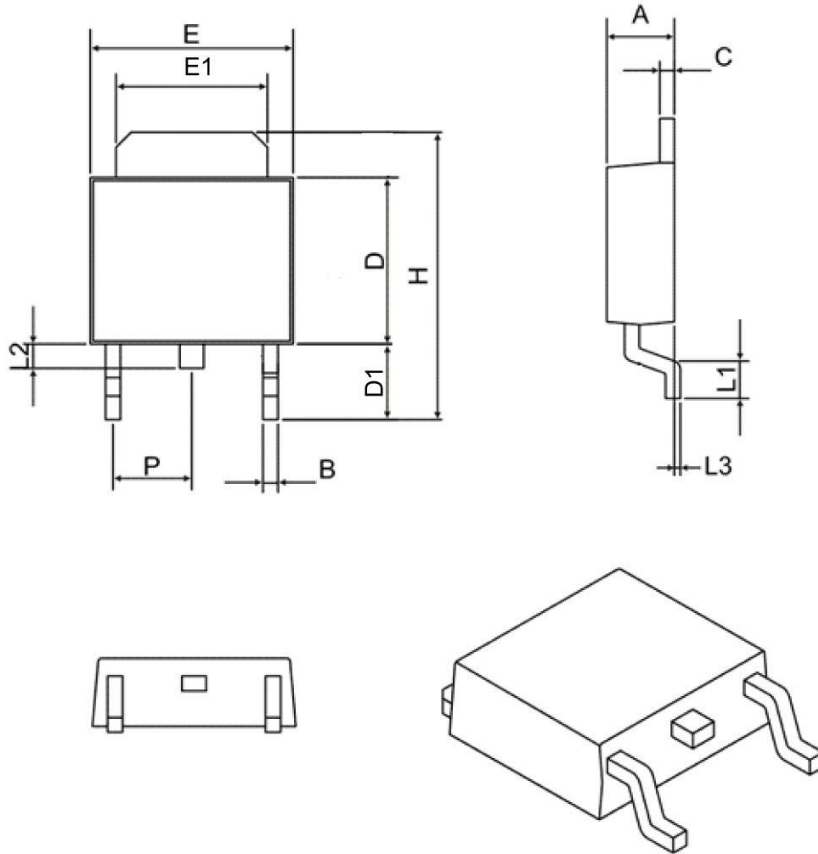


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**TO252-3L Package Outline**



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

