ME200N04T / ME200N04T-G

N- Channel 40V (D-S) MOSFET

GENERAL DESCRIPTION

The ME200N04T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

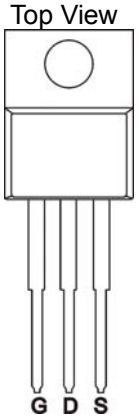
FEATURES

- $R_{DS(ON)} \leqq 3.5m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 4.7m\Omega @ V_{GS}=5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION

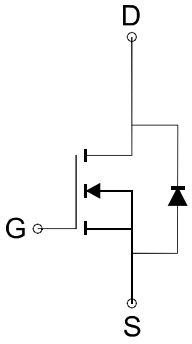
(TO-220)

Top View



APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch



N-Channel MOSFET

Ordering Information: ME200N04T (Pb-free)

ME200N04T-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	189	A
	T_C=70℃		158	
Pulsed Drain Current		I_{DM}	755	A
Maximum Power Dissipation	T_C=25℃	P_D	231	W
	T_C=70℃		162	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 175	℃
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.65	℃/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in^2 FR4 board with 2 oz copper.

Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±16V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=75A		2.5	3.5	mΩ
		V_{GS}=5V, I_D=40A		3.5	4.7	mΩ
V_{SD}	Diode Forward Voltage *	I_S=75A, V_{GS}=0V			1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=32V, V_{GS}=5V, I_D=75A		137		nC
Qgs	Gate-Source Charge			60.8		
Qgd	Gate-Drain Charge			52.6		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		3		Ω
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		15872		pF
Coss	Output Capacitance			1242		
Crss	Reverse Transfer Capacitance			245		
$t_{d(on)}$	Turn-On Delay Time	V_{GS} =5V, R_L=0.5Ω V_{DD}=20V, R_G=4Ω		170		ns
t_r	Turn-On Rise Time			767		
$t_{d(off)}$	Turn-Off Delay Time			153		
t_f	Turn-Off Fall Time			95.4		

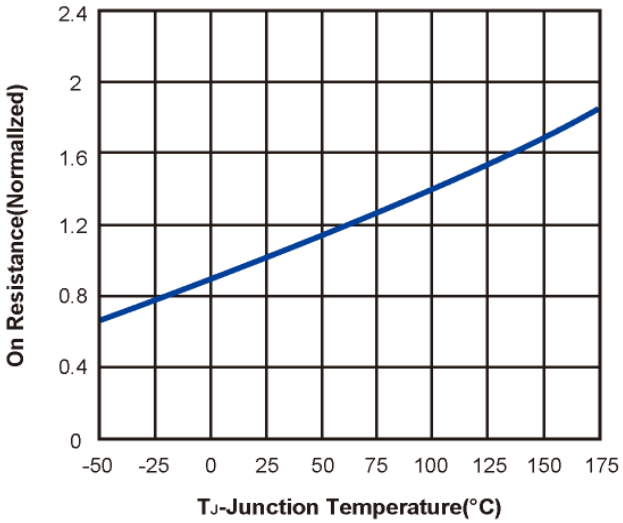
Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

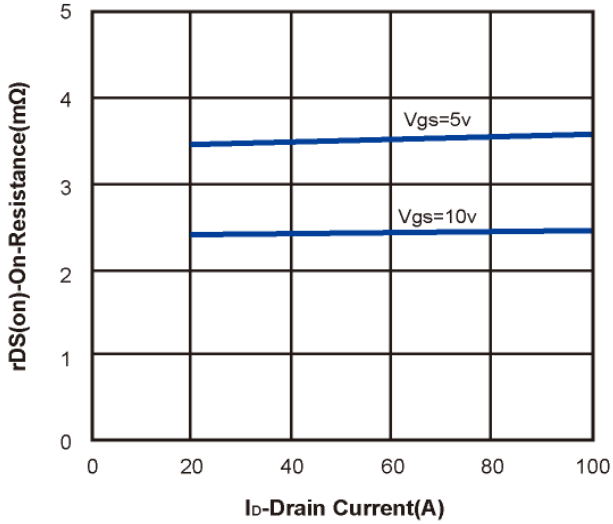
N- Channel 40V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

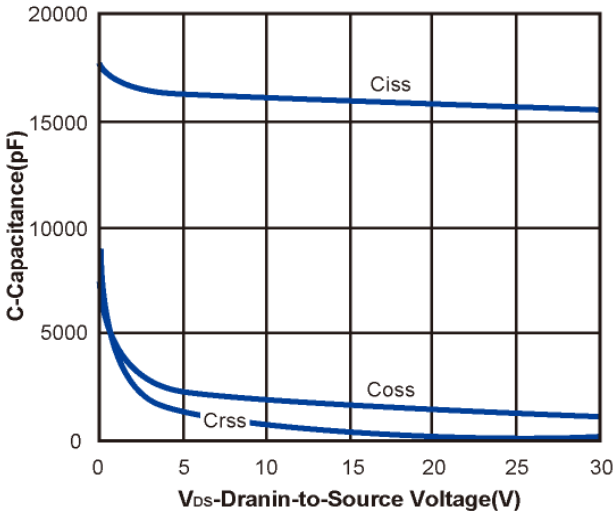
On Resistance vs. Junction Temperature



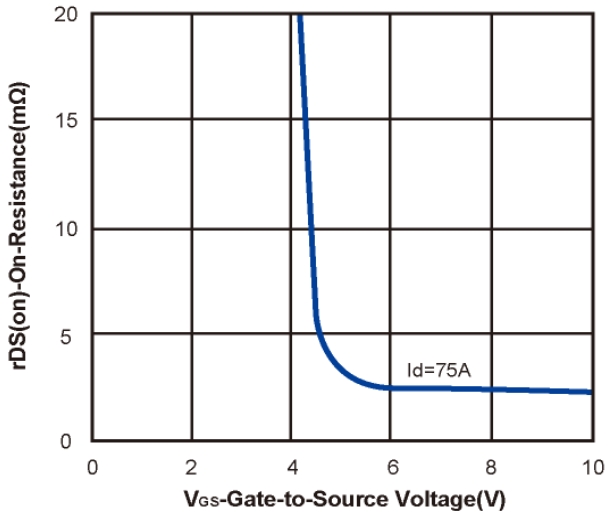
On Resistance vs. Drain Current



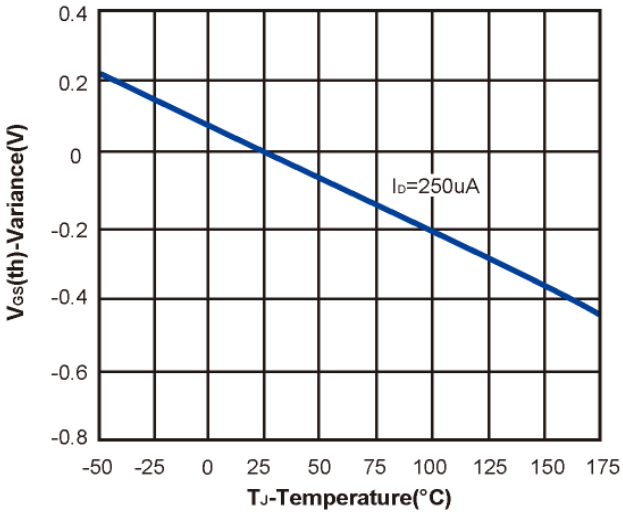
Capacitance



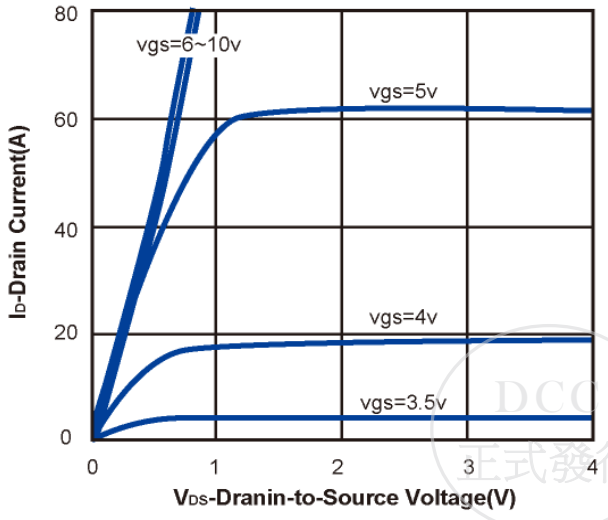
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



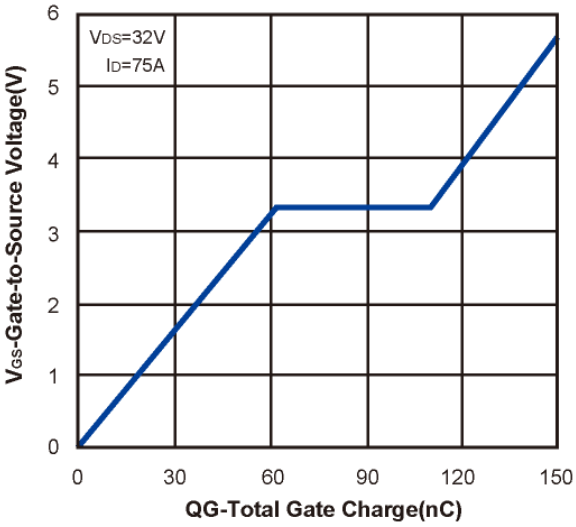
On-Region Characteristics



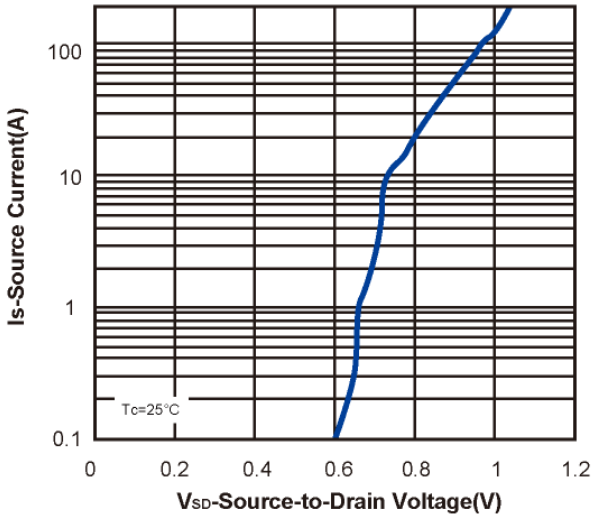
N- Channel 40V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

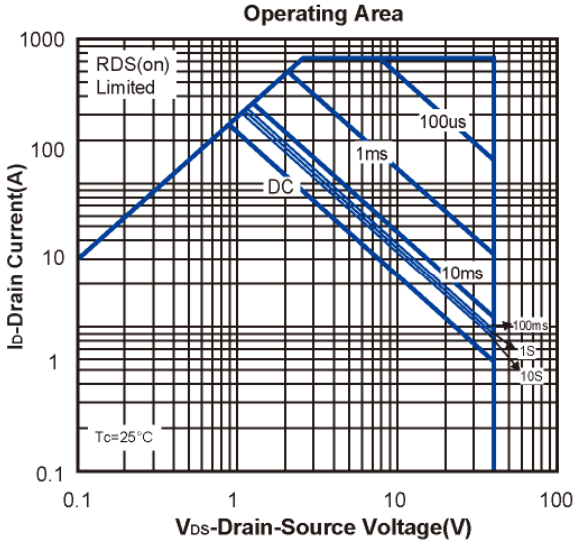
Gate Charge



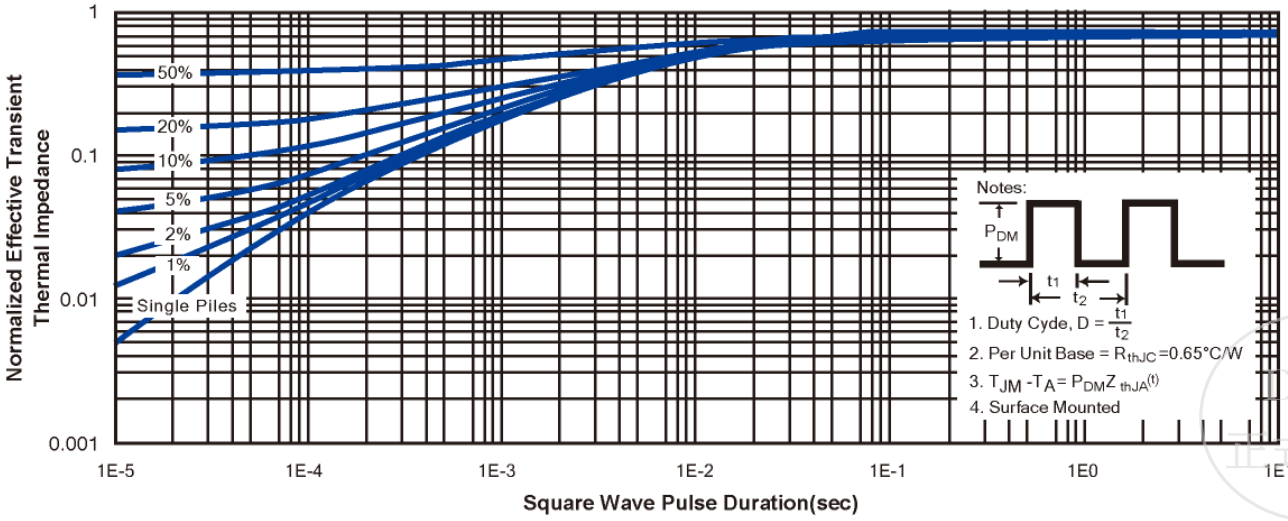
Body-diode characteristics



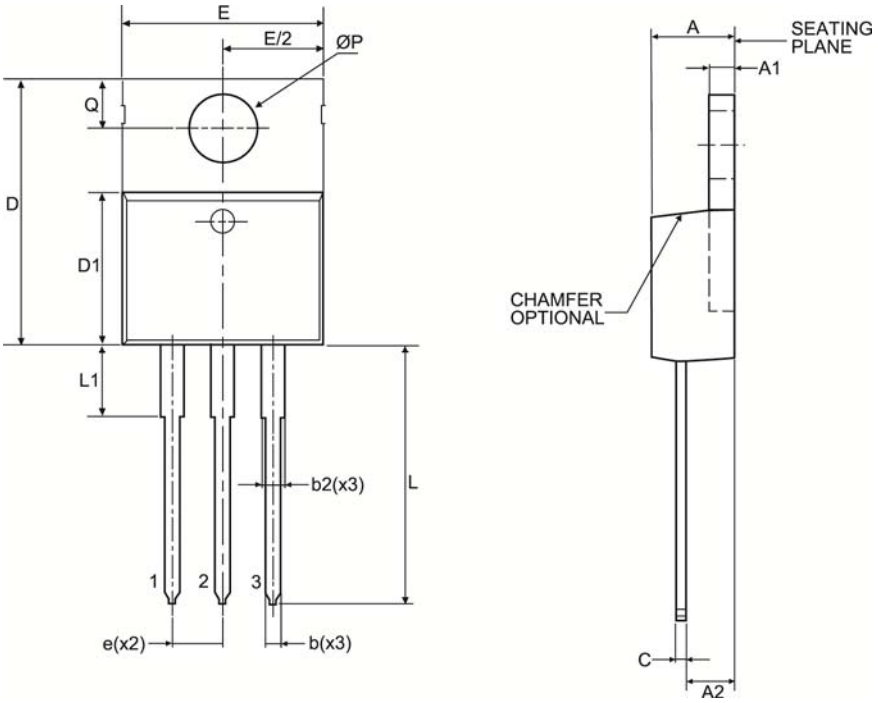
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20