

P-Channel 30V (D-S) MOSFET

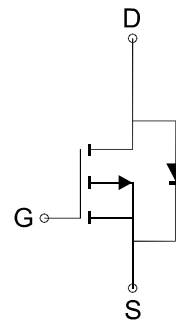
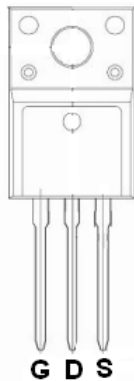
GENERAL DESCRIPTION

The ME20P03F is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

PIN CONFIGURATION

(TO-220F)

Top View



P-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leq 31.5m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 44m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

Ordering Information: ME20P03F (Pb-free)

ME20P03F-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_c = 25^\circ C$	-29.7
		$T_c = 70^\circ C$	-24.9
Pulsed Drain Current	I_{DM}	-119	A
Maximum Power Dissipation	P_D	$T_c = 25^\circ C$	40.3
		$T_c = 70^\circ C$	28.2
Operating Junction Temperature	T_J	-55 to 175	°C
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	3.72	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper.

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Electrical Characteristics ($T_c = 25^\circ\text{C}$ Unless Otherwise Specified)

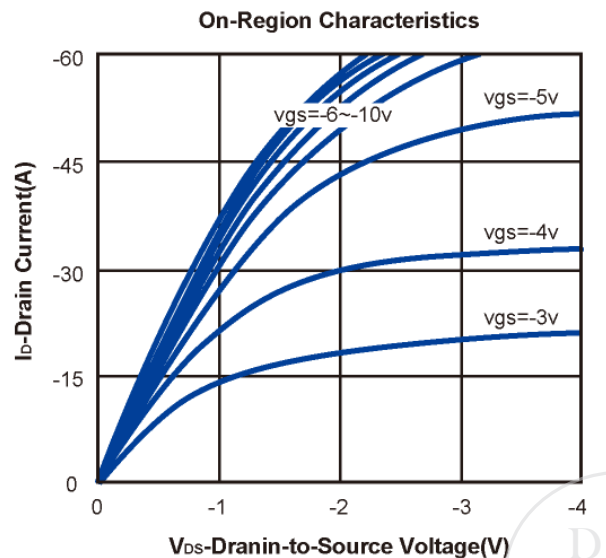
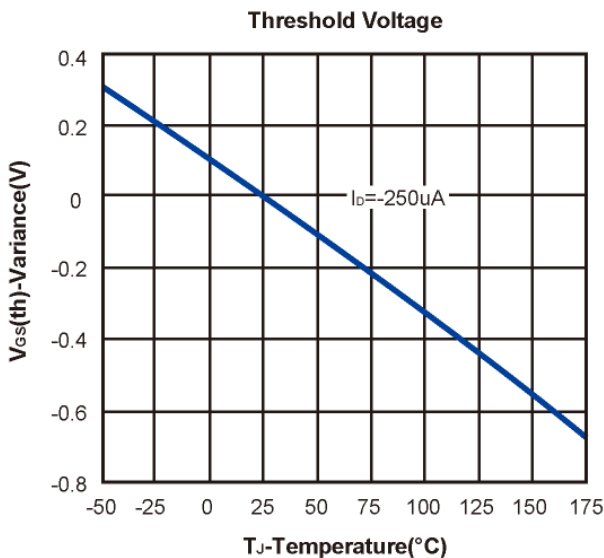
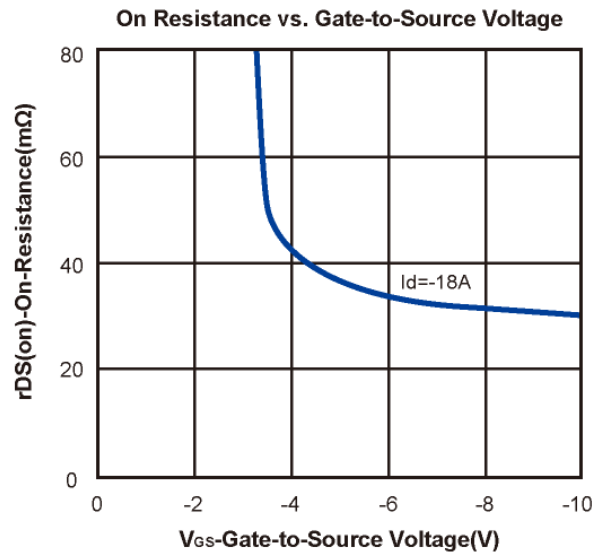
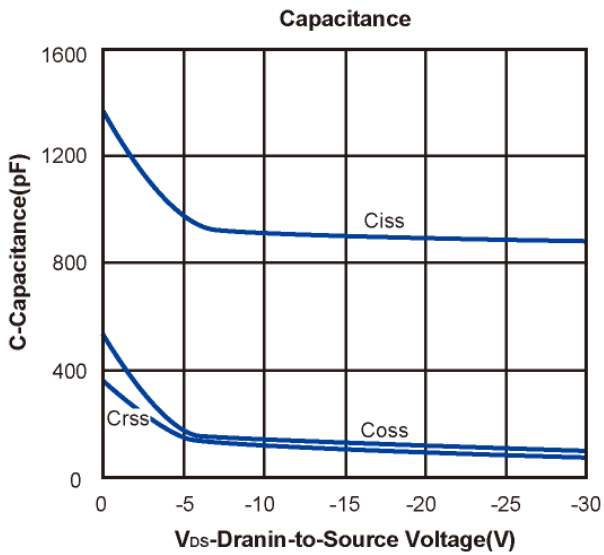
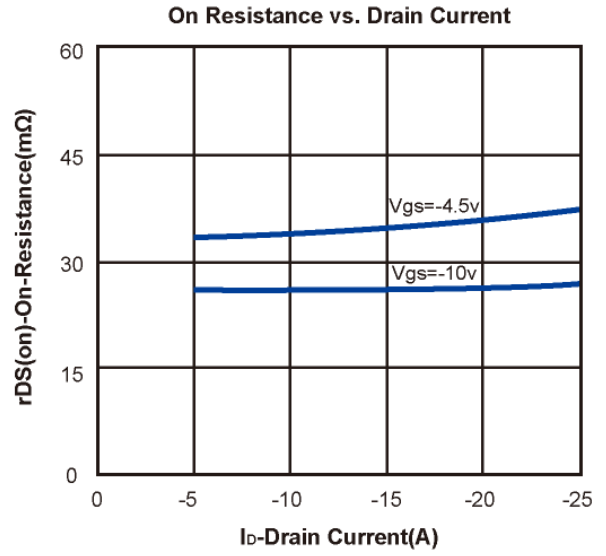
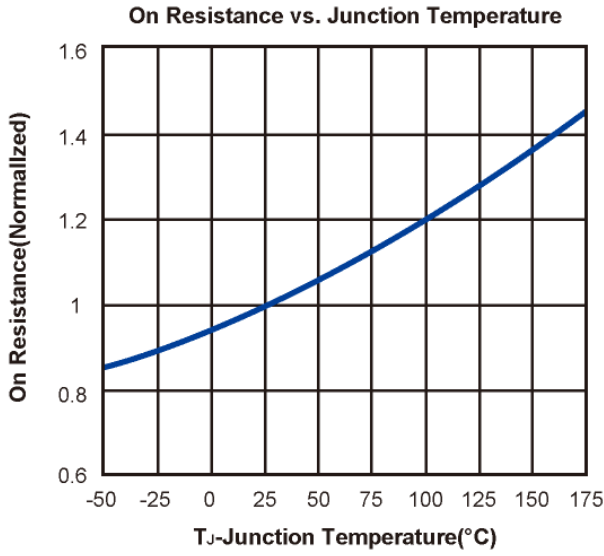
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3	V
I _{GSS}	Gate-Body Leakage	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30, V_{GS}=0V$			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	$V_{GS}=-10V, I_D=-18A$		26	31.5	m Ω
		$V_{GS}=-4.5V, I_D=-10A$		34	44	
V _{SD}	Diode Forward Voltage*	$I_{SD}=-18A, V_{GS}=0V$			-1.3	V
DYNAMIC						
Q _g	Total Gate Charge	$V_{DD}=-25V, V_{GS}=-4.5V, I_D=-18A$		17.6		nc
Q _{gs}	Gate-Source Charge			7.3		
Q _{gd}	Gate-Drain Charge			9.3		
C _{iss}	Input Capacitance	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$		887		pF
C _{oss}	Output Capacitance			110		
C _{rss}	Reverse Transfer Capacitance			96.2		
t _{d(on)}	Turn-On Delay Time	$V_{DD}=-15V, I_D=-18A,$ $V_{GS}=-10V, R_G=3.3\Omega,$ $R_L=0.8\Omega$		34		ns
t _r	Turn-On Rise Time			17		
t _{d(off)}	Turn-Off Delay Time			51		
t _f	Turn-Off Fall Time			10		

 Notes: a, pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b, Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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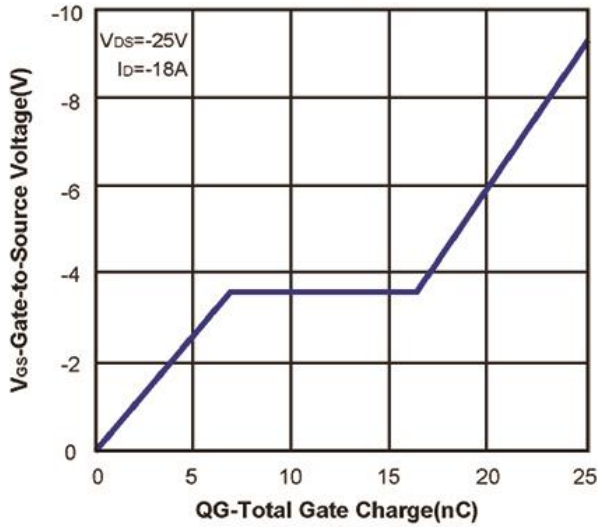
Typical Characteristics (T_J =25°C Noted)



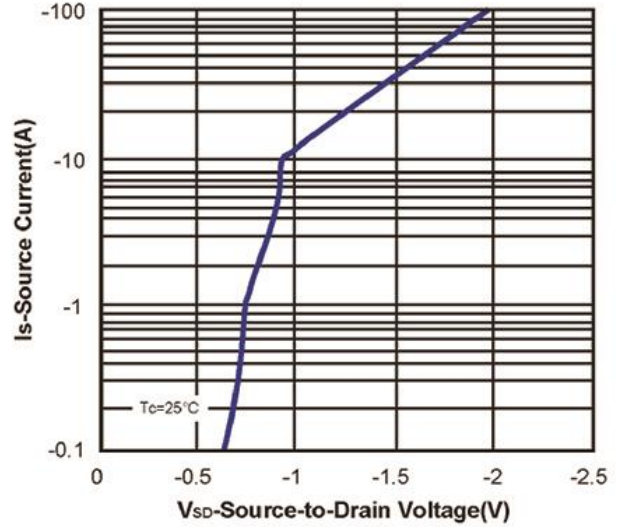
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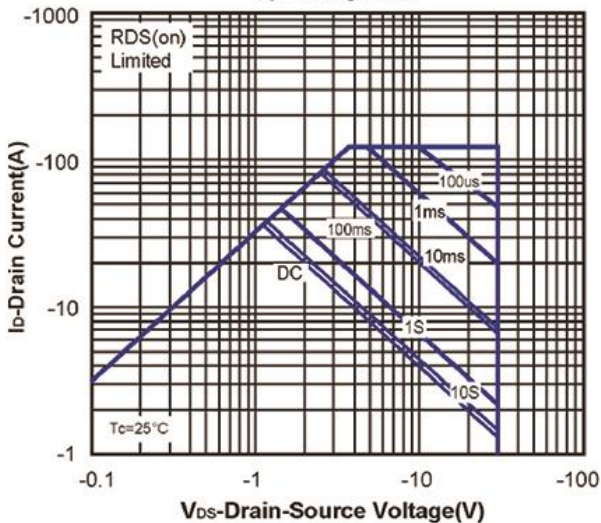
Gate Charge



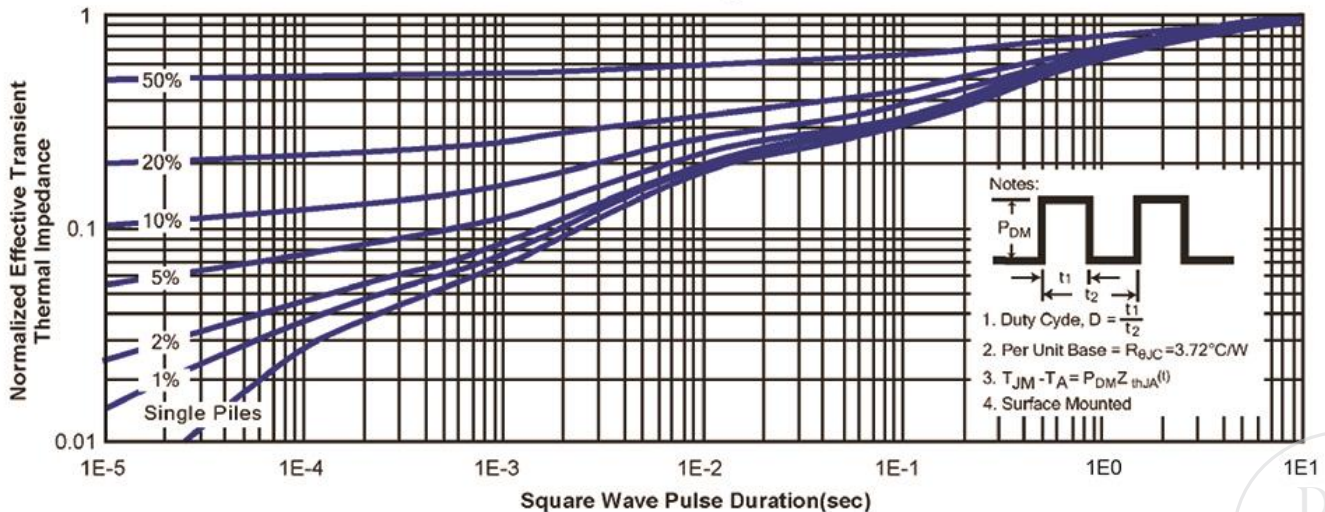
Body-diode characteristics



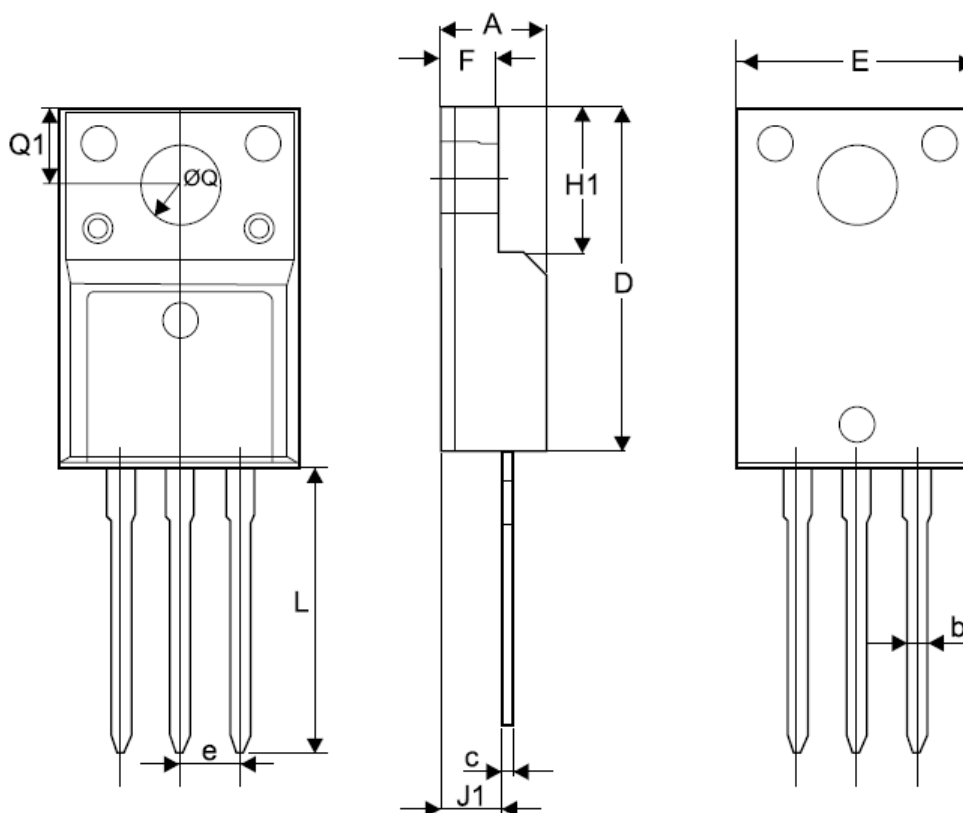
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-220F Package Outline



Symbol	MILLIMETERS(mm)	
	MIN	MAX
A	4.40	5.00
b	0.60	1.00
C	0.30	0.70
D	15.40	16.40
E	6.96	10.46
F	2.30	2.80
e	2.54 TYP	
H1	6.40	7.00
J1	2.45	3.05
L	12.28	13.68
ØQ	2.92	3.38
Q1	3.05	3.55