

P-Channel 20V(D-S) MOSFET, ESD Protected

GENERAL DESCRIPTION

The ME2301DC is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

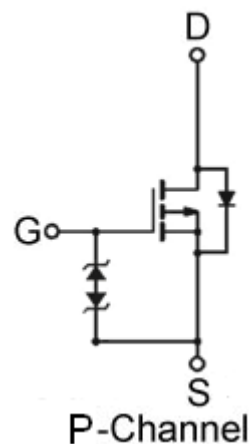
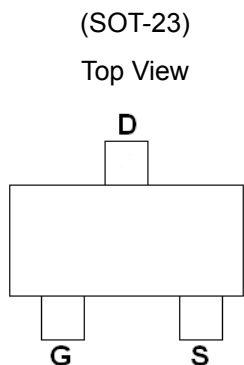
FEATURES

- R_{DS(ON)} 110mΩ@V_{GS}=-4.5V
- R_{DS(ON)} 150mΩ@V_{GS}=-2.5V
- Super high density cell design for extremely low R_{DS(ON)}

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



Ordering Information: ME2301DC (Pb-free)
 ME2301DC-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25 Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±8	V
Continuous Drain Current *	I _D	T _A =25	-2.7
		T _A =70	-2.1
Pulsed Drain Current	I _{DM}	-11	A
Maximum Power Dissipation	P _D	T _A =25	1.3
		T _A =70	0.8
Operating Junction Temperature	T _J	-55 to 150	
Thermal Resistance-Junction to Ambient*	R _{θJA}	100	/W

* The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_A=25 Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-0.4		-1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±8V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-4.5V, I _D = -2.8A		90	110	m
		V _{GS} =-2.5V, I _D = -2.0A		110	150	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1.4	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-6V, V _{GS} =-4.5V, I _D =-2.8A		5.5		nC
Q _{gs}	Gate-Source Charge			1.5		
Q _{gd}	Gate-Drain Charge			1.3		
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1.0MHz		510		pF
C _{oss}	Output Capacitance			53		
C _{rss}	Reverse Transfer Capacitance			17		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-6V, R _L =6 R _{GEN} =6, V _{GS} =-4.5V		1360		ns
t _r	Turn-On Rise Time			831		
t _{d(off)}	Turn-Off Delay Time			5520		
t _f	Turn-Off Fall time			1520		

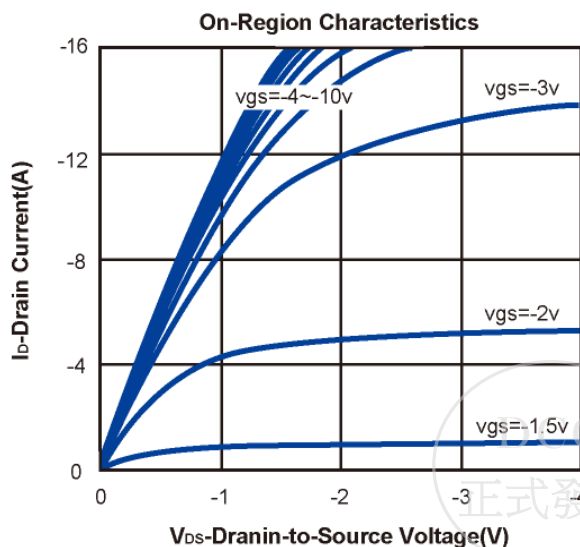
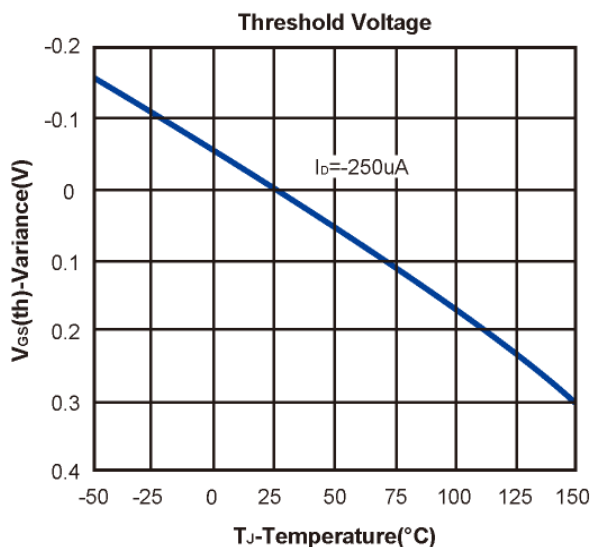
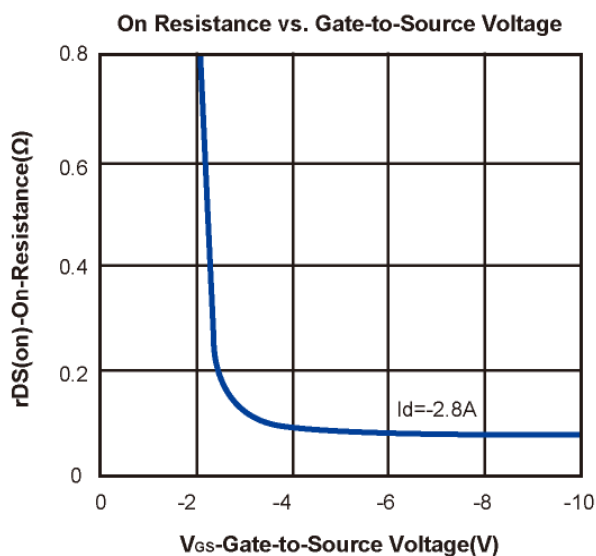
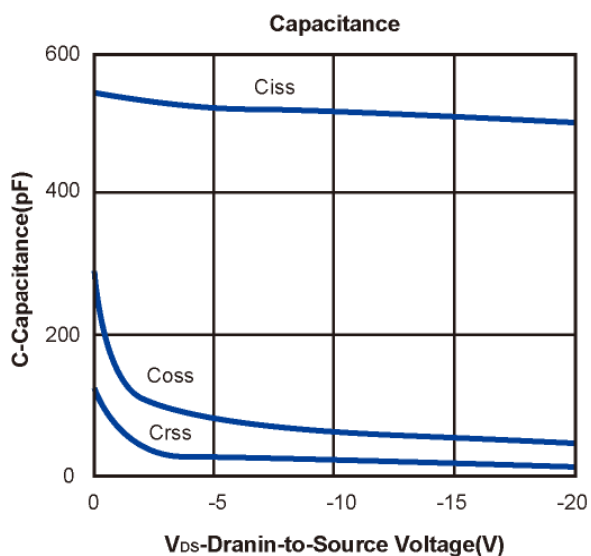
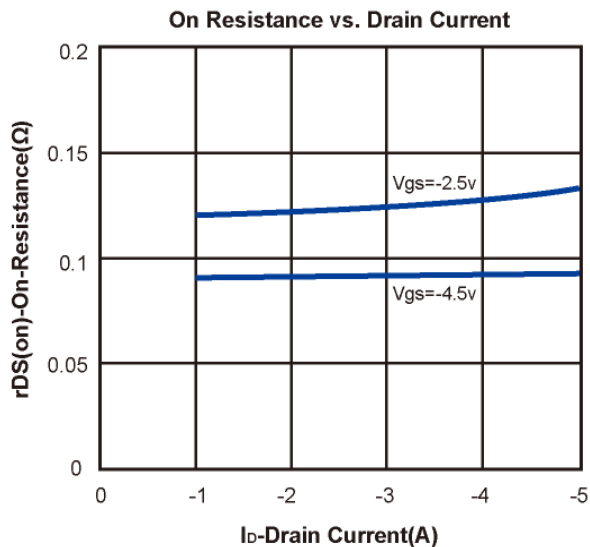
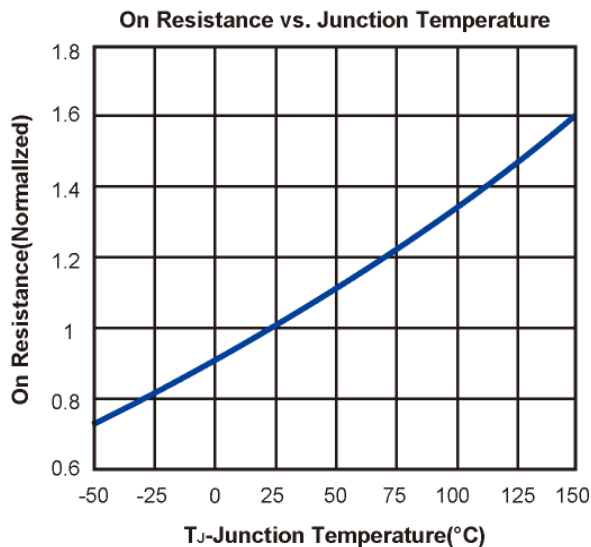
Notes: a. Pulse test: pulse width 300us, duty cycle 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



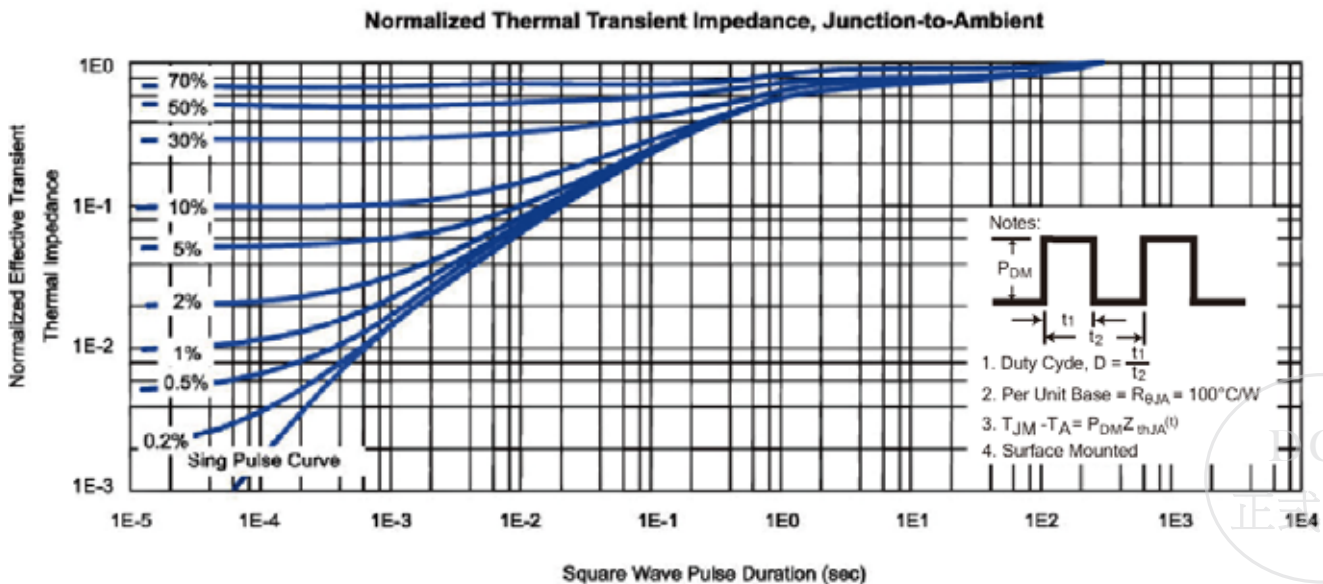
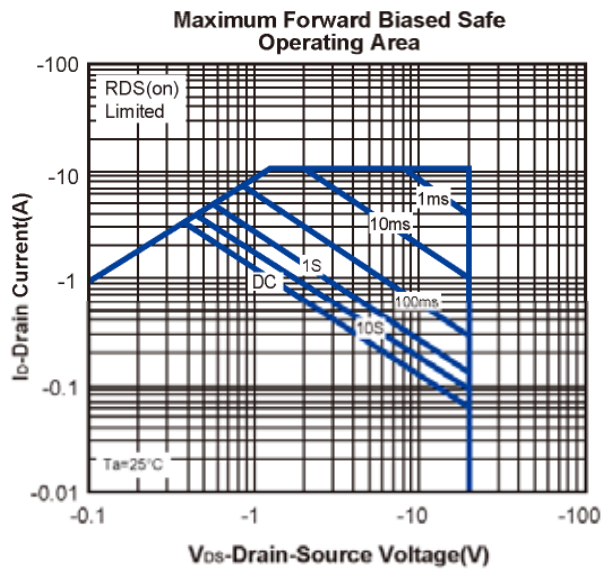
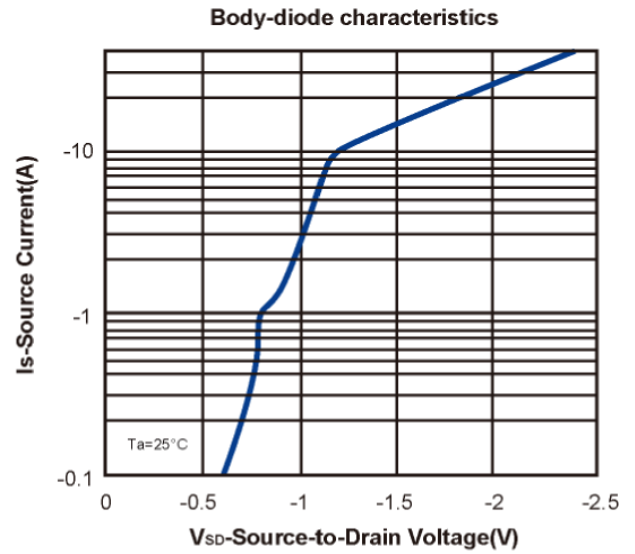
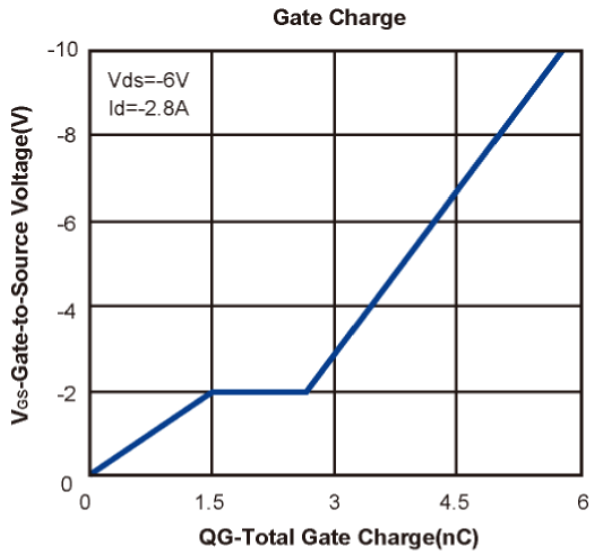
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Typical Characteristics (T_J =25 Noted)

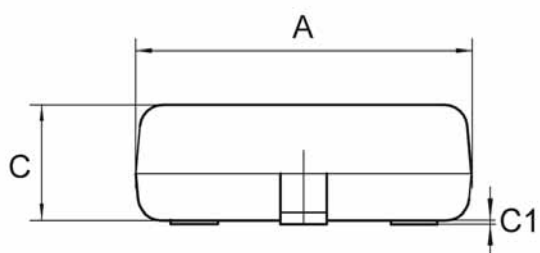
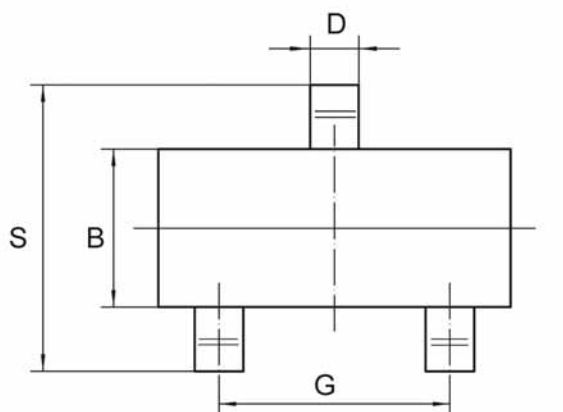


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SOT-23 Package Outline



Symbol	MILLIMETERS	
	MIN	MAX
A	2.8	3.0
B	1.2	1.4
C	0.9	1.1
C1	-	0.1
D	0.3	0.5
G	1.90 REF	
J	0.05	0.15
K	0.2	-
S	2.2	2.6

