ME2304/ME2304-G

N-Channel Enhancement MOSFET

GENERAL DESCRIPTION

The ME2304 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦117mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦190mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

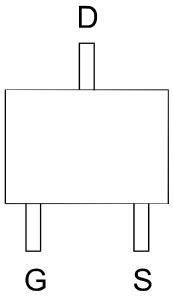
APPLICATIONS

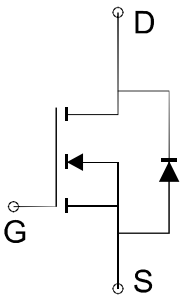
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(SOT-23)

Top View





Ordering Information: ME2304 (Pb-free)

ME2304-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	2.3	A
	T_A=70℃		1.8	
Pulsed Drain Current		I_{DM}	9	A
Maximum Power Dissipation	T_A=25℃	P_D	1	W
	T_A=70℃		0.6	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	130	℃/W

N-Channel Enhancement MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.5		3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D= 2.5A		92	117	mΩ
		V_{GS}=4.5V, I_D= 2.0A		142	190	
V_{SD}	Diode Forward Voltage	I_S=1.25A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=2.5A		4.6		nC
Qgs	Gate-Source Charge			0.8		
Qgd	Gate-Drain Charge			1.2		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		225		pF
Coss	Output Capacitance			50		
Crss	Reverse Transfer Capacitance			28		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1.0A, V_{GEN}=10V R_G=6Ω		7.5		ns
t_r	Turn-On Rise Time			12.5		
$t_{d(off)}$	Turn-Off Delay Time			19		
t_f	Turn-Off Fall time			15		

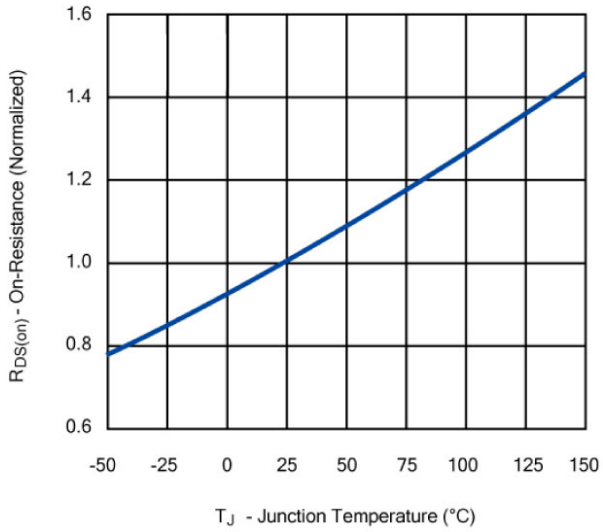
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

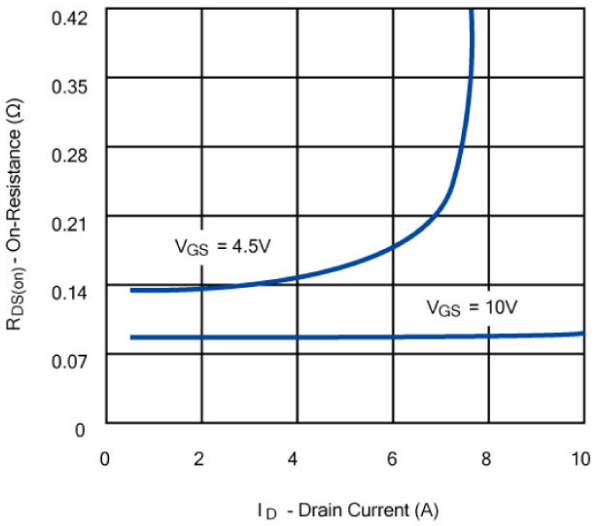
N-Channel Enhancement MOSFET

Typical Characteristics (T_J =25℃ Noted)

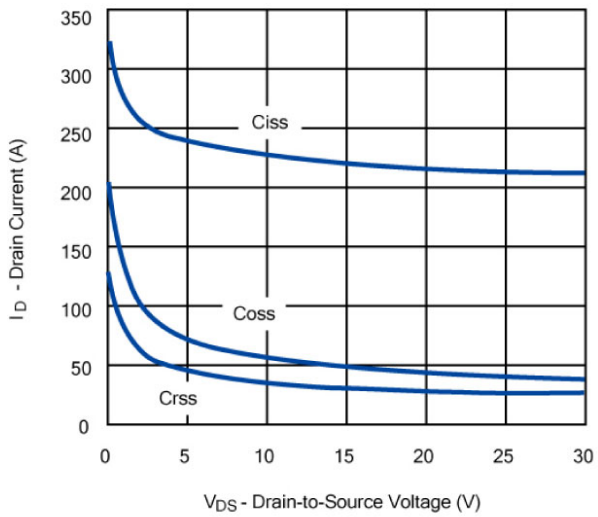
On-Resistance vs. Junction Temperature



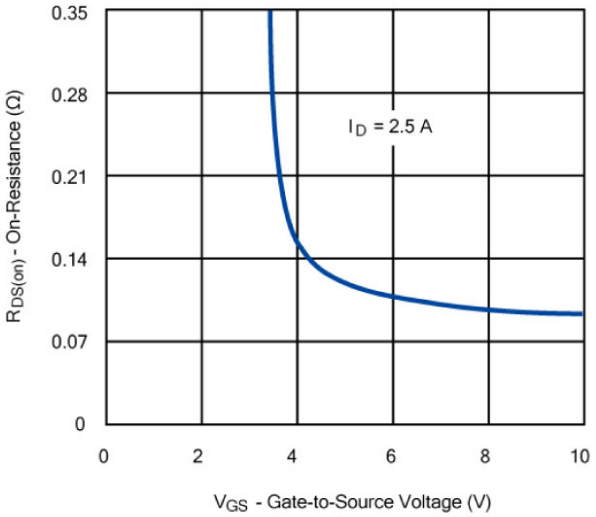
On-Resistance vs. Drain Current



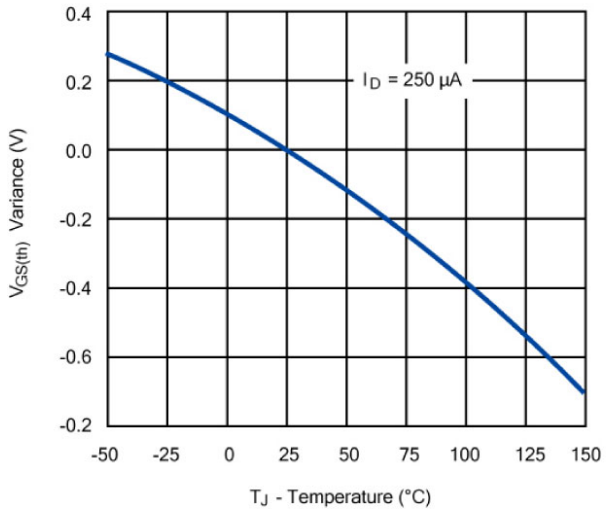
Capacitance



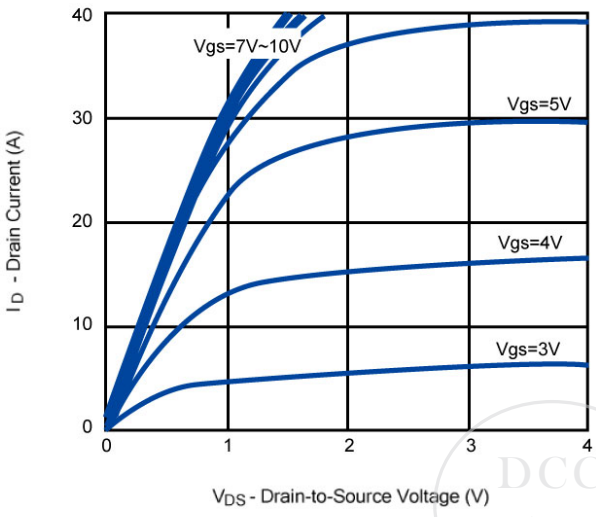
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



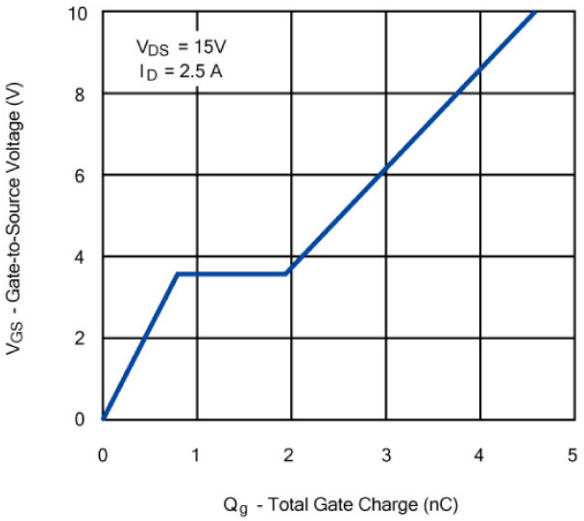
Output Characteristics



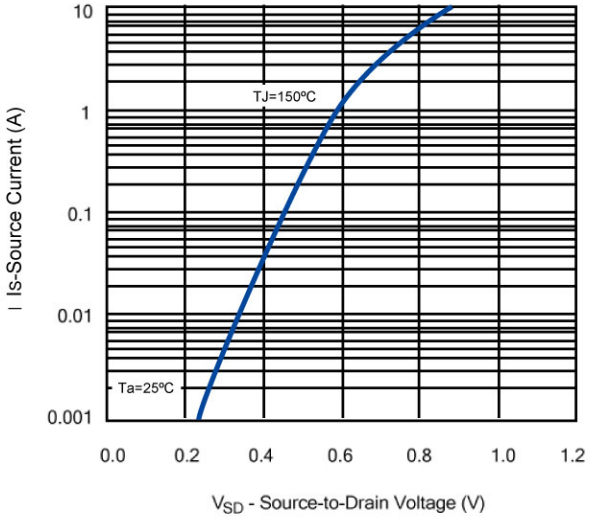
N-Channel Enhancement MOSFET

Typical Characteristics (T_J =25℃ Noted)

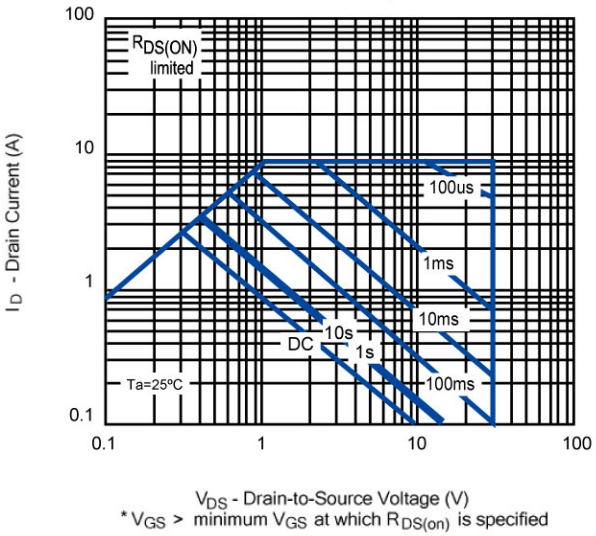
Gate Charge



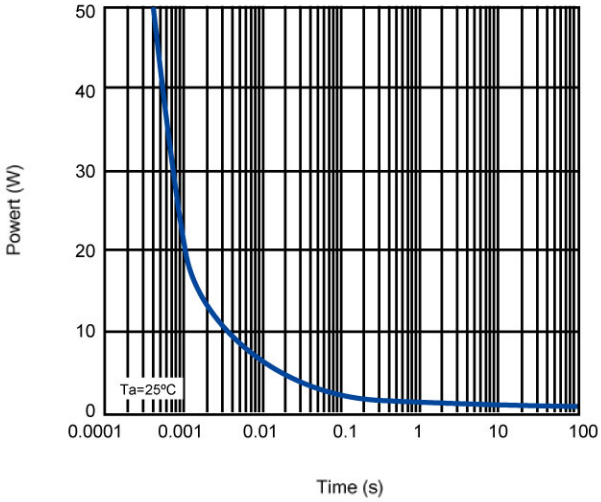
Body-diode characteristics



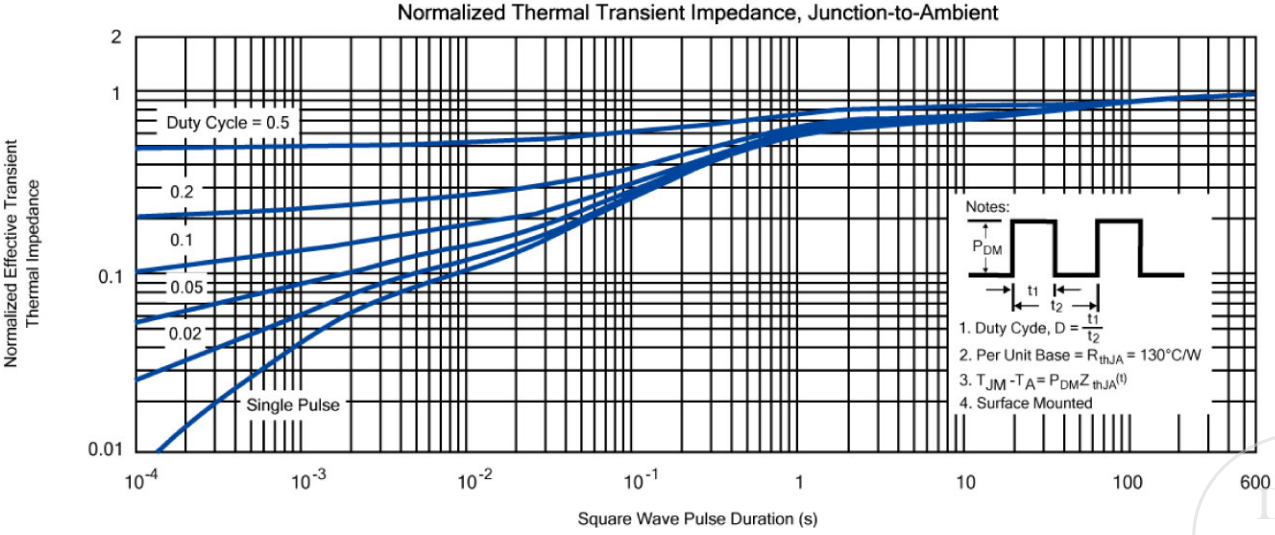
Safe Operating Area



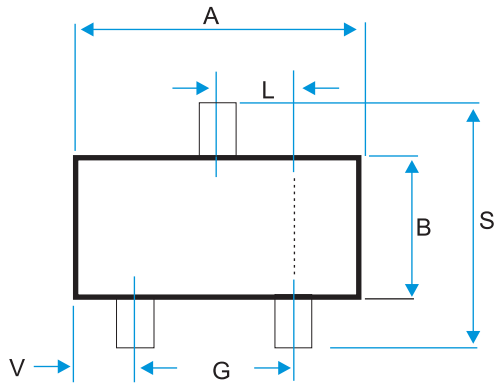
Single Pulse Power

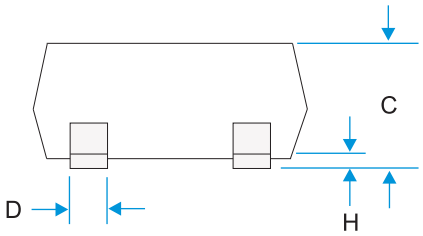


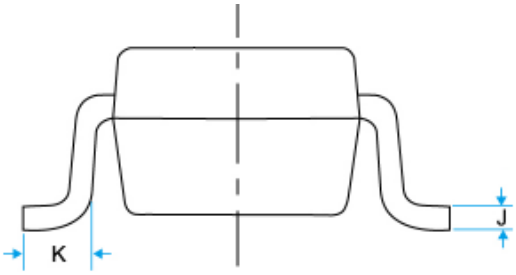
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60