P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2317D-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦45mΩ@V_{GS}=-10V
- $R_{DS(ON)}$ ≦53mΩ@V_{GS}=-4.5V
- $R_{DS(ON)}$ ≦80mΩ@V_{GS}=-2.5V
- Typical ESD performance 3KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

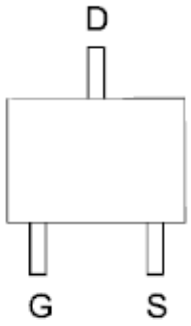
APPLICATIONS

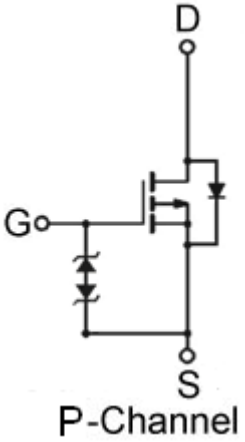
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

PIN CONFIGURATION

(SOT-23)

Top View





Ordering Information ME2317D-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25℃	I_D	-4.4	A
	T_A=70℃		-3.5	
Pulsed Drain Current		I_{DM}	-18	A
Maximum Power Dissipation	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.6		-1.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -3.7A		28	45	mΩ
		V_{GS}=-4.5V, I_D= -2A		34	53	
		V_{GS}=-2.5V, I_D= -2A		61.5	80	
V_{SD}	Diode Forward Voltage	I_S=-2.9A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V,V_{GS}=-10V,I_D=-3.7A		21		nC
Qg	Total Gate Charge	V_{DS}=-15V,V_{GS}=-4.5V,I_D=-3.7A		10.6		
Qgs	Gate-Source Charge			2.6		
Qgd	Gate-Drain Charge			4		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		918		pF
Coss	Output Capacitance			101		
Crss	Reverse Transfer Capacitance			87		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V,R_L=4Ω V_{GS}=-10V,R_G=6Ω I_D=-3.7A		145		ns
t_r	Turn-On Rise Time			115		
$t_{d(off)}$	Turn-Off Delay Time			945		
t_f	Turn-Off Fall time			378		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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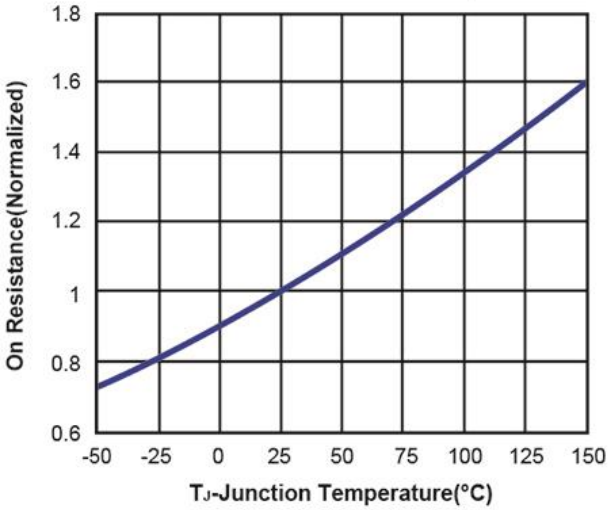
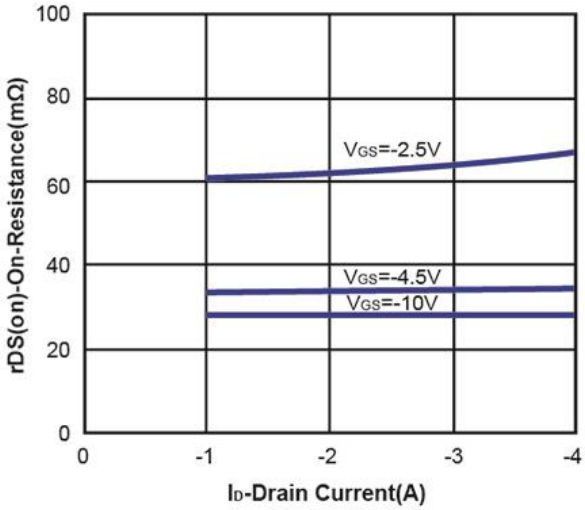
Typical Characteristics (T_J =25℃ Noted)

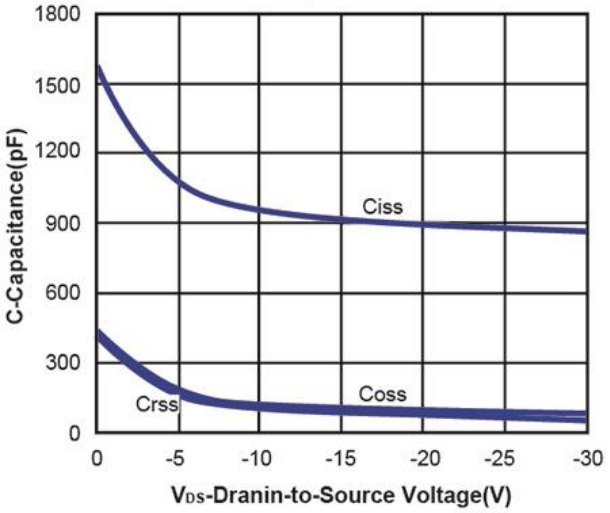
On Resistance vs. Junction Temperature



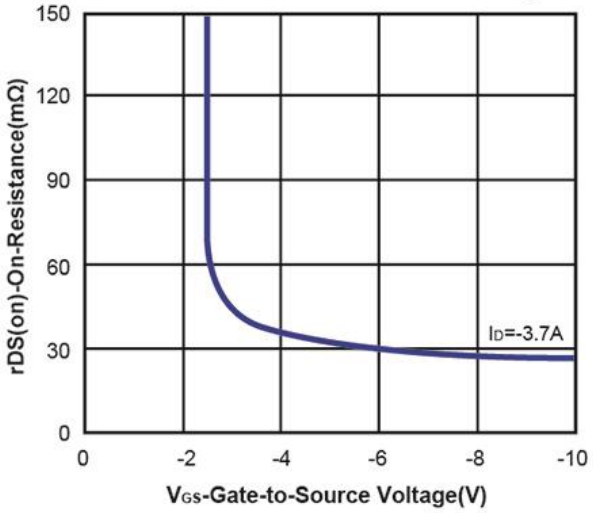
On Resistance vs. Drain Current



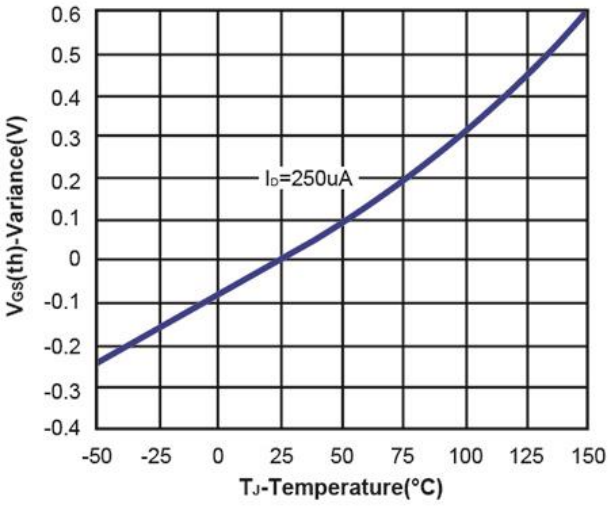
Capacitance



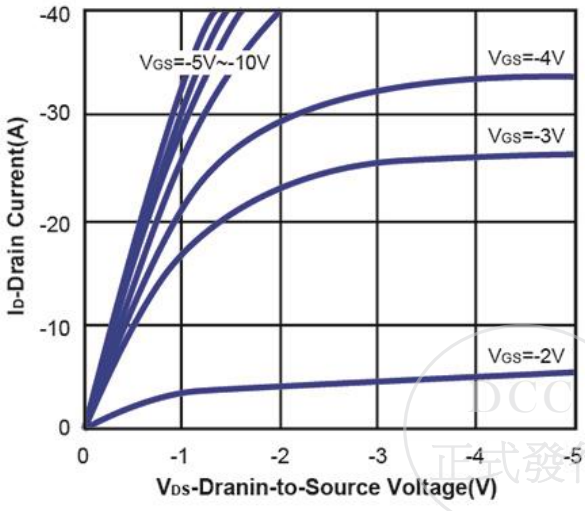
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



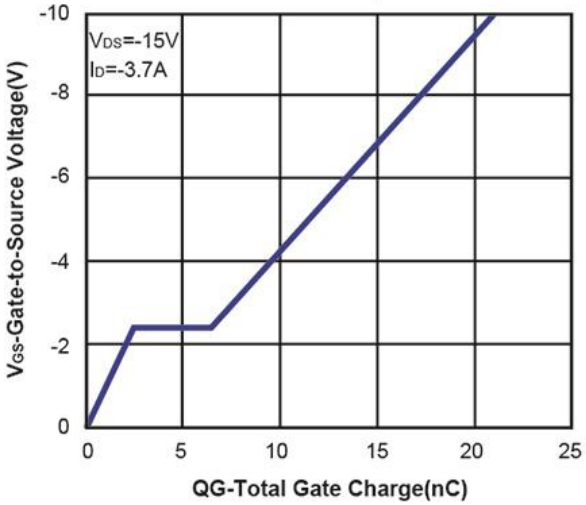
On-Region Characteristics



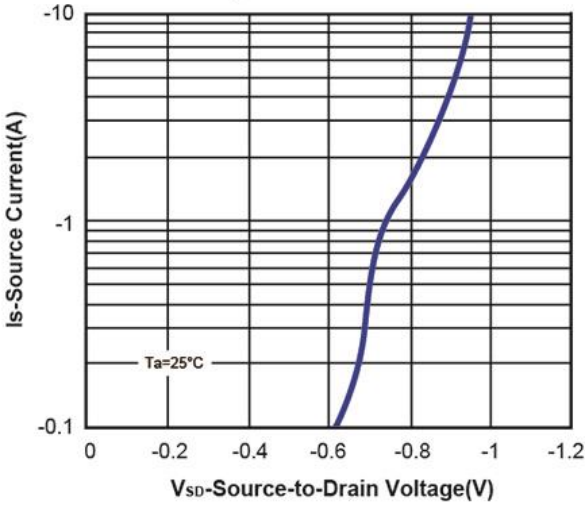
P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

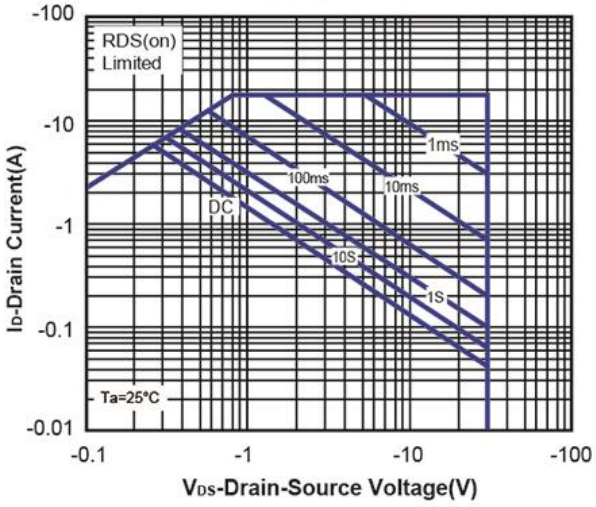
Gate Charge



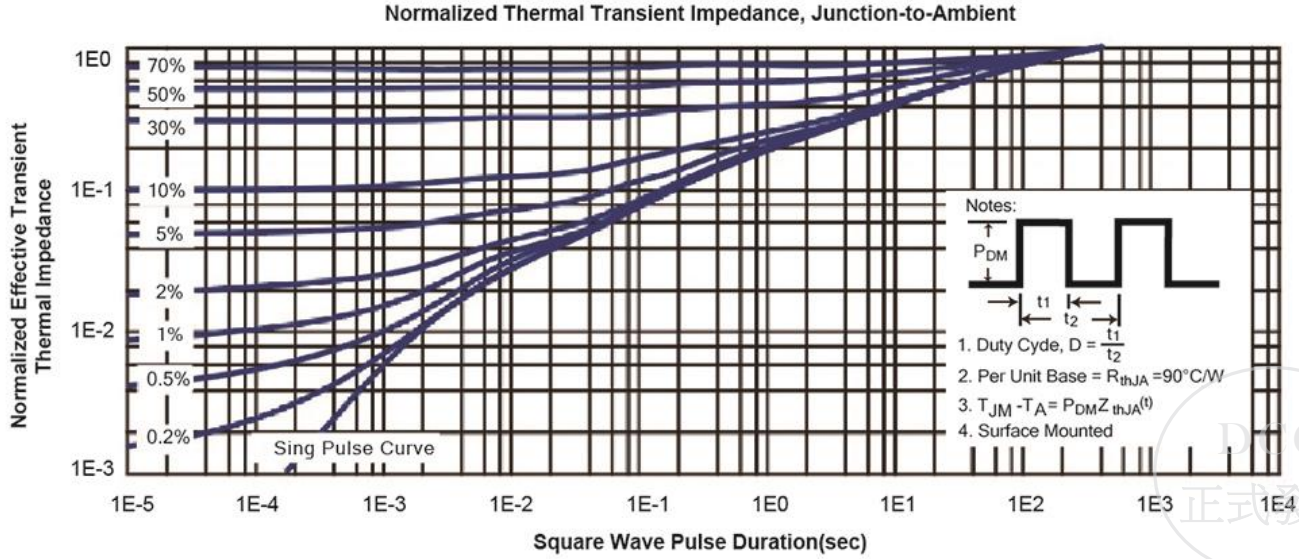
Body-diode characteristics



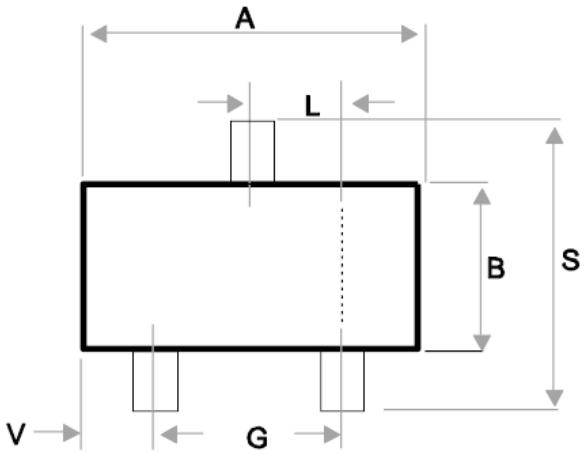
Maximum Forward Biased Safe Operating Area

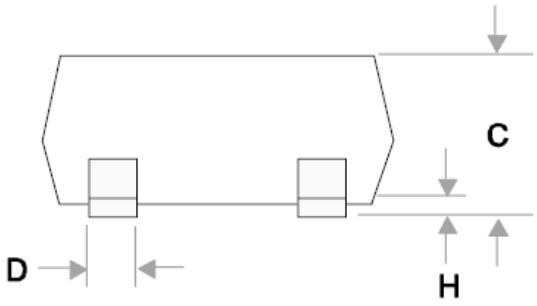


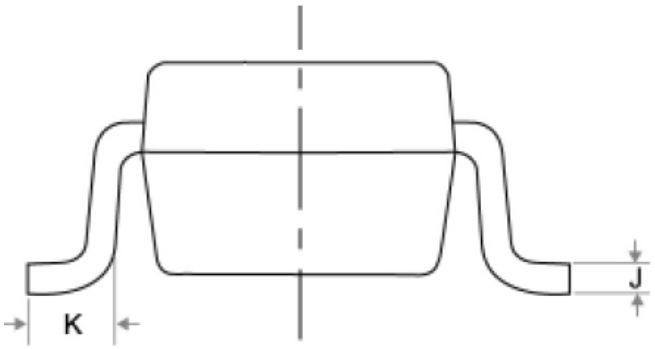
Normalized Thermal Transient Impedance, Junction-to-Ambient



大 SOT-23 Package







Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	2.8	3.05
B	1.5	1.75
C	0.9	1.3
D	0.35	0.5
G	1.8	2
H	0	0.15
J	0.1	0.2
K	0.35	0.6
L	0.85	1.05
S	2.6	3
V	0.375	0.675