N-Channel 20-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2318-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 34m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 45m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

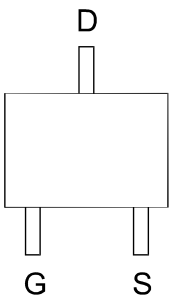
APPLICATIONS

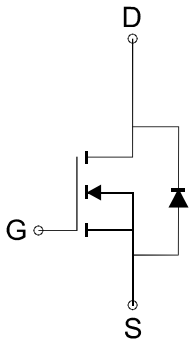
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





N-Channel MOSFET

Ordering Information: ME2318-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	5 sec	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	±12		V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	3.6	3.0	A
	T_A=70℃		2.8	2.4	
Pulsed Drain Current		I_{DM}	10		A
Maximum Body-Diode Continuous Current		I_S	1.6		A
Maximum Power Dissipation	T_A=25℃	P_D	1.25	0.75	W
	T_A=70℃		0.8	0.48	
Operating Junction Temperature		T_J	-55 to 150		℃
Storage Temperature Range		T_{stg}	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	64	℃/W
			Steady State	96	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	61		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel 20-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

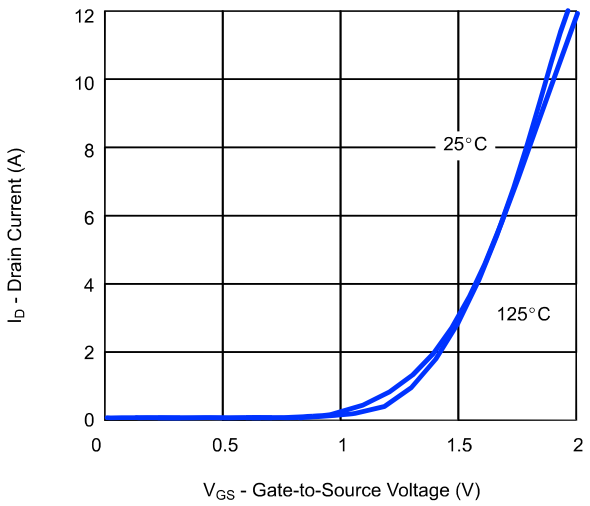
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.6		1.2	V
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			1.5	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=4.5V, I_D= 3.6A		26	34	mΩ
		V_{GS}=2.5V, I_D= 3.1A		35	45	
V_{SD}	Diode Forward Voltage	I_S=1.6A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=3.6A		9.7		nC
Qgs	Gate-Source Charge			2.6		
Qgd	Gate-Drain Charge			2.8		
Ciss	Input Capacitance	V_{DS}=10V, V_{GS}=0V,f=1MHz		570		pF
Coss	Output Capacitance			100		
Crss	Reverse Transfer Capacitance			30		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=10V, R_L =10Ω V_{GS}=4.5V, R_G=6Ω I_D=1.0A		10		ns
t_r	Turn-On Rise Time			35		
$t_{d(off)}$	Turn-Off Delay Time			40		
t_f	Turn-Off Fall Time			4.2		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

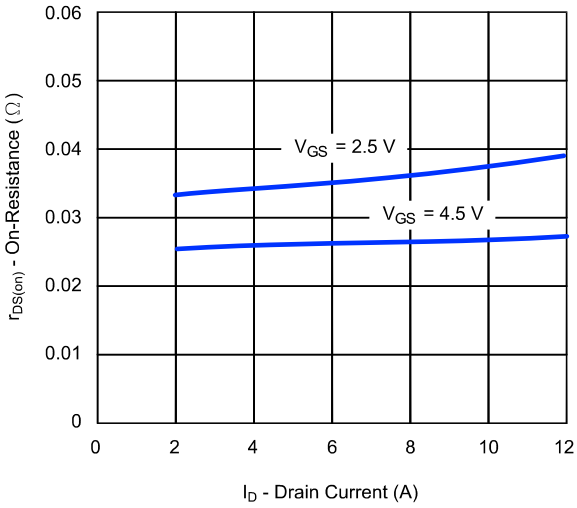
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J =25℃ Noted)

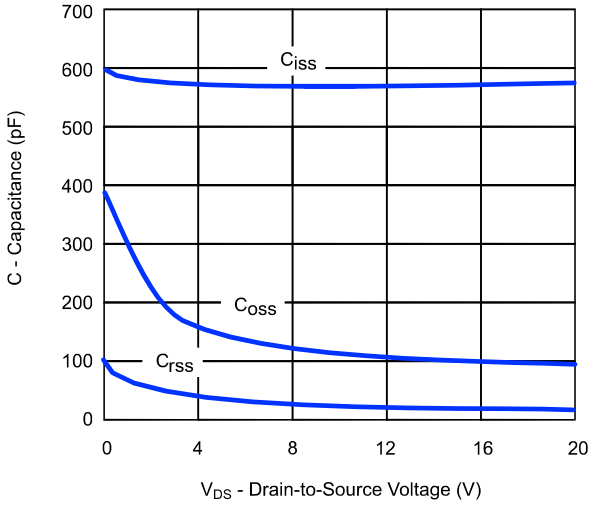
Transfer Characteristics



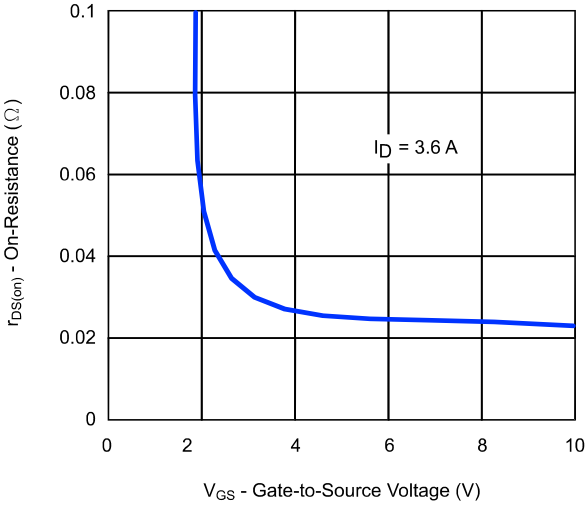
On-Resistance vs. Drain Current



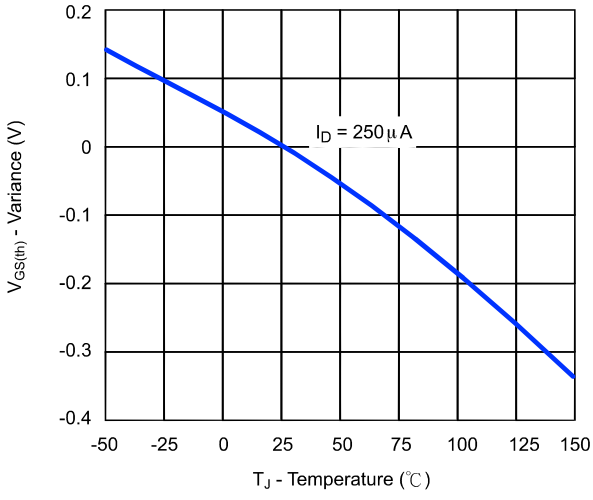
Capacitance



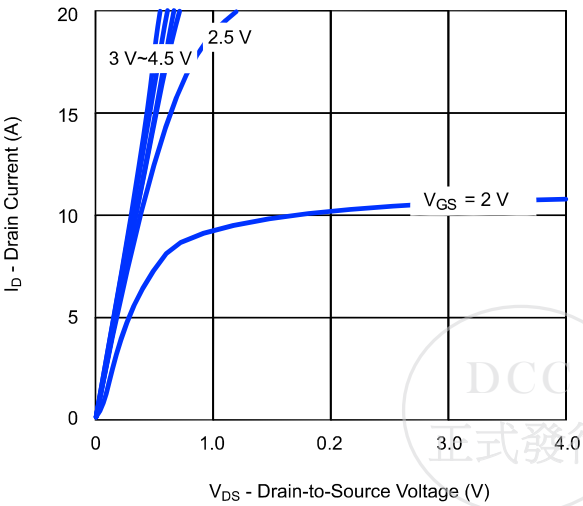
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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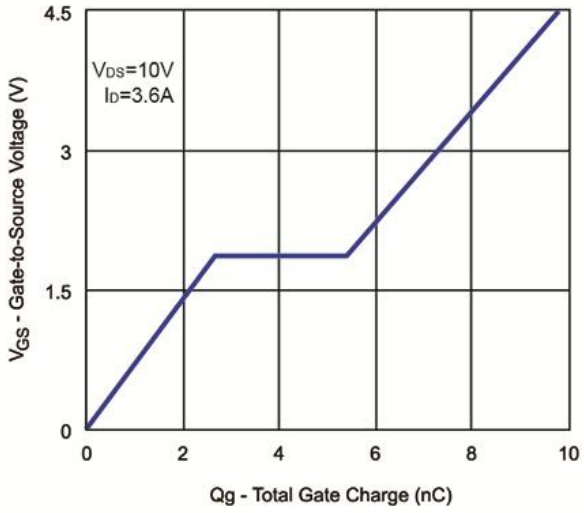
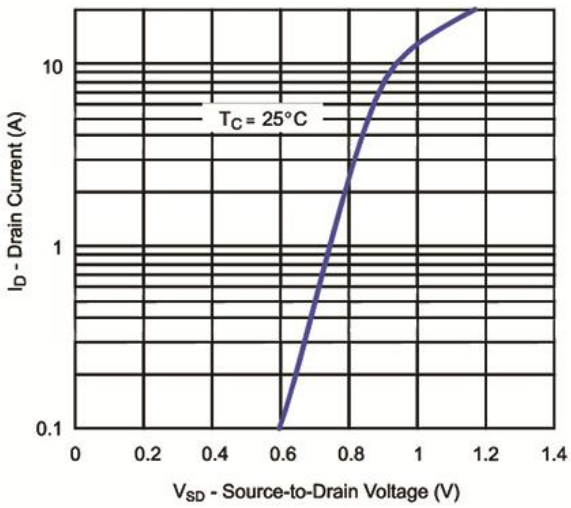
Typical Characteristics (T_J =25℃ Noted)

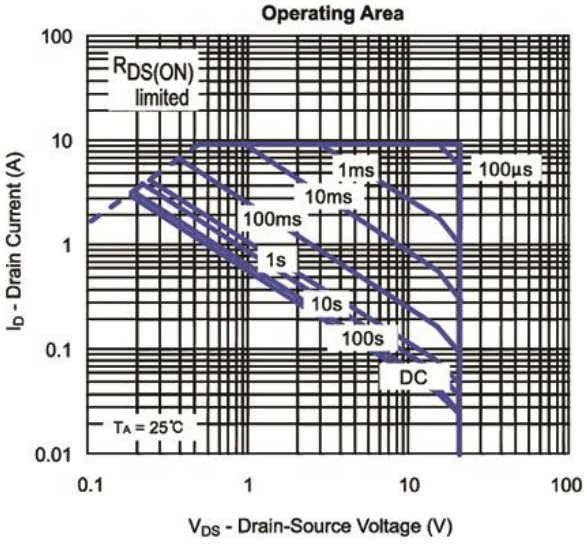
Gate Charge



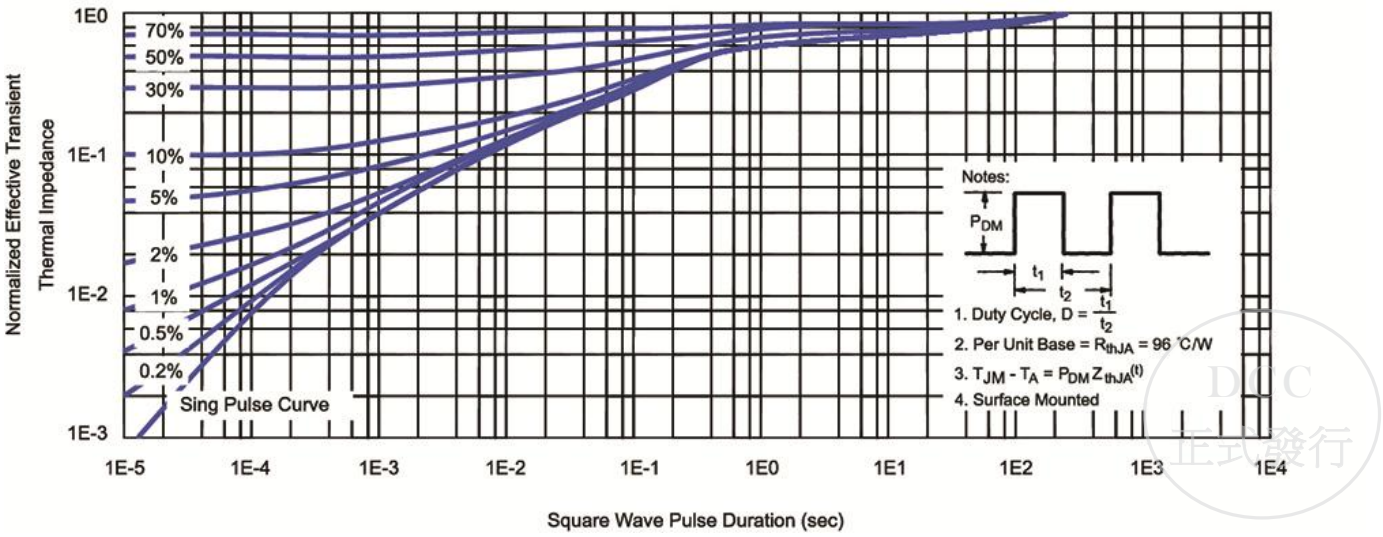
On-Resistance vs. Drain Current



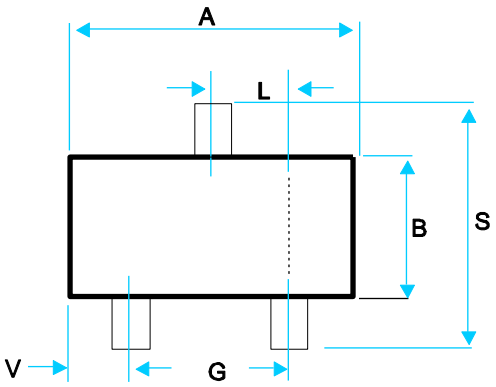
Maximum Forward Biased Safe Operating Area

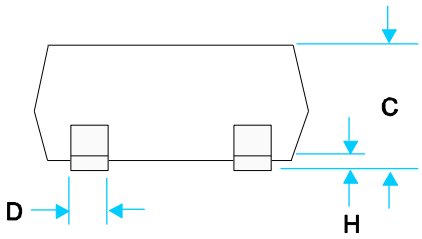


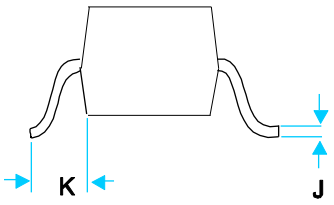
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	2.80	3.1
B	1.20	1.7
C	0.89	1.3
D	0.37	0.50
G	1.78	2.04
H	0.013	0.15
J	0.085	0.2
K	0.45	0.7
L	0.89	1.02
S	2.10	3
V	0.45	0.60