

N-Channel 20V (D-S) MOSFET , ESD Protection

GENERAL DESCRIPTION

The ME2320D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

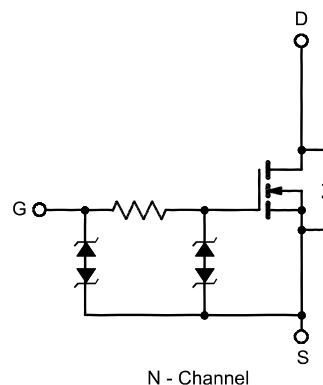
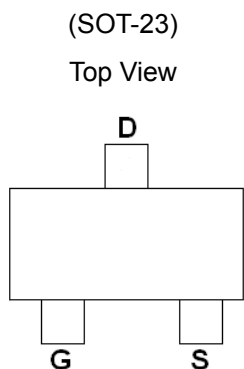
FEATURES

- R_{DS(ON)}=21m @V_{GS}=4.5V
- R_{DS(ON)}=25 m @V_{GS}=2.5V
- R_{DS(ON)}=33 m @V_{GS}=1.8V
- Super high density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION



Ordering Information:ME2320D(Pb-Free)

ME2320D-G(Green product-Halogen free)

Absolute Maximum Ratings (T_A=25 Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±8	V
Continuous Drain Current	I _D	T _A =25	6.4
		T _A =70	5.1
Pulsed Drain Current	I _{DM}	26	A
Maximum Power Dissipation	P _D	T _A =25	1.4
		T _A =70	0.9
Operating Junction Temperature	T _J	-55 to 150	
Thermal Resistance-Junction to Ambient*	R _{θJA}	90	/W

* The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_A = 25 Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.4		1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±4.5V			±1	μA
		V _{DS} =0V, V _{GS} =±8V			±10	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =4.5V, I _D = 6.5A		17	21	m
		V _{GS} =2.5V, I _D = 5.5A		20	25	
		V _{GS} =1.8V, I _D = 5A		25	33	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.6	1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =4.5, I _D =6.5A		10		nC
Q _{gs}	Gate-Source Charge			0.9		
Q _{gd}	Gate-Drain Charge			3		
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1MHz		150		pF
C _{oss}	Output Capacitance			95		
C _{rss}	Reverse Transfer Capacitance			25		
t _{d(on)}	Turn-On Delay Time	V _{DS} =10V, R _L = 1.5 V _{GS} =5V, R _{GEN} =3		250		ns
t _r	Turn-On Rise Time			420		
t _{d(off)}	Turn-Off Delay Time			3950		
t _f	Turn-Off Fall Time			3700		

Notes: a. Pulse test; pulse width 300us, duty cycle 2%

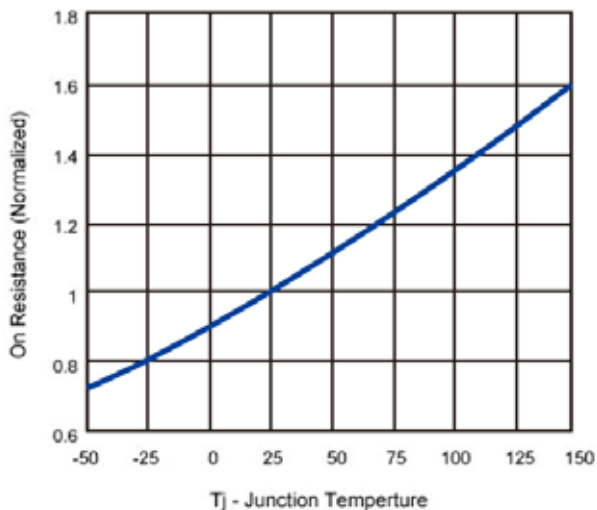
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



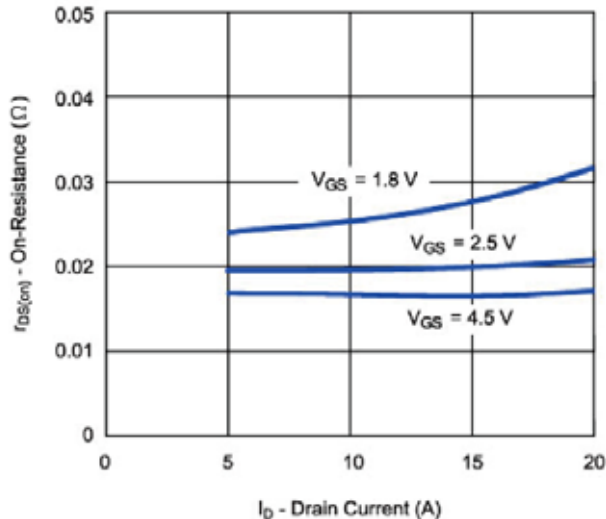
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Typical Characteristics (T_J =25 Noted)

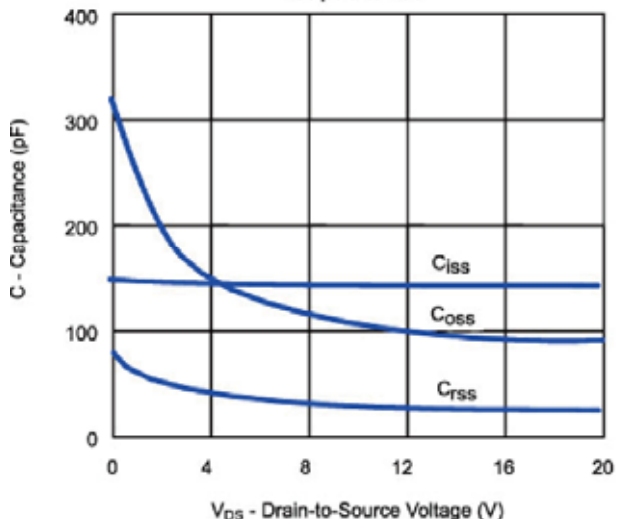
On Resistance vs. Junction Temperature



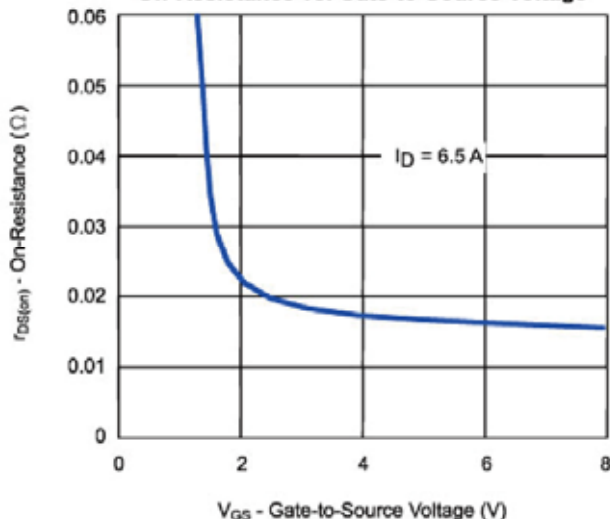
On-Resistance vs. Drain Current



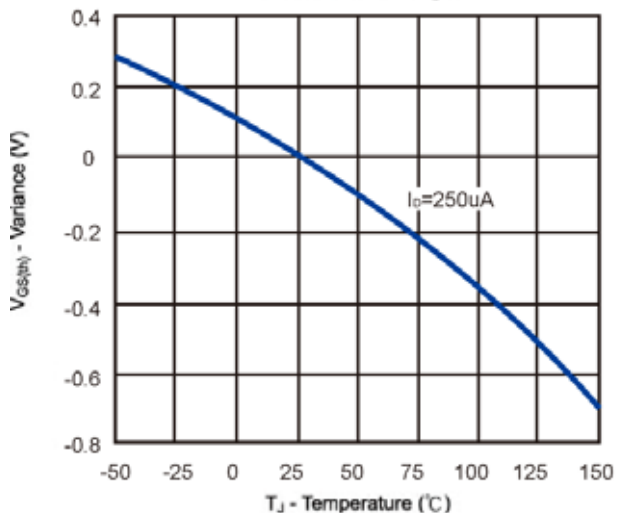
Capacitance



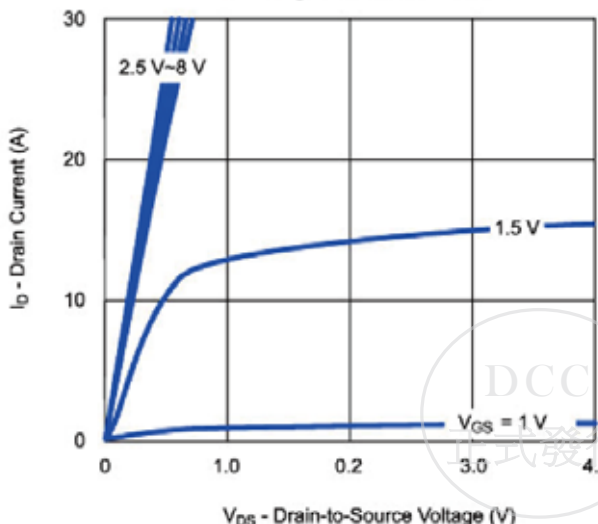
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

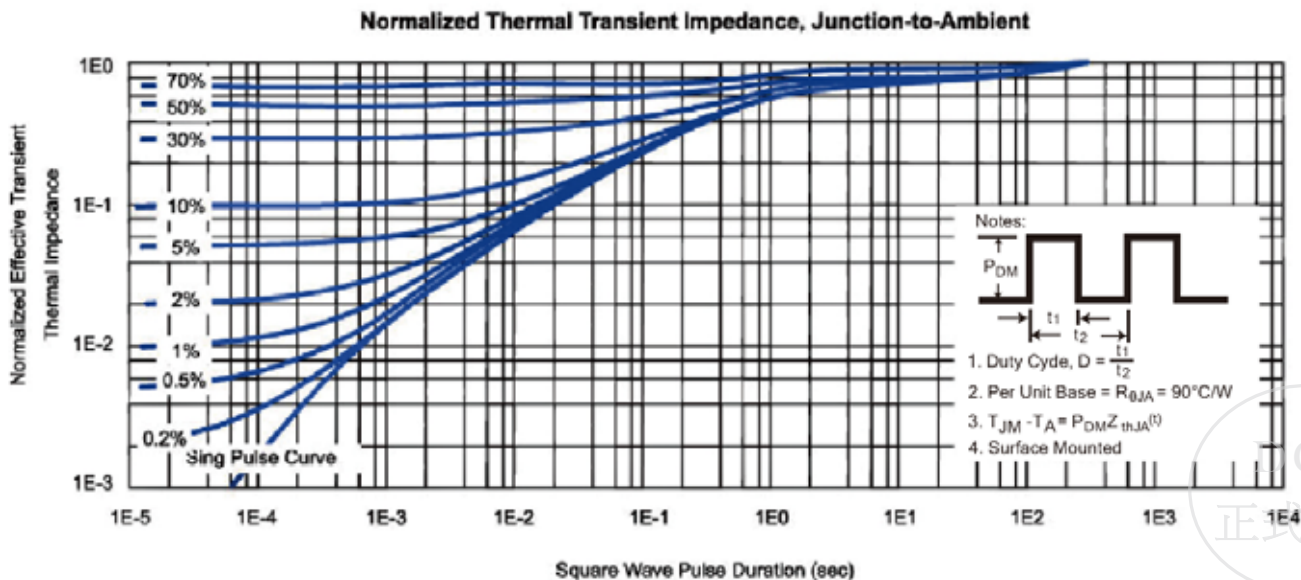
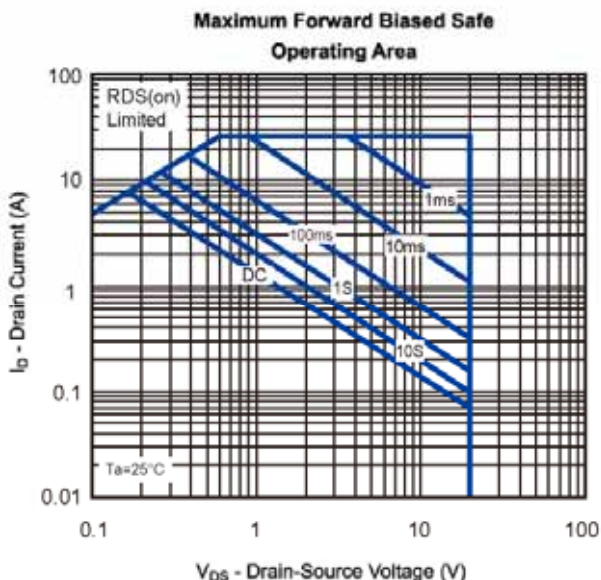
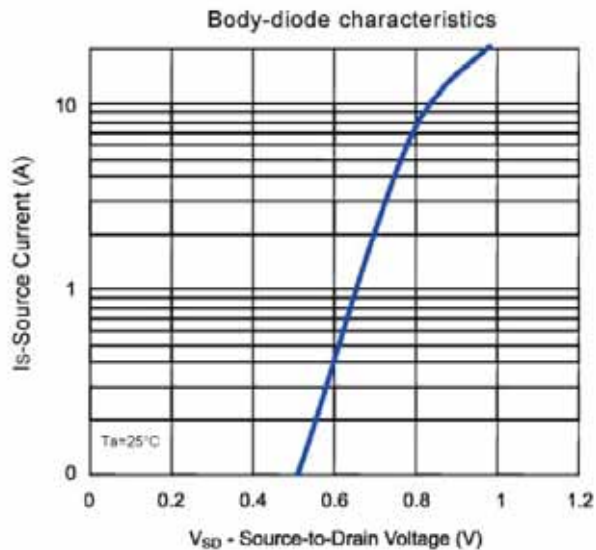
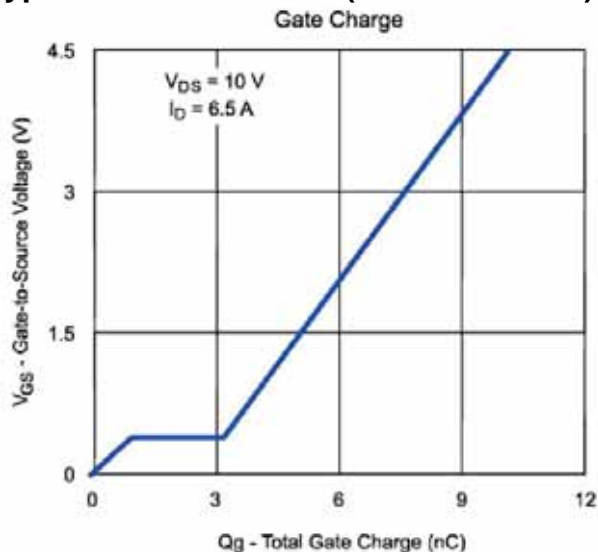


On-Region Characteristics

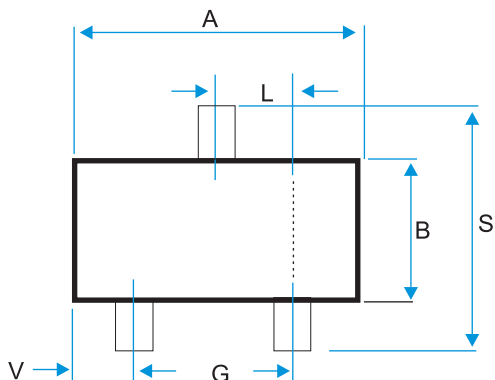


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Typical Characteristics (T_J =25 Noted)



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

