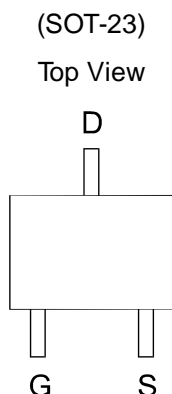


P-Channel 20-V (D-S) MOSFET , ESD Protection

GENERAL DESCRIPTION

The ME2323D(-G) is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

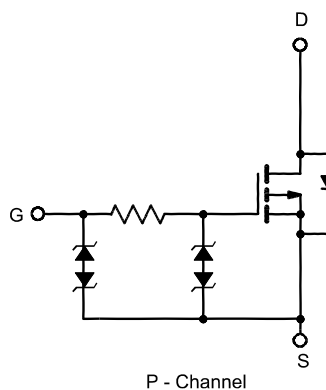


FEATURES

- $R_{DS(ON)} \leq 50m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 65m\Omega @ V_{GS} = -2.5V$
- $R_{DS(ON)} \leq 75m\Omega @ V_{GS} = -1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P - Channel

Ordering Information: ME2323D (Pb-free)

ME2323D-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain	I_D	$T_A = 25^\circ C$	-4.2
		$T_A = 70^\circ C$	-3.3
Pulsed Drain Current	I_{DM}	-17	A
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	1.4
		$T_A = 70^\circ C$	0.9
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	90	$^\circ C/W$

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P-Channel 20-V (D-S) MOSFET , ESD Protection

Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-0.25	-0.5	-1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±4.5V			±5	μA
		V _{DS} =0V, V _{GS} =±8V			±10	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-16V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-4.5V, I _D = -4.0A		45	50	mΩ
		V _{GS} =-2.5V, I _D = -3.0A		52	65	
		V _{GS} =-1.8V, I _D = -2.0A		60	75	
V _{SD}	Diode Forward Voltage	I _S =-1.0A, V _{GS} =0V		-0.78	-1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-10V, V _{GS} =-4.5V, I _D =-4A		10.5		nC
Q _{gs}	Gate-Source Charge			0.5		
Q _{gd}	Gate-Drain Charge			3		
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, f=1MHz		220		pF
C _{oss}	Output Capacitance			95		
C _{rss}	Reverse Transfer Capacitance			30		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-10V, R _L =2.5Ω R _{GEN} =3Ω, V _{GS} =-4.5V		560		ns
t _r	Turn-On Rise Time			4000		
t _{d(off)}	Turn-Off Delay Time			400		
t _f	Turn-Off Fall Time			4000		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

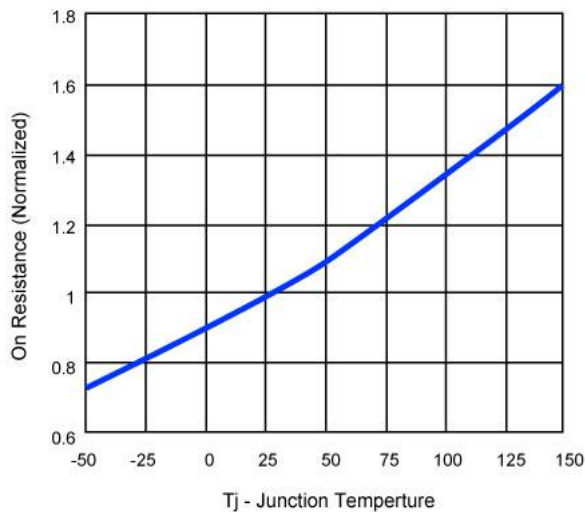
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

DCC
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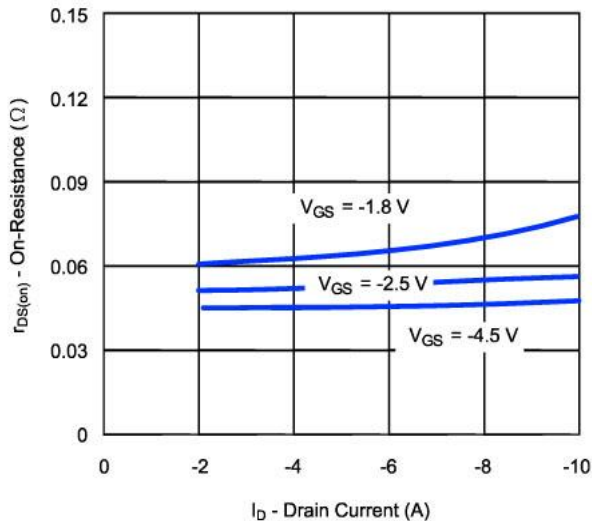
P-Channel 20-V (D-S) MOSFET , ESD Protection

Typical Characteristics (T_J = 25°C Noted)

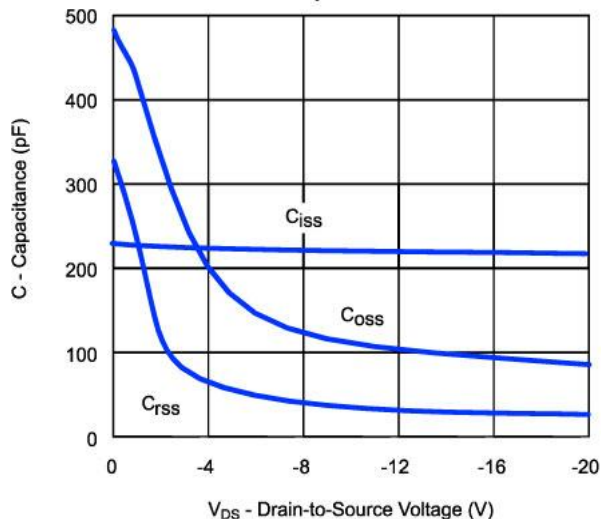
On Resistance vs. Junction Temperature



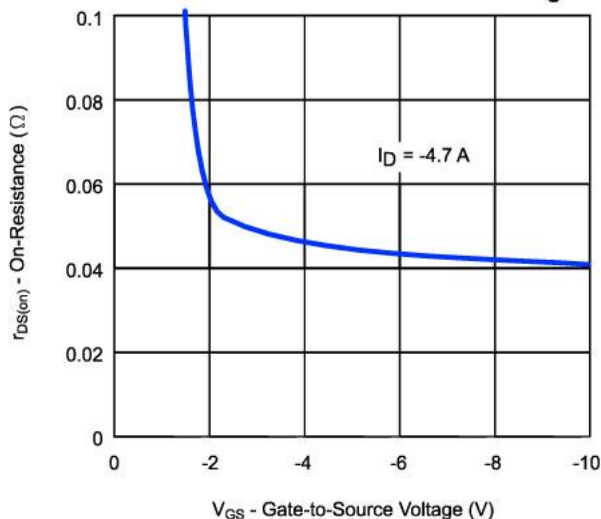
On-Resistance vs. Drain Current



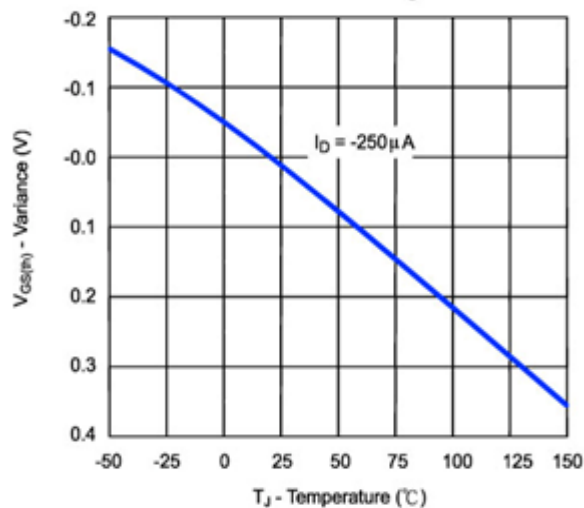
Capacitance



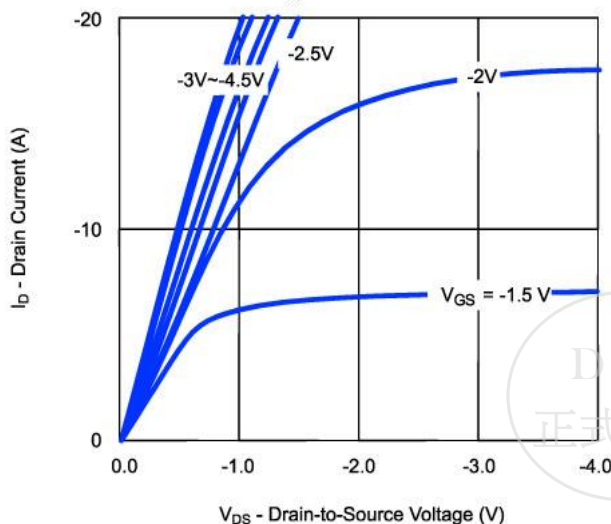
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

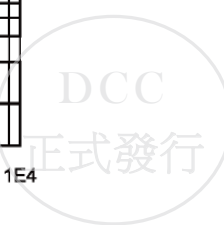
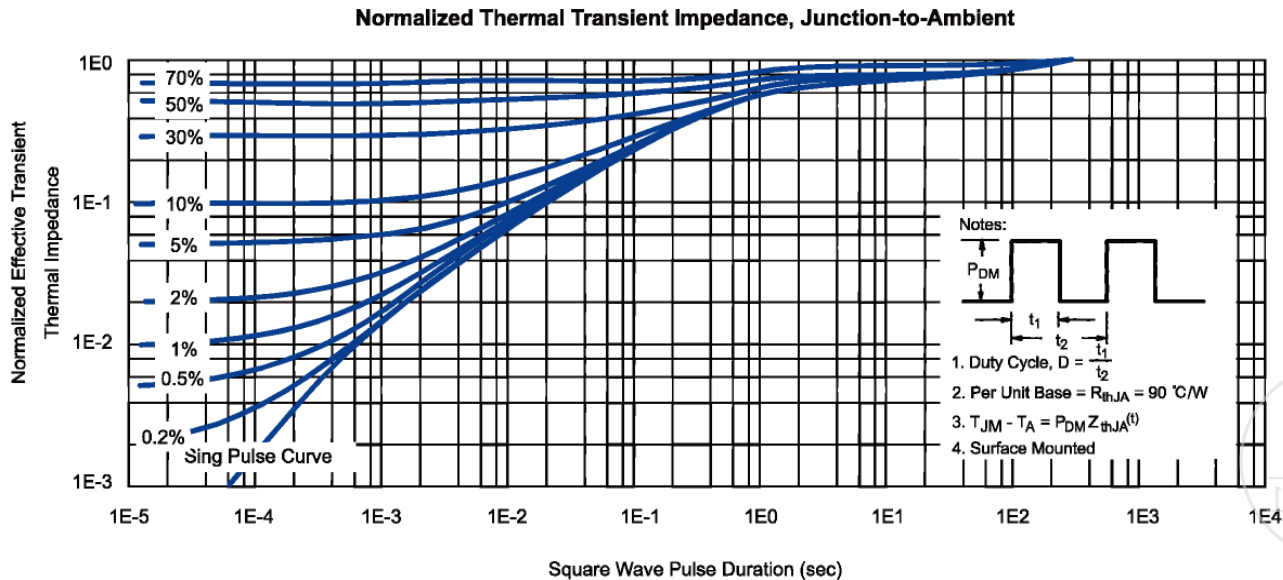
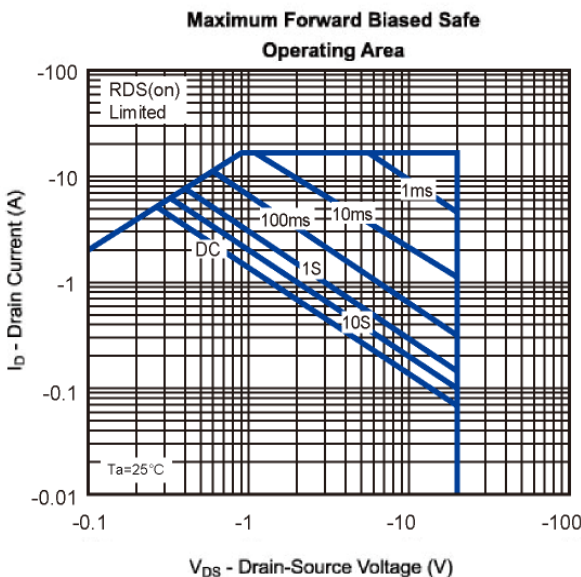
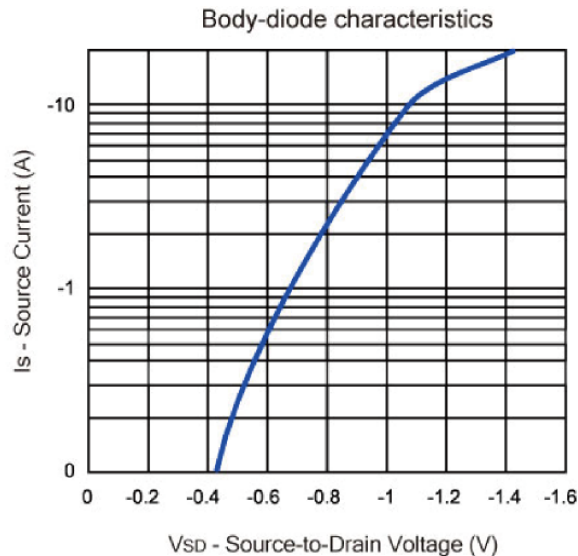
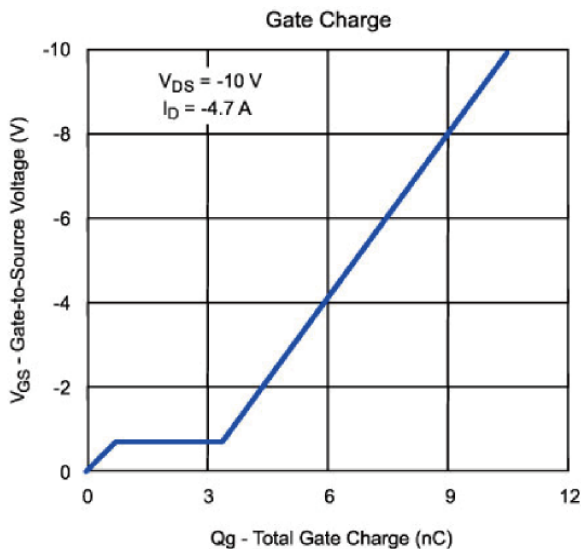


On-Region Characteristics

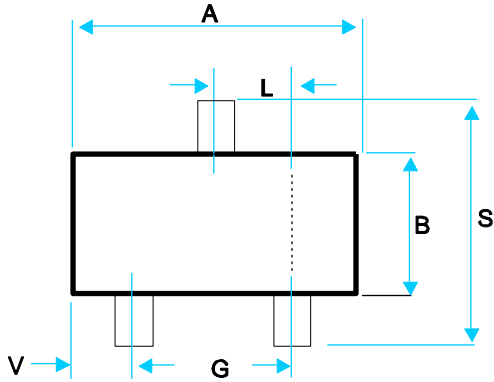


P-Channel 20-V (D-S) MOSFET , ESD Protection

Typical Characteristics (T_J = 25°C Noted)



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

