

P-Channel 20V (D-S) MOSFET

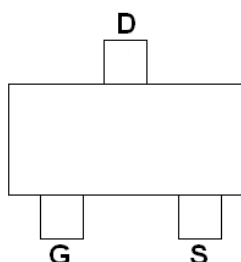
GENERAL DESCRIPTION

The ME2333 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(SOT-23)

Top View



Ordering Information: ME2333 (Pb-free)

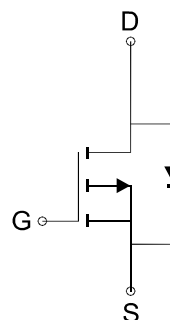
ME2333 -G (Green product-Halogen free)

FEATURES

- $R_{DS(ON)} \leq 35m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 49m\Omega @ V_{GS} = -2.5V$
- $R_{DS(ON)} \leq 69m\Omega @ V_{GS} = -1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-5.1	A
	$T_A = 70^\circ\text{C}$		-4.1	
Pulsed Drain Current		I_{DM}	-21	A
Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	1.39	W
	$T_A = 70^\circ\text{C}$		0.89	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	$^\circ\text{C/W}$

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J = 25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-0.3		-1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±12V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =-4.5V, I _D = -4.5A		27	35	mΩ
		V _{GS} =-2.5V, I _D = -2.5A		35	49	
		V _{GS} =-1.8V, I _D = -2A		49	69	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.62	-1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-10V, V _{GS} =-4.5V, I _D =-8A		12.6		nC
Q _{gs}	Gate-Source Charge			2.9		
Q _{gd}	Gate-Drain Charge			4		
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, f=1MHz		1050		pF
C _{oss}	Output Capacitance			122		
C _{rss}	Reverse Transfer Capacitance			120		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-10V, R _L =10Ω R _{GEN} =3Ω, V _{GS} =-4.5V		56.3		ns
t _r	Turn-On Rise Time			31.5		
t _{d(off)}	Turn-Off Delay Time			86.1		
t _f	Turn-Off Fall Time			32.7		

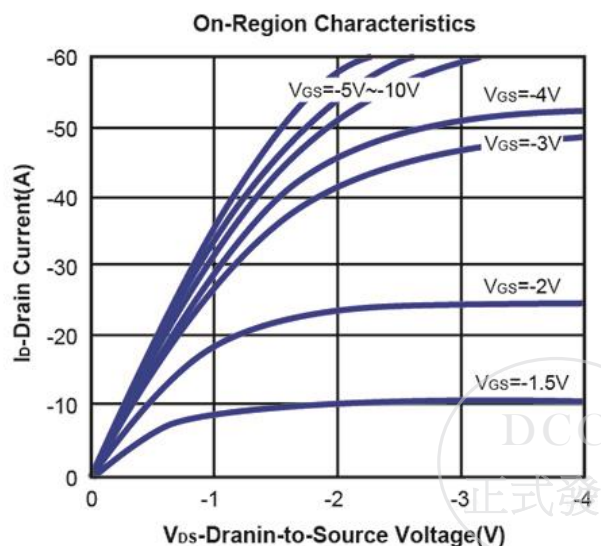
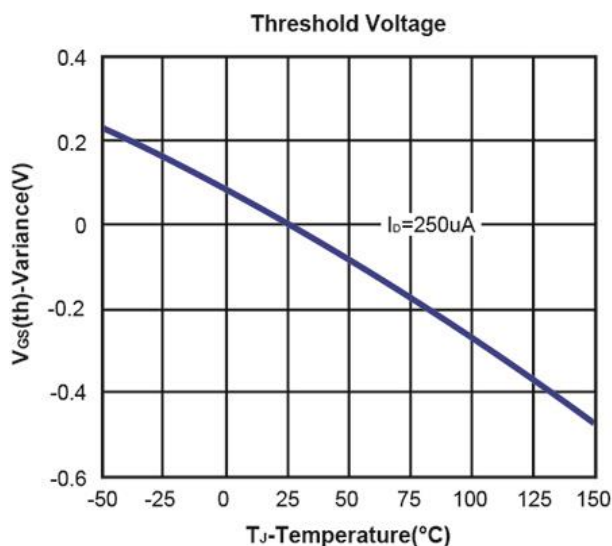
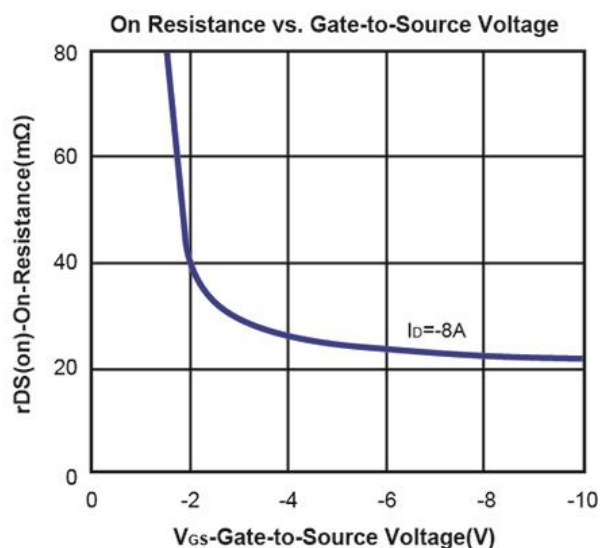
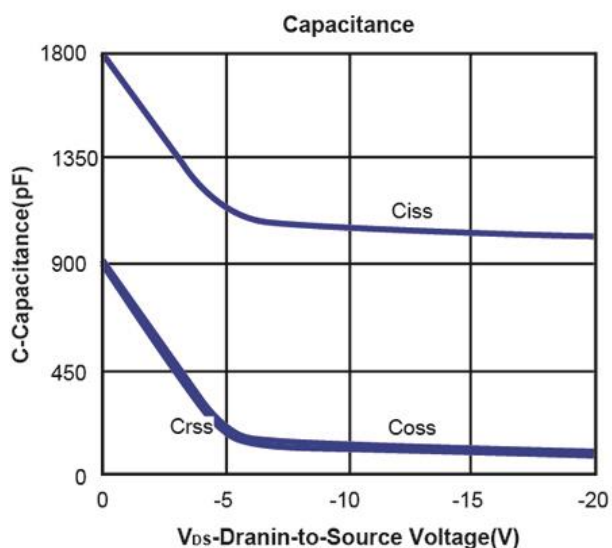
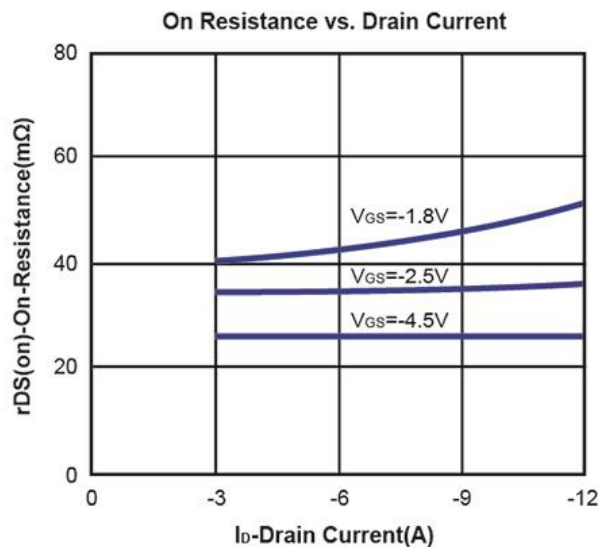
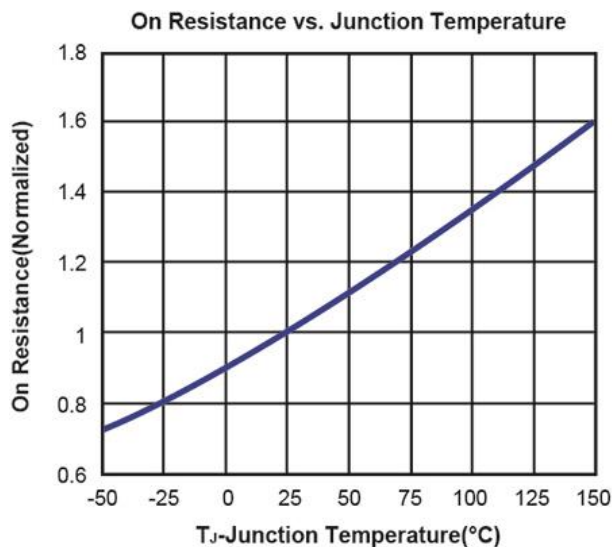
Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



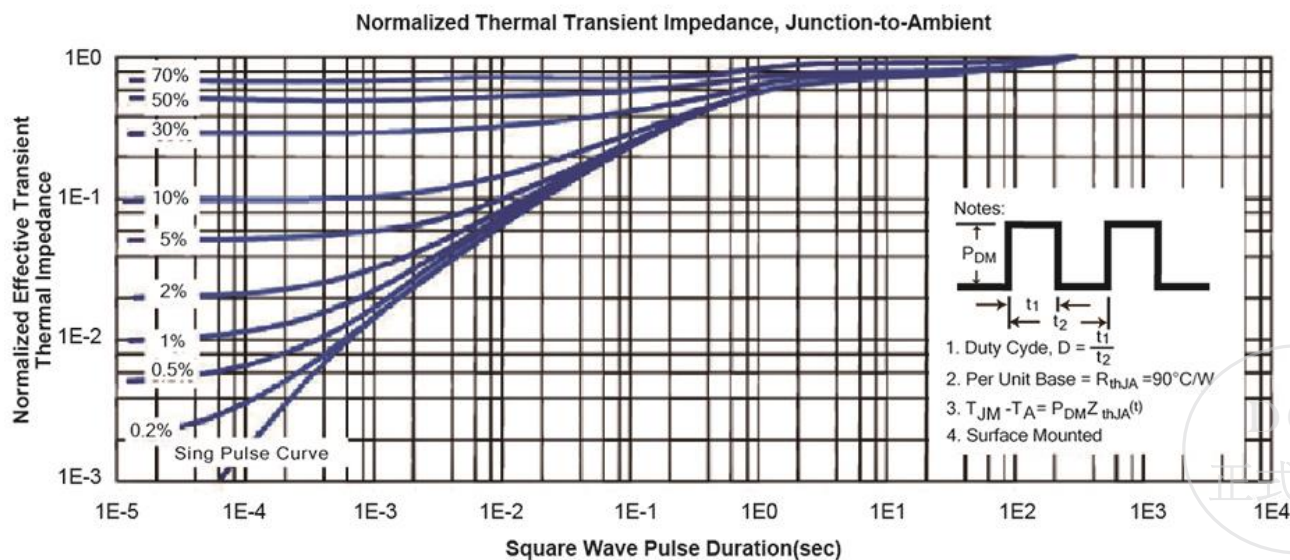
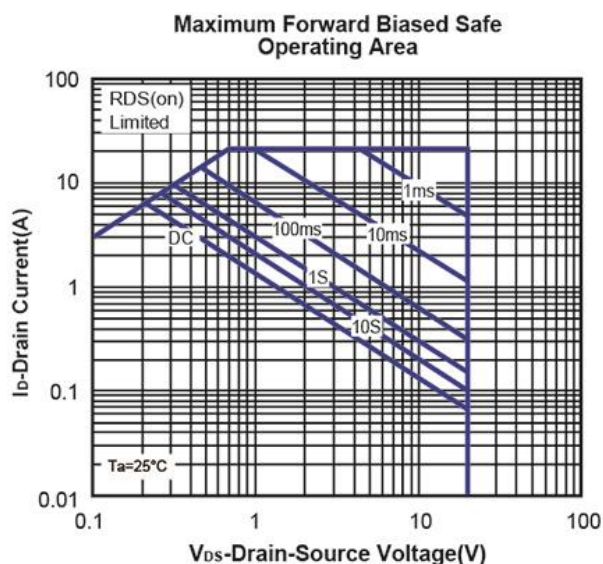
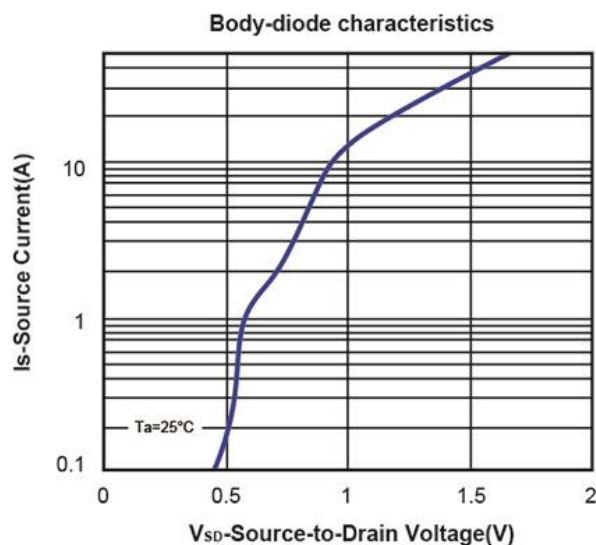
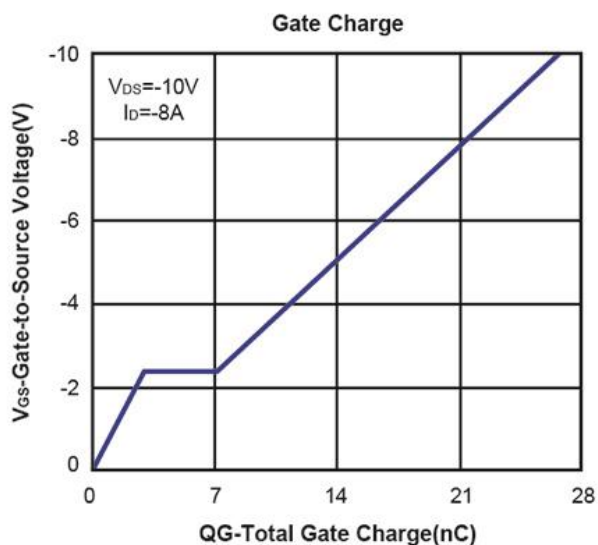
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Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

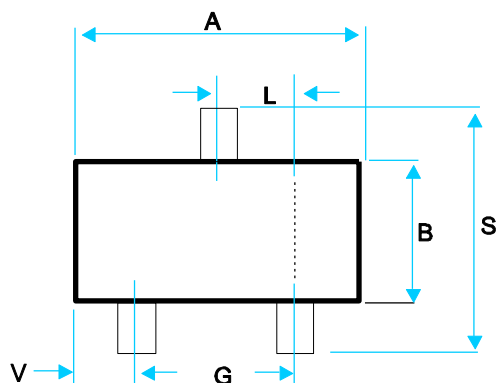


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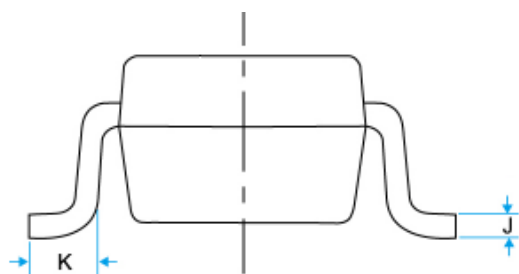
Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)



大 SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60



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