

P-Channel Enhancement Mode Mosfet

GENERAL DESCRIPTION

The ME2345 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

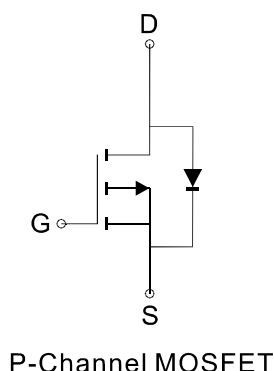
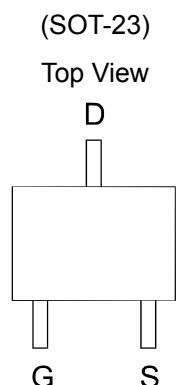
FEATURES

- $R_{DS(ON)} \leq 65m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 75m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 105m\Omega @ V_{GS} = -2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



Ordering Information: ME2345 (Pb-free)

ME2345-G (Green product-Halogen free) (Green)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V _{DSS}	-30		V
Gate-Source Voltage		V _{GSS}	±12		V
Continuous Drain Current(T _j =150°C)*	T _A =25°C	I _D	-3.65		A
	T _A =70°C		-2.9		
Pulsed Drain Current		I _{DM}	-15		A
Maximum Power Dissipation*	T _A =25°C	P _D	1.4		W
	T _A =70°C		0.9		
Operating Junction Temperature		T _J	-55 to 150		°C
Thermal Resistance-Junction to Ambient*		R _{θJA}	T ≤ 10 sec	90	°C/W
			Steady State	120	

* The device mounted on 1in² FR4 board with 2 oz copper, the current rating is based on $t \leq 10 \text{ sec}$ $R_{\theta JA}$ rating.

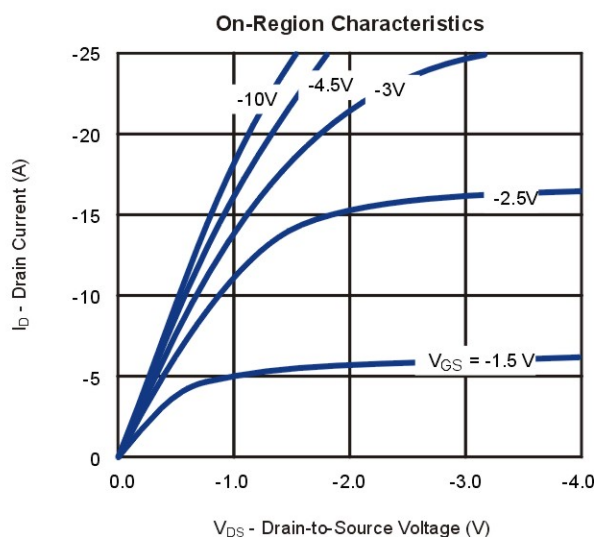
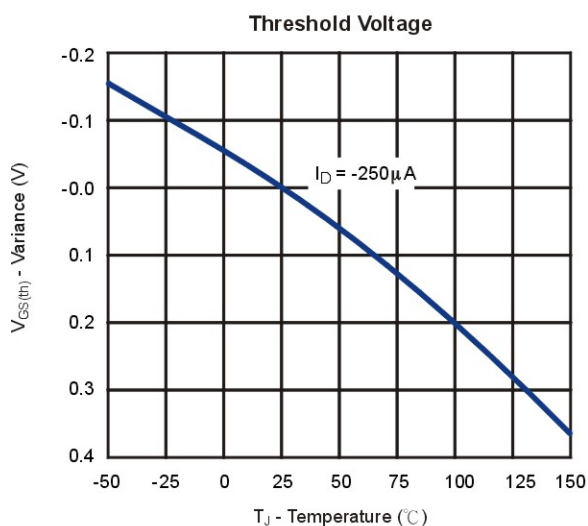
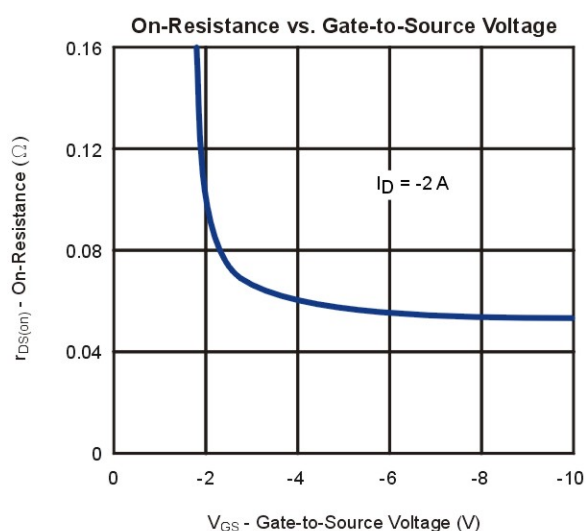
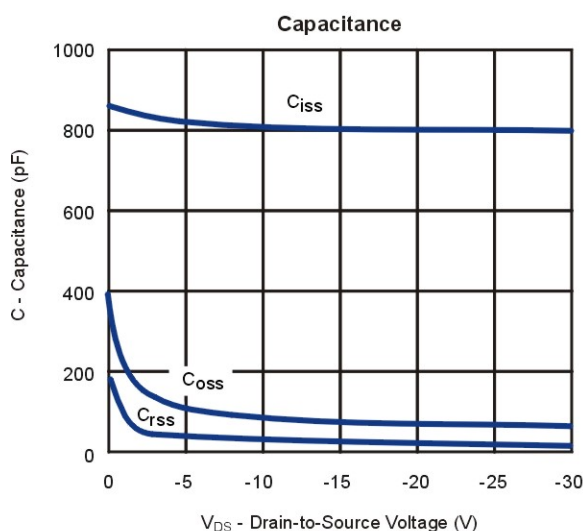
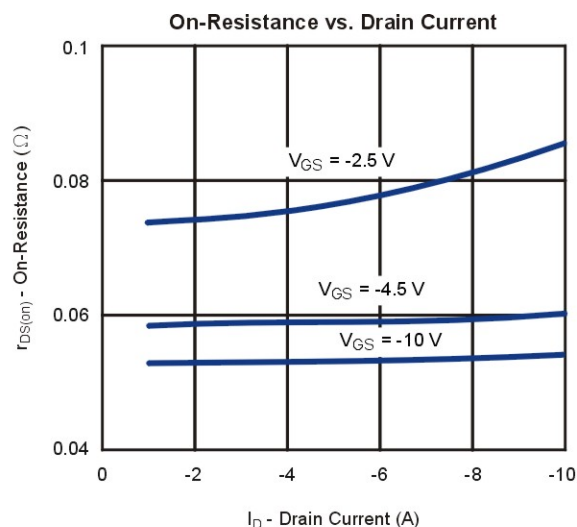
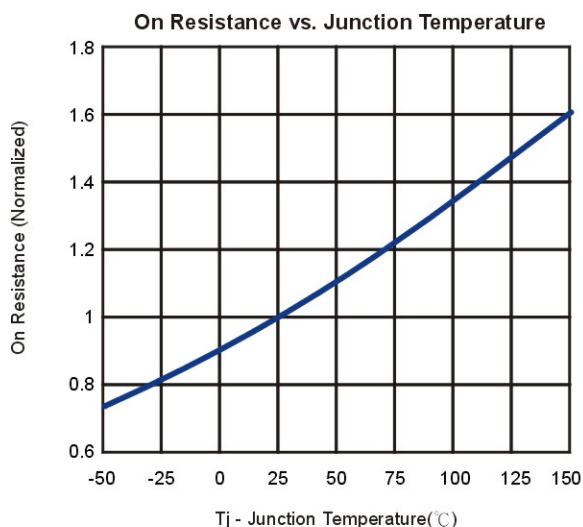
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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

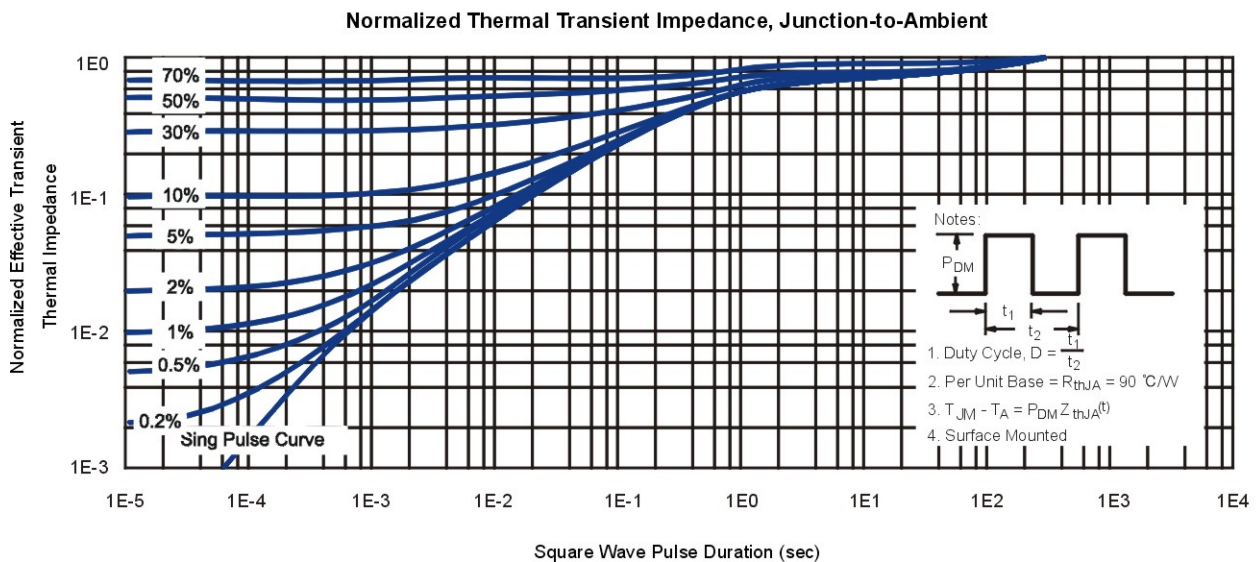
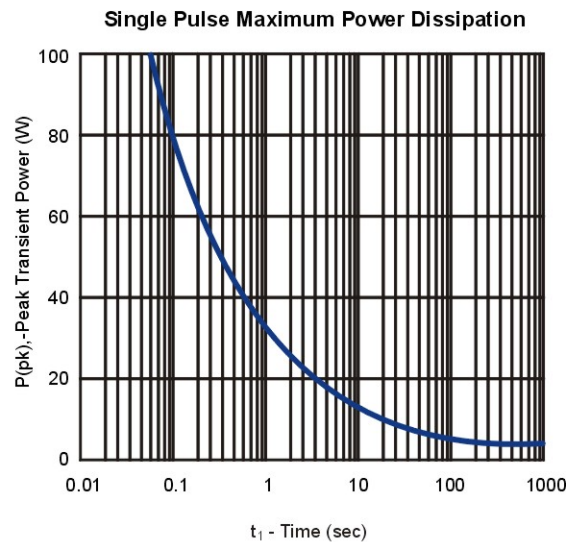
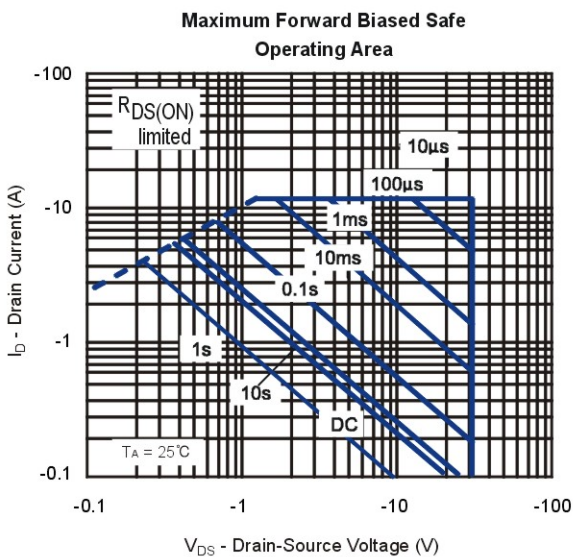
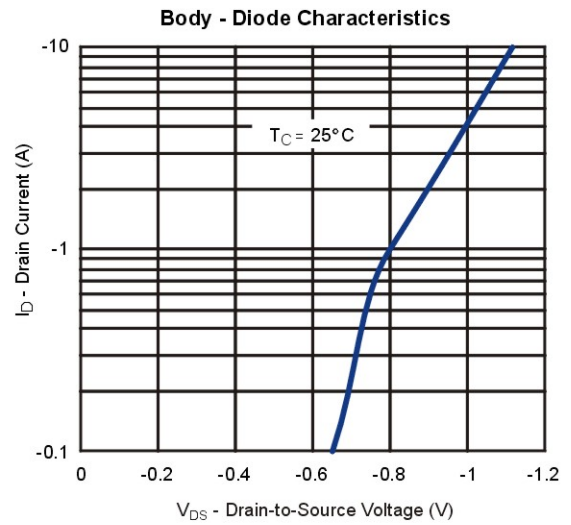
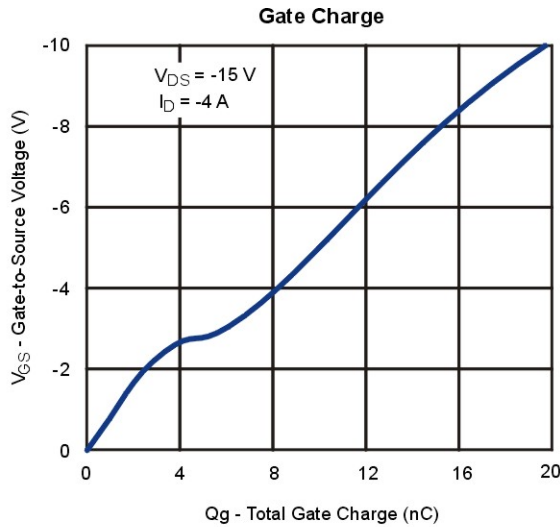
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V(BR)DSS	Drain-Source Breakdown Voltage	VGS=0V, ID=-250 μ A	-30			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=-250 μ A	-0.7		-1.3	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±12V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=-24V, VGS=0V			-1	μ A
RDS(ON)	Drain-Source On-Resistance ^a	VGS=-10V, ID= -4.2A		53	65	m Ω
		VGS=-4.5V, ID= -4A		59	75	
		VGS=-2.5V, ID= -2A		74	105	
VSD	Diode Forward Voltage	IS=-1A, VGS=0V		-0.7	-1	V
DYNAMIC						
Qg	Total Gate Charge	VDS=-15V, VGS=-4.5V, ID=-4A		9.5		nC
Qgs	Gate-Source Charge			3		
Qgd	Gate-Drain Charge			2		
Rg	Gate-Resistance	VDS=0V, VGS=0V, F=1MHz		5.5		Ω
Ciss	Input Capacitance	VDS=-15V, VGS=0V, f=1MHz		800		pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			20		
td(on)	Turn-On Delay Time	VDS=-15V, RL =3.6 Ω RGEN=6 Ω , VGS=-10V		37		ns
tr	Turn-On Rise Time			23		
td(off)	Turn-Off Delay Time			46		
tf	Turn-Off Fall time			3		

Notes: a. Pulse test; pulse width $\leq$ 300us, duty cycle $\leq$ 2%

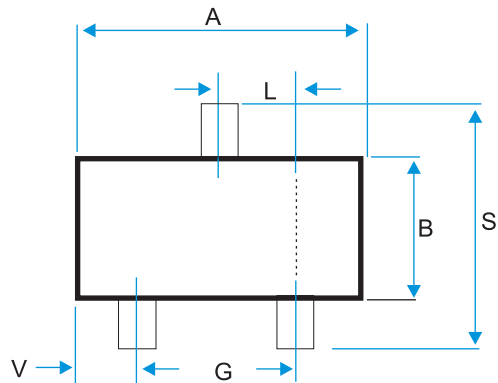
Typical Characteristics (T_J = 25°C Noted)



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SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

