P-Channel Enhancement Mode Mosfet

GENERAL DESCRIPTION

The ME2347 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 80m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 95m\Omega @ V_{GS}=-4.5V$
- $R_{DS(ON)} \leqq 120m\Omega @ V_{GS}=-2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

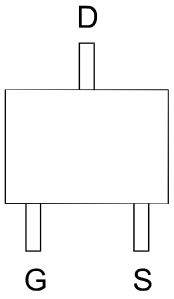
APPLICATIONS

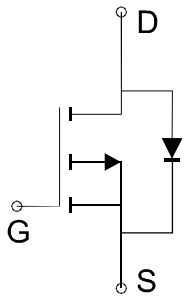
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





Ordering Information: ME2347(Pb-free)

ME2347-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	-3.3	A
	T_A=70℃		-2.6	
Pulsed Drain Current		I_{DM}	-13	A
Maximum Power Dissipation	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Storage Temperature Range		T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.7		-1.3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -2.6A		60	80	mΩ
		V_{GS}=-4.5V, I_D= -2A		70	95	
		V_{GS}=-2.5V, I_D= -1A		85	120	
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Qg	Total Gate Charge (-10V)	V_{DS}=-15, V_{GS}=-10V, I_D=-2.6A		19		nC
Qg	Total Gate Charge (-4.5V)			9		
Qgs	Gate-Source Charge			2.3		
Qgd	Gate-Drain Charge			2.1		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		720		pF
Coss	Output Capacitance			72		
Crss	Reverse Transfer Capacitance			23		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L =15Ω R_{GEN}=6Ω, V_{GS}=-10V		33		ns
t_r	Turn-On Rise Time			17		
$t_{d(off)}$	Turn-Off Delay Time			51		
t_f	Turn-Off Fall Time			4.4		

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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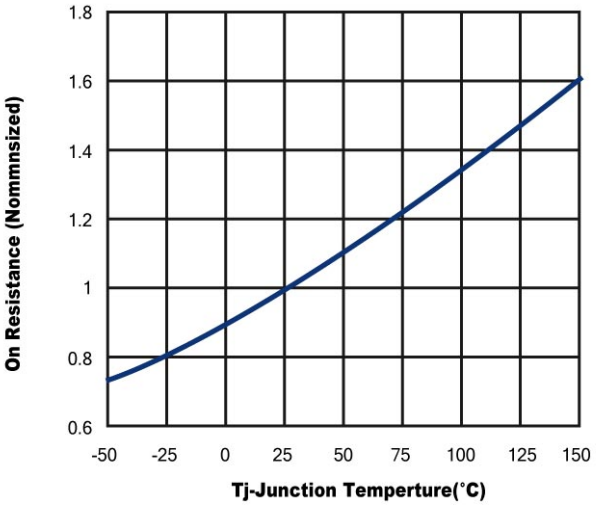
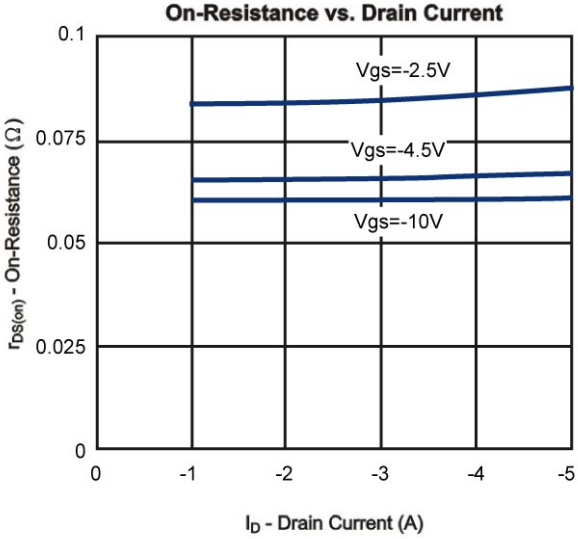
Typical Characteristics (T_J =25℃ Noted)

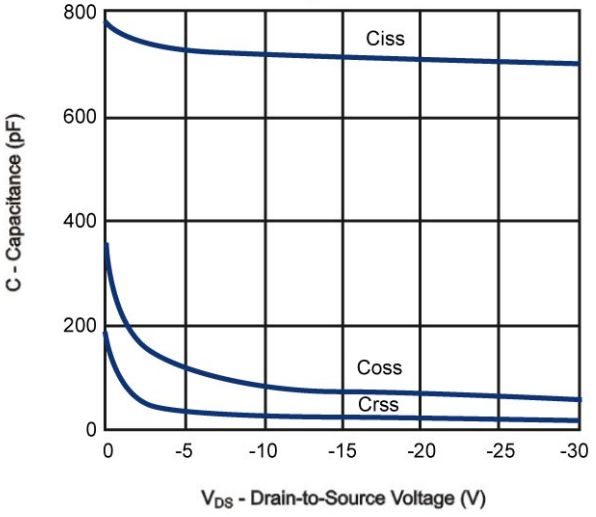
On Resistance vs. Junction Temperture



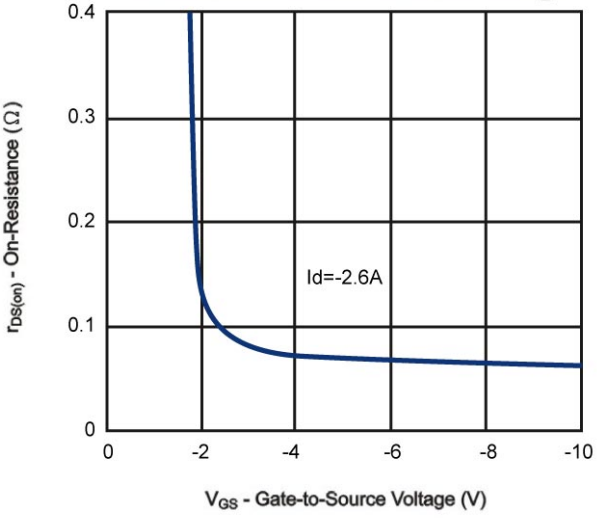
On-Resistance vs. Drain Current



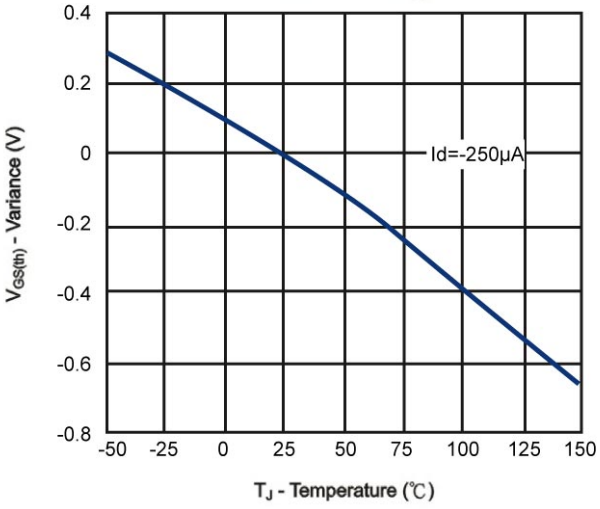
Capacitance



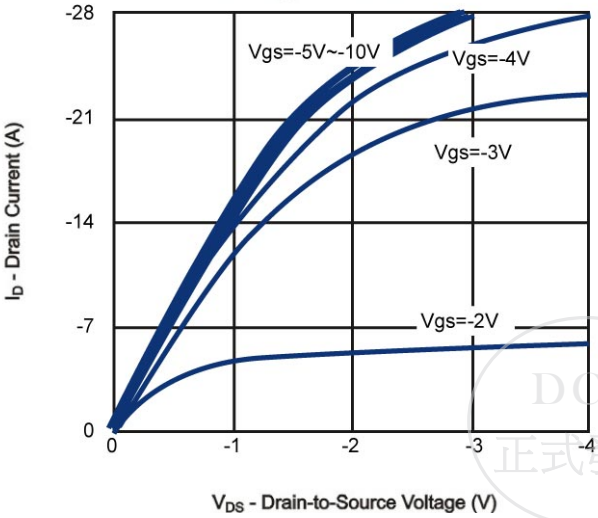
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



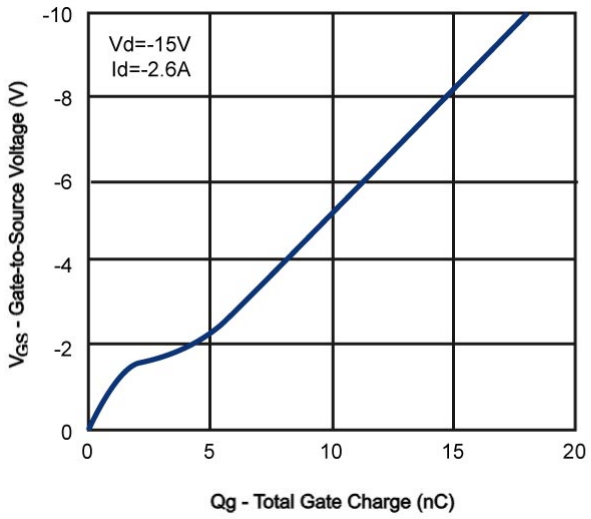
On-Region Characteristics



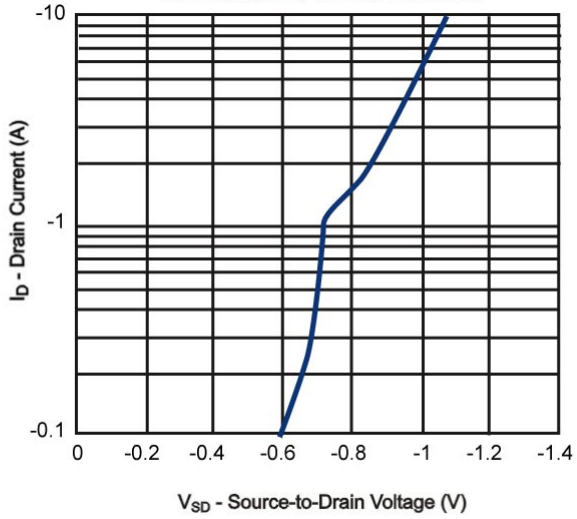
P-Channel Enhancement Mode Mosfet

Typical Characteristics (T_J =25℃ Noted)

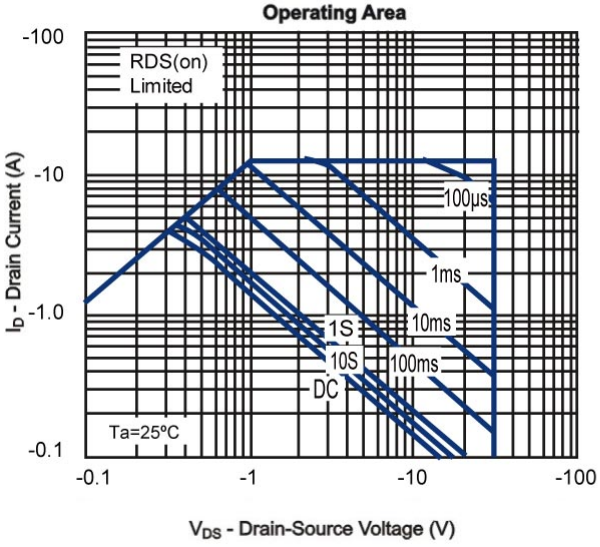
Gate Charge



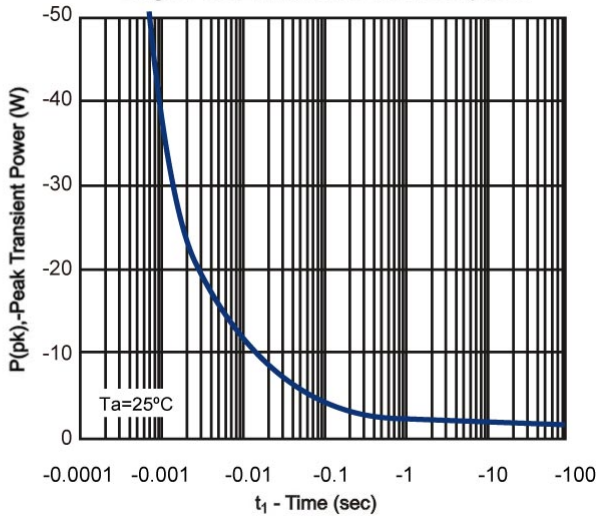
On-Resistance vs. Drain Current



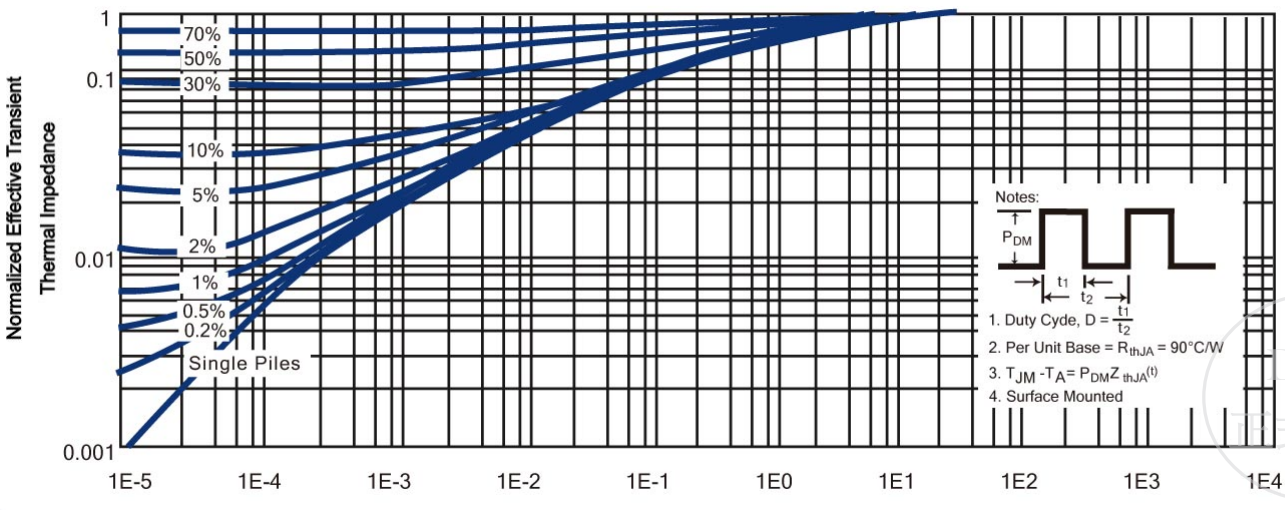
Maximum Forward Biased Safe Operating Area



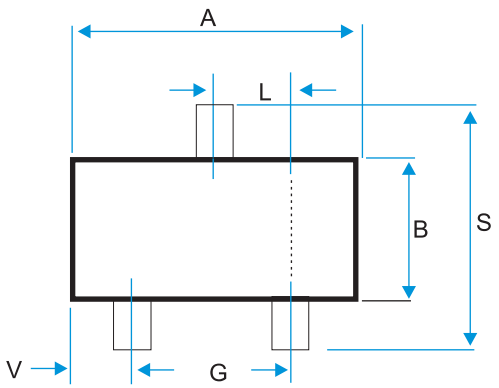
Single Pulse Maximum Power Dissipation

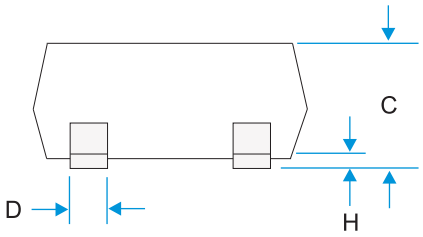


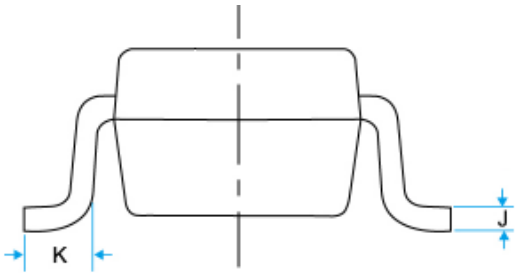
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60