

N-Channel 150-V (D-S) MOSFET

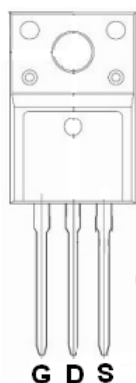
GENERAL DESCRIPTION

The ME25N15F is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

PIN CONFIGURATION

(TO-220F)

Top View

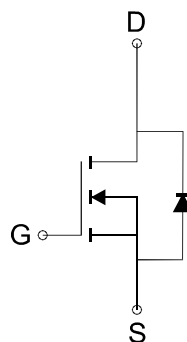


FEATURES

- $R_{DS(ON)} \leq 75m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



N-Channel MOSFET

Ordering Information: ME25N15F (Pb-free)

ME25N15F-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_c=25^\circ\text{C}$	I_D	21.0	A
	$T_c=70^\circ\text{C}$		17.6	
Pulsed Drain Current		I_{DM}	84.3	A
Maximum Power Dissipation	$T_c=25^\circ\text{C}$	P_D	66.6	W
	$T_c=70^\circ\text{C}$		46.6	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	2.25	$^\circ\text{C/W}$

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics ($T_c = 25^\circ\text{C}$ Unless Otherwise Specified)

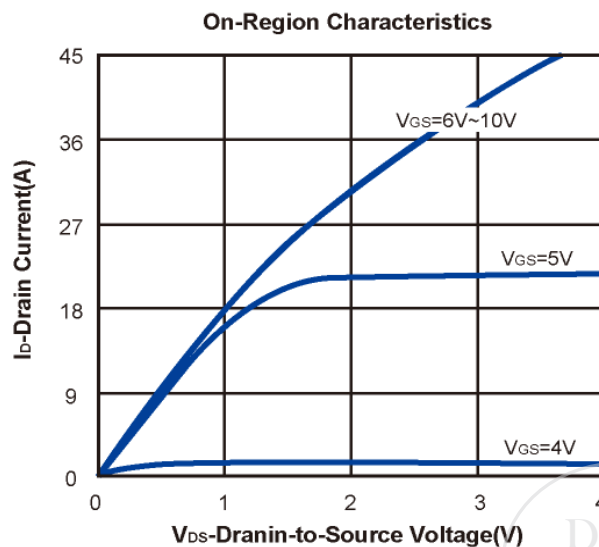
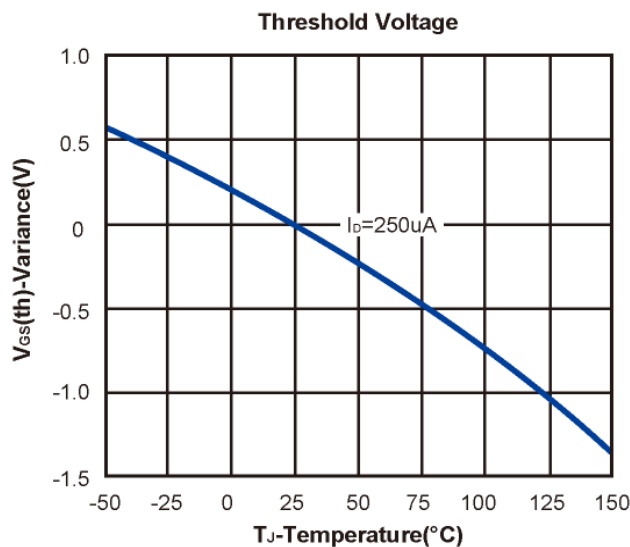
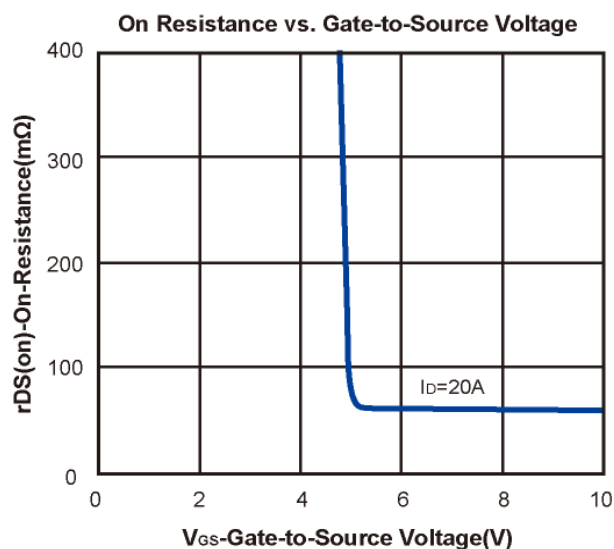
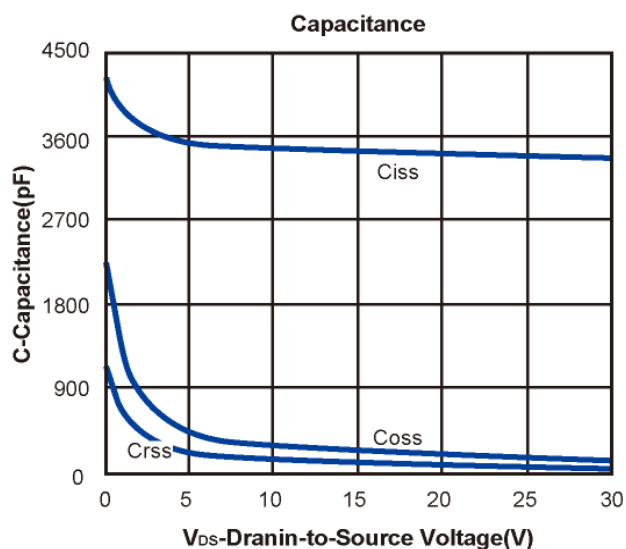
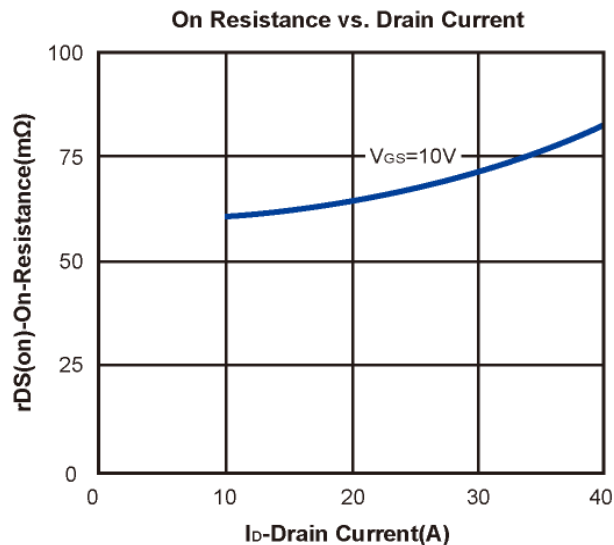
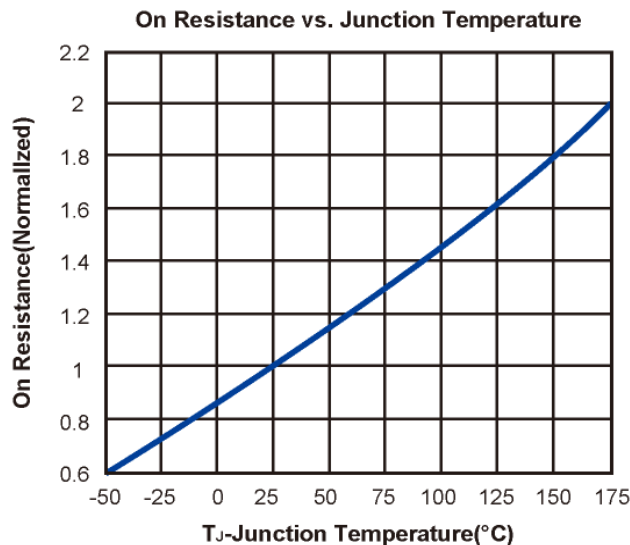
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	150			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=120V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance ^a	$V_{GS}=10V, I_D=20A$		60	75	m Ω
V_{SD}	Diode Forward Voltage	$I_S=20A, V_{GS}=0V$			1.4	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=75V, V_{GS}=10V, I_D=20A$		68.2		nC
Q_{gs}	Gate-Source Charge			14.8		
Q_{gd}	Gate-Drain Charge			19.2		
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		3360		pF
C_{oss}	Output Capacitance			153		
C_{rss}	Reverse Transfer Capacitance			75.7		
R_g	Gate-Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		2.7		Ω
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=75V, R_L=3.75\Omega, V_{GEN}=10V, R_G=2.5\Omega$		25.4		ns
t_r	Turn-On Rise Time			69.8		
$t_{d(off)}$	Turn-Off Delay Time			36.1		
t_f	Turn-Off Fall Time			19.9		

 Notes: a. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

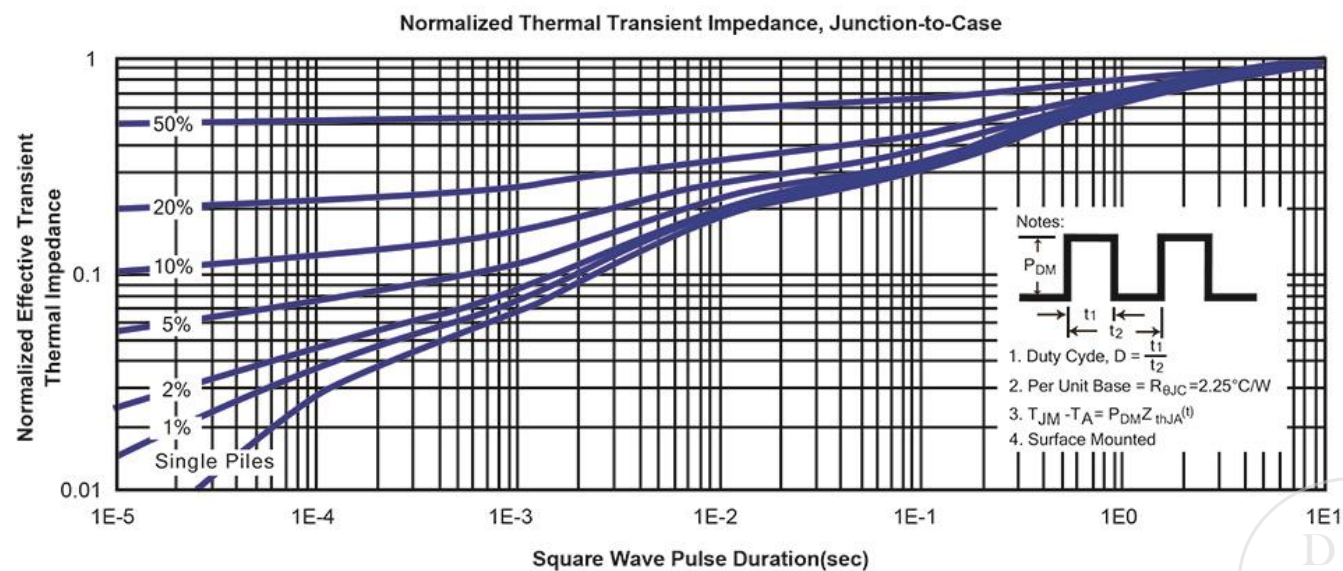
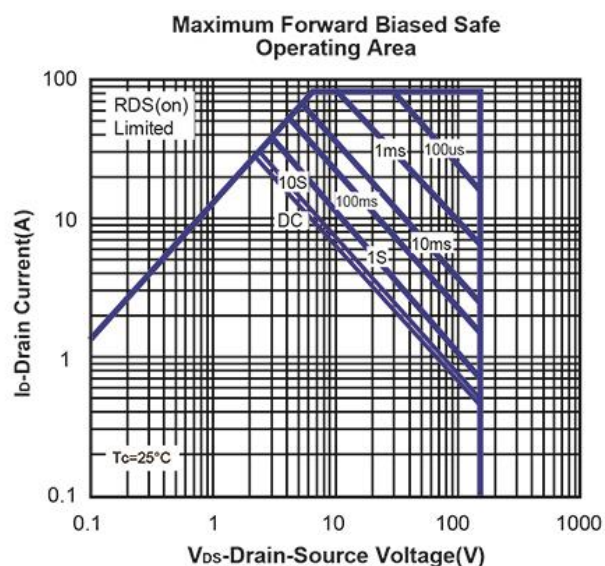
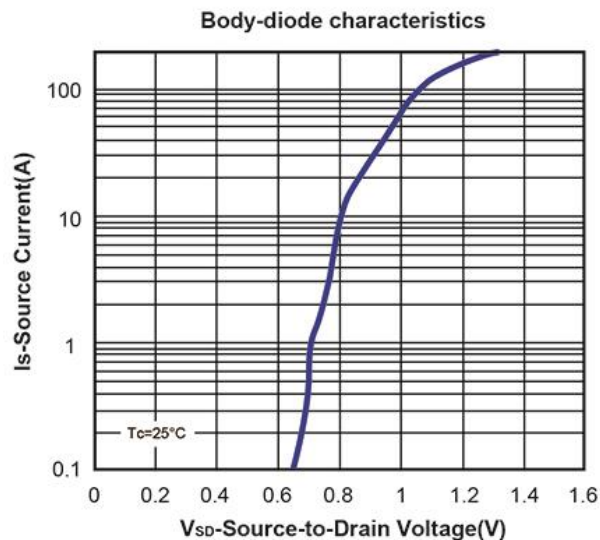
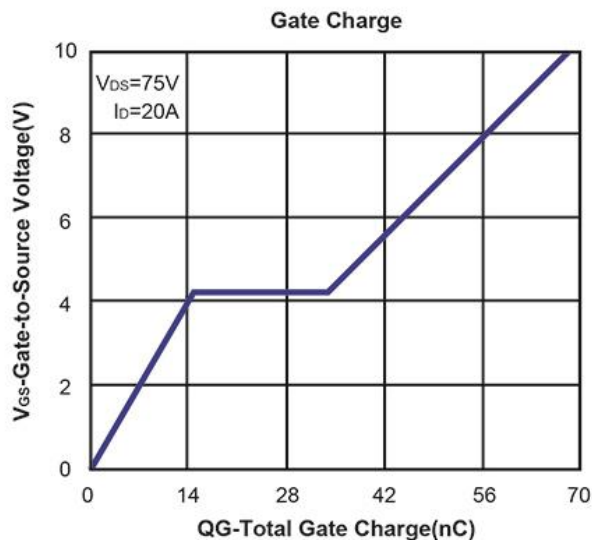
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Typical Characteristics (T_J = 25°C Noted)

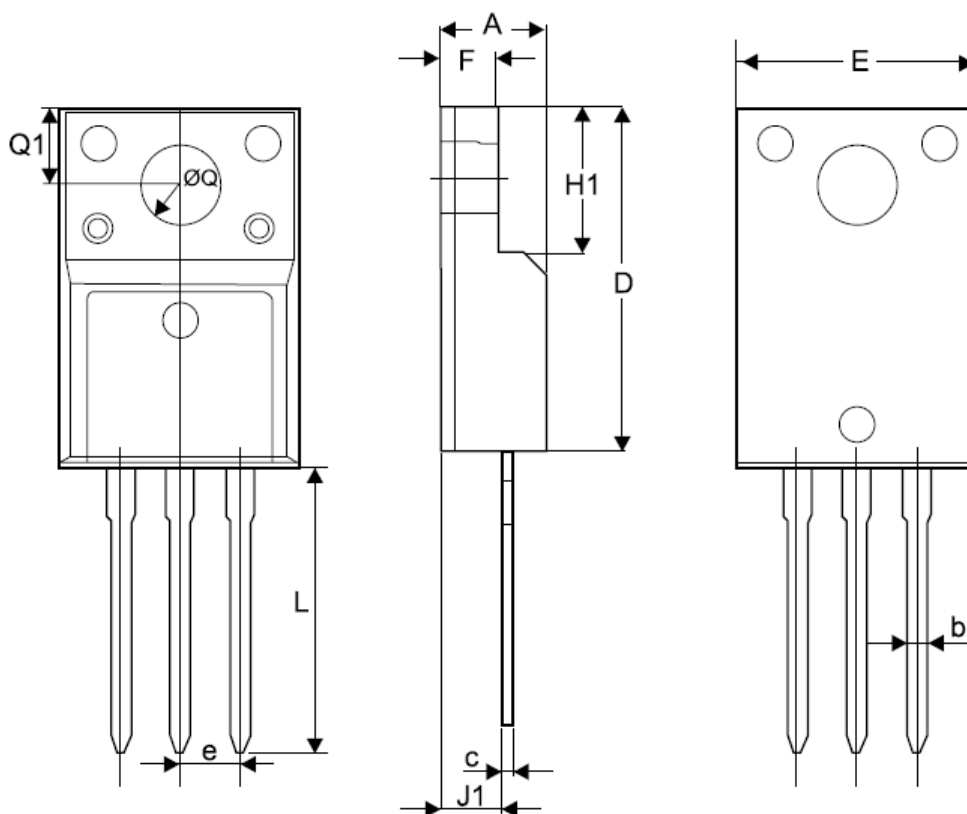


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TO-220F Package Outline



Symbol	MILLIMETERS(mm)	
	MIN	MAX
A	4.40	5.00
b	0.60	1.00
C	0.30	0.70
D	15.40	16.40
E	6.96	10.46
F	2.30	2.80
e	2.54 TYP	
H1	6.40	7.00
J1	2.45	3.05
L	12.28	13.68
Ø Q	2.92	3.38
Q1	3.05	3.55