Dual N - Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME2N7002D2KW-G is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 4\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 4.5\Omega @ V_{GS}=3V$
- ESD Protection HBM >2KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

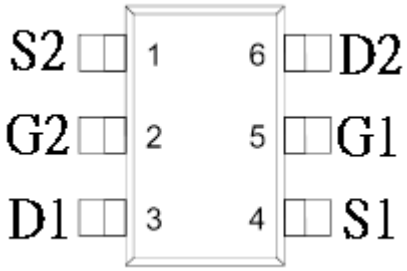
APPLICATIONS

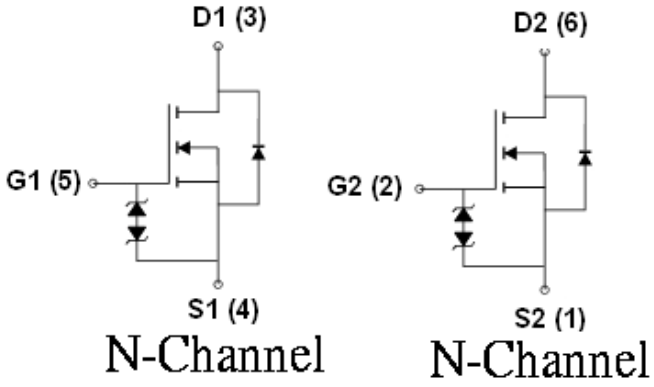
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-363)

Top View





Ordering Information: ME2N7002D2KW-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	0.3	A
	T_A=70℃	I_D	0.2	
Pulsed Drain Current		I_{DM}	1.1	A
Maximum Power Dissipation	T_A=25℃	P_D	0.3	W
	T_A=70℃	P_D	0.2	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	375	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		2.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=500mA		2	3	Ω
		V_{GS}=4.5V, I_D=200mA		2.3	4	
		V_{GS}=3V, I_D=10mA		3.7	4.5	
V_{SD}	Diode Forward Voltage *	I_S=200mA, V_{GS}=0V		0.82	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V,V_{GS}=10V,I_D=200mA		3.7		nC
Qg	Total Gate Charge	V_{DS}=30V,V_{GS}=4.5V,I_D=200mA		1.5		
Qgs	Gate-Source Charge			2.3		
Qgd	Gate-Drain Charge			0.5		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		18		pF
Coss	Output Capacitance			3		
Crss	Reverse Transfer Capacitance			1		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, R_L =150Ω V_{GS}=10V,R_{GS}=10Ω I_D=200mA		5.5		ns
t_r	Turn-On Rise Time			20		
$t_{d(off)}$	Turn-Off Delay Time			6		
t_f	Turn-Off Fall Time			20.6		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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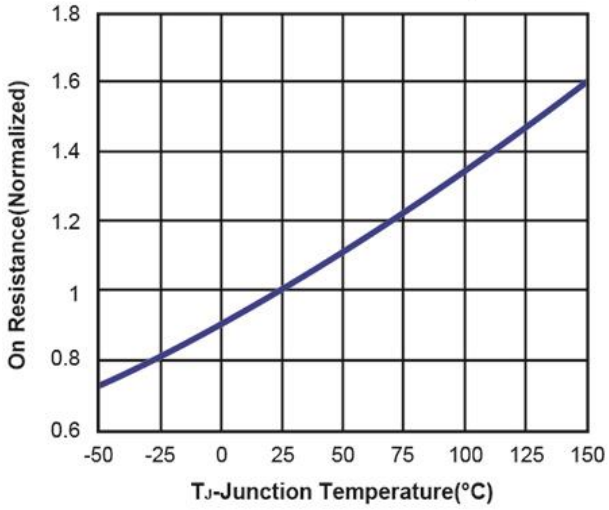
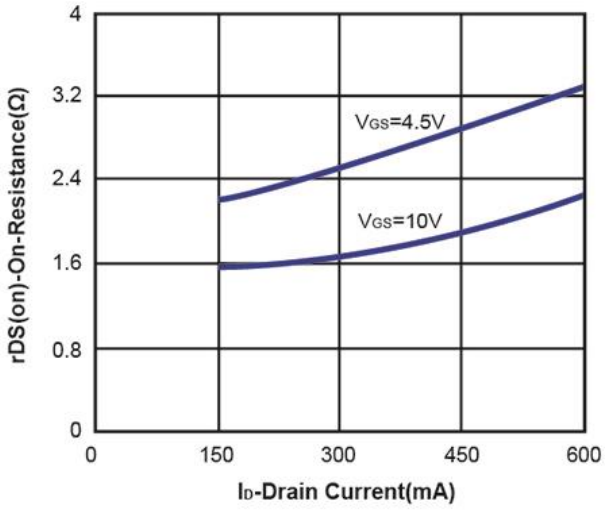
Typical Characteristics (T_J =25℃ Noted)

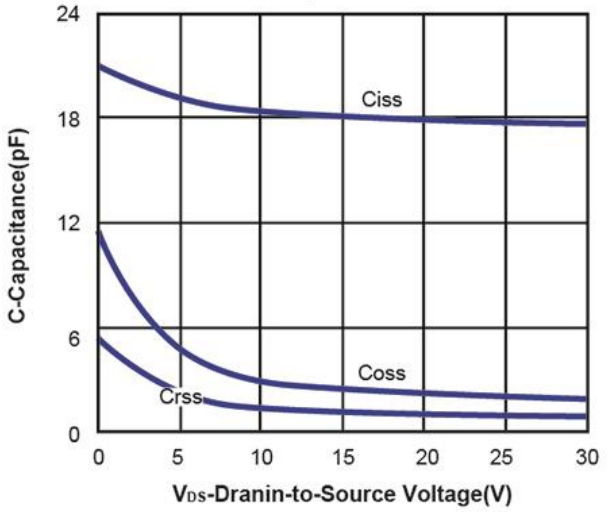
On Resistance vs. Junction Temperature



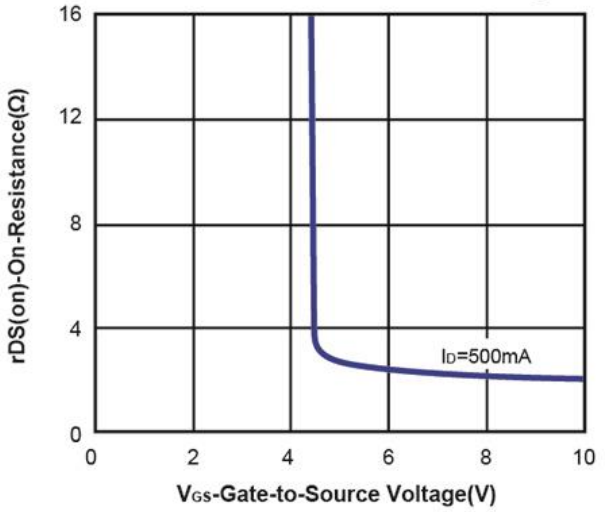
On Resistance vs. Drain Current



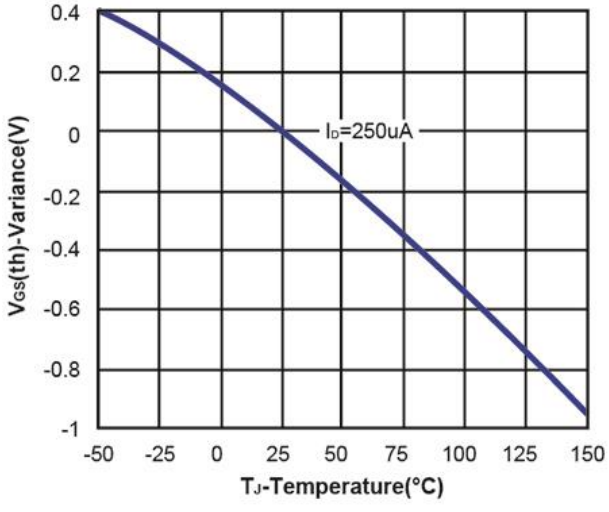
Capacitance



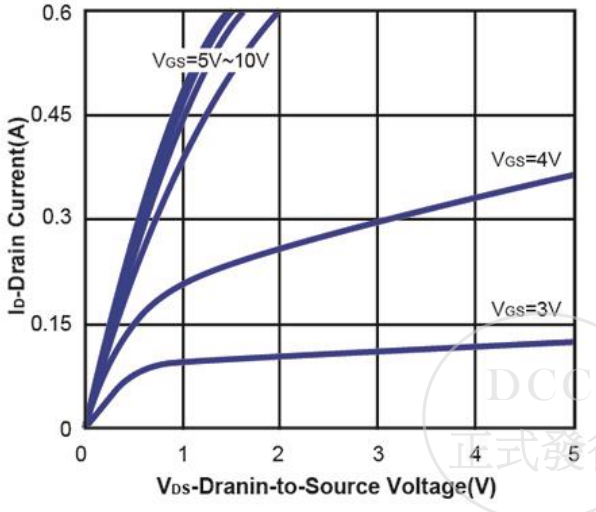
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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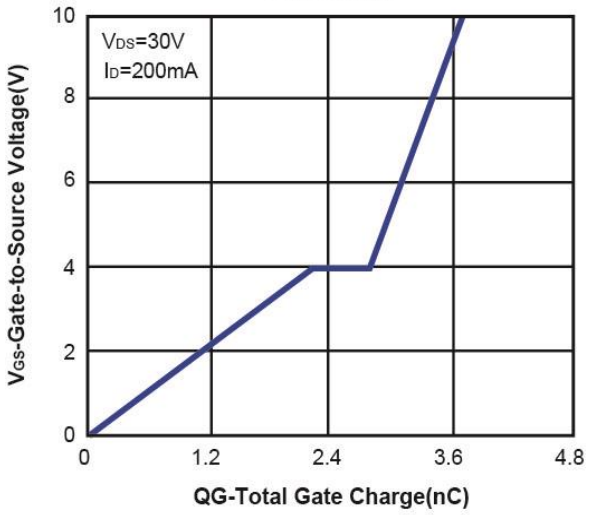
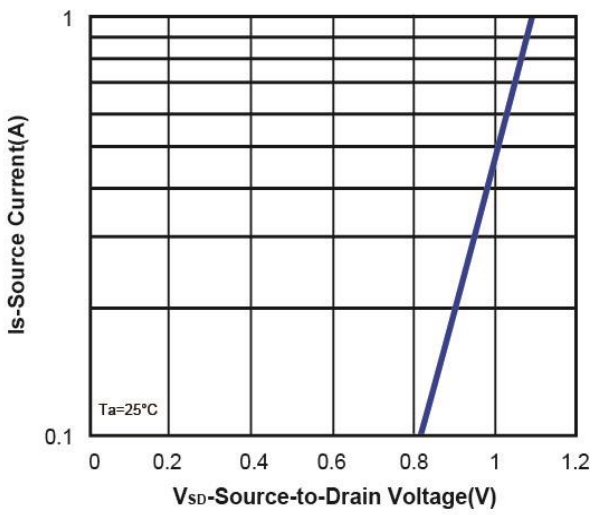
Typical Characteristics (T_J =25℃ Noted)

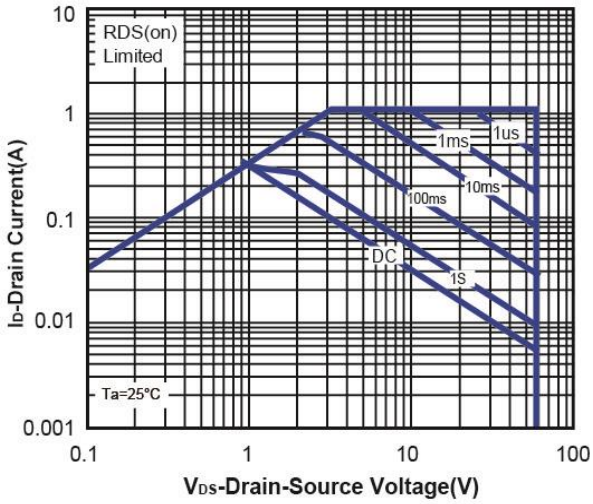
Gate Charge



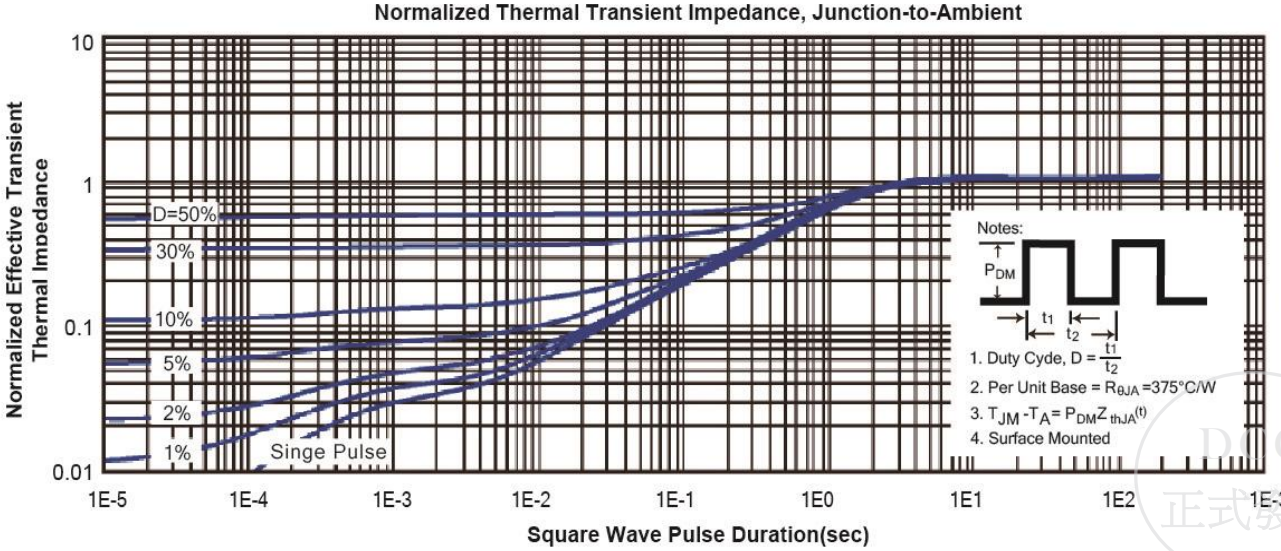
Body-diode characteristics



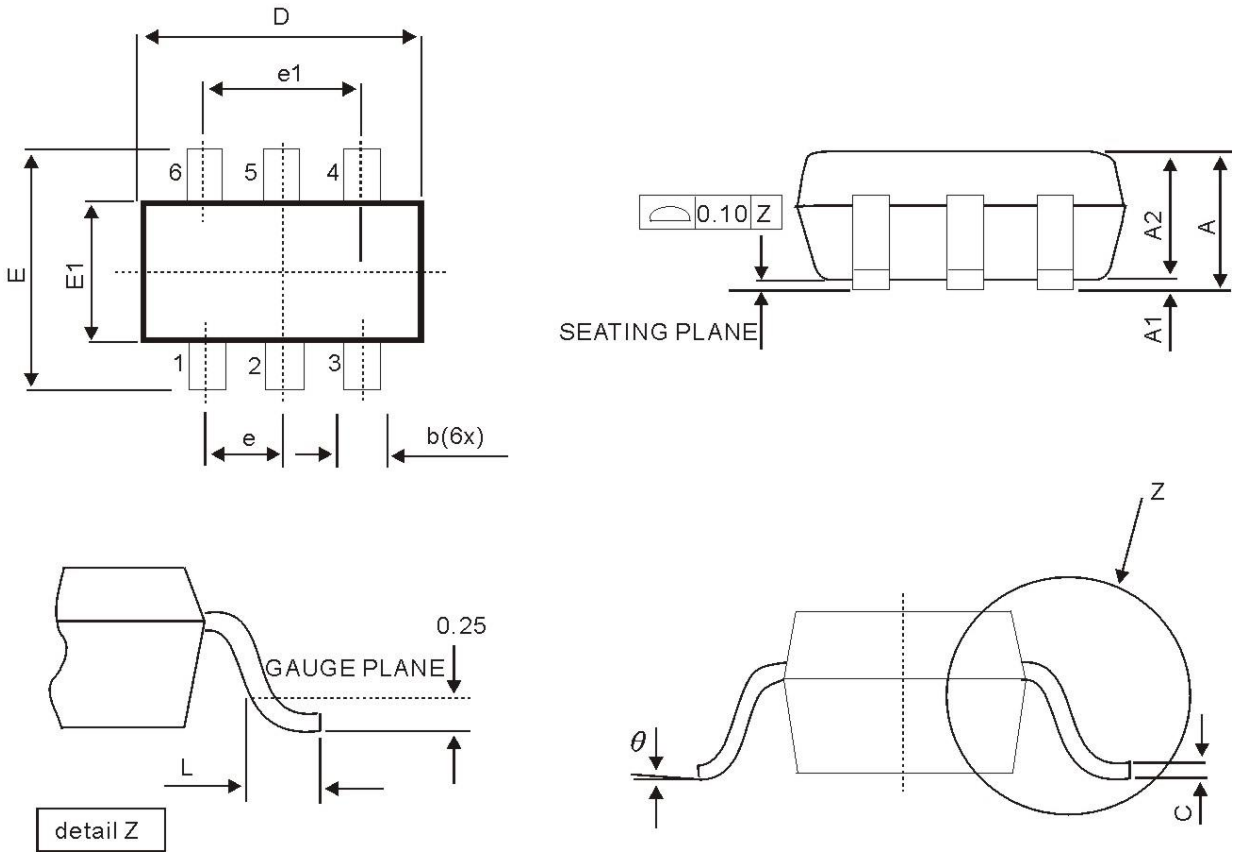
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-363 Package Outline



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.10		0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
b	0.15	0.30	0.006	0.012
c	0.08	0.22	0.003	0.009
D	1.80	2.15	0.073	0.085
E	1.80	2.40	0.071	0.094
E1	1.10	1.40	0.060	0.066
e	0.65 BSC		0.026 BSC	
e1	1.30 BS C		0.051 BSC	
L	0.26	0.46	0.043	0.055
θ	0°	8°	0°	8°