## N-Channel MOSFET – ESD Protected

### GENERAL DESCRIPTION

The ME2N7002DW is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

### FEATURES

- ESD Rating 2KV HBM
- 3-pin SOT-323 package
- Pb-free plating ; RoHS compliant (green Product)

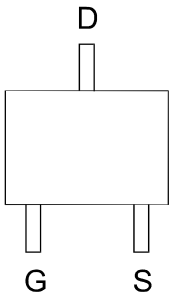
### Mechanical data

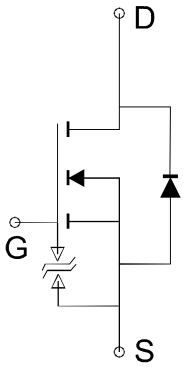
- High density cell design for low $R_{DS(ON)}$
- Very low leakage current in off condition
- Advanced trench process technology
- High-speed switching.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.

### PIN CONFIGURATION

(SOT-323)

Top View




**Maximum Ratings** @ TA=25℃ unless otherwise specified

| Characteristic | | Symbol | ME2N7002DW | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | VDSS | 60 | V |
| Gate-Source Voltage | Continuous | VGSS | ±20 | V |
| Drain Current | Continuous | ID | 115 | mA |
| | Pulsed | IDP *1 | 800 | mA |
| Reverse drain current | Continuous | IDR | 115 | mA |
| | Pulsed | IDRP *1 | 800 | mA |
| Total Power Dissipation | | Pd *2 | 225 | mW |
| Channel temperature | | Tch | 150 | ℃ |
| Storage Temperature Range | | Tstg | -55 to +150 | ℃ |

*1 Pw ≦10 μs, Duty cycle ≦1 %

*2 When mounted on a 1*0.75*0.062 inch glass epoxy board

**Electrical Characteristics** @ $T_A$=25℃ unless otherwise specified, per element

| Characteristic | Symbol | Min | Typ | MAX | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS(Note 2)** | | | | | | |
| Drain-Source Breakdown Voltage | V(BR)DSS | 60 | | | V | VGS=0V, ID=10μA |
| Zero Gate Voltage Drain Current | IDSS | | | 1.0 | μA | VDS=60V, VGS=0V |
| Gate-source Leakage | IGSS | | | ±10 | μA | VGS=±20V, VDS=0V |
| **ON CHARACTERISTICS(Note 2)** | | | | | | |
| Gate Threshold Voltage | VGS(th) | 1.0 | 1.85 | 2.5 | V | VDS=VGS, ID=250uA |
| Static Drain-Source On-Resistance | RDS(ON) | | | 7.5 | Ω | VGS=10V, ID =0.5A |
| | | | | 7.5 | | VGS=5V, ID=0.05A |
| Forward transfer admittance | $g_{fs}$ * | 80 | | | mS | VDS=10V, ID=0.2A |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | CiSS | | 25 | 50 | pF | VDS=25V |
| Output Capacitance | COSS | | 10 | 25 | pF | VGS=0V |
| Reverse Transfer Capacitance | CrSS | | 3.0 | 5.0 | pF | f=1.0MHz |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn-On Delay Time | TD(ON) * | | 12 | 20 | nS | ID=0.2A,VDD=30V, |
| Turn-Off Delay Time | TD(OFF)* | | 20 | 30 | nS | VGS=10v,RL=150Ω,RG=10Ω |

* Pw ≦ 300 μs, Duty cycle ≦ 1%

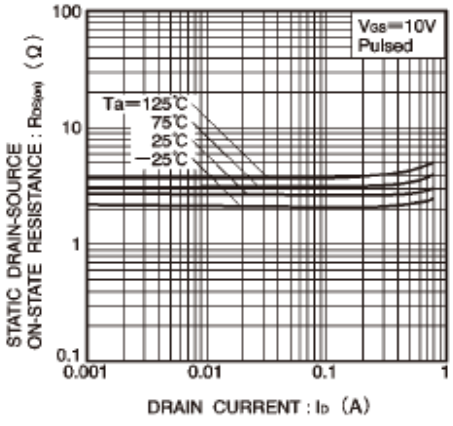



Fig.1 Static drain-source on-state resistance vs. drain current (Ⅰ)

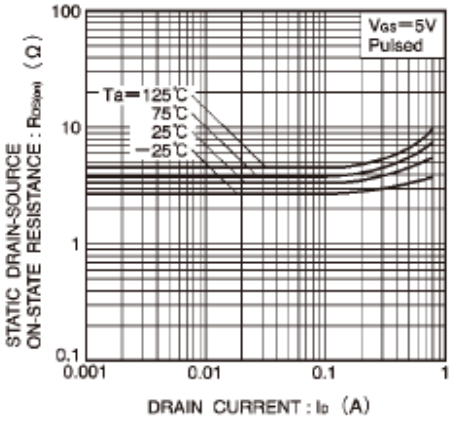



Fig.2 Static drain-source on-state resistance vs. drain current (Ⅱ)

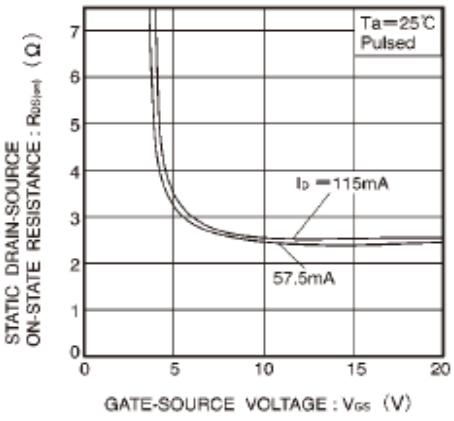



Fig.3 Static drain-source on-state resistance vs. gate-source voltage

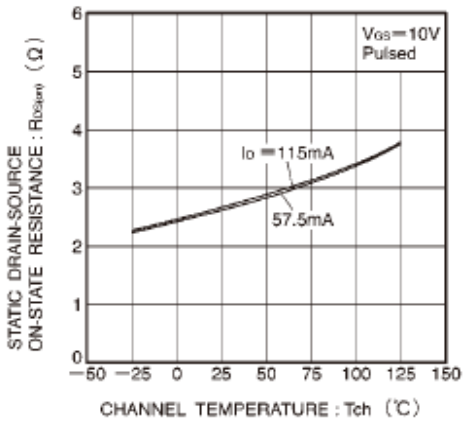



Fig.4 Static drain-source on-state resistance vs. channel temperature

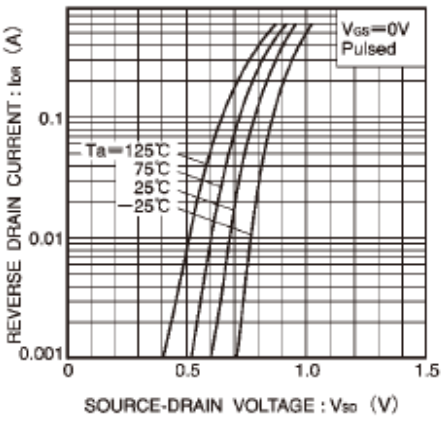



Fig.5 Reverse drain current vs. source-drain voltage (Ⅰ)

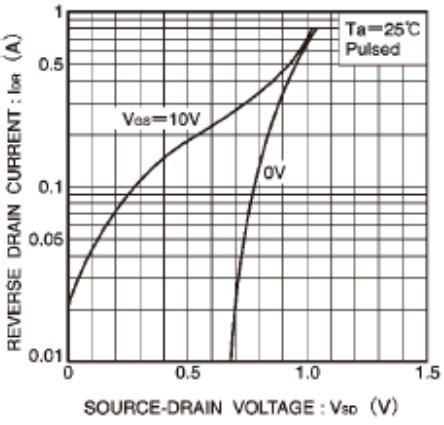



Fig.6 Reverse drain current vs. source-drain voltage (Ⅱ)

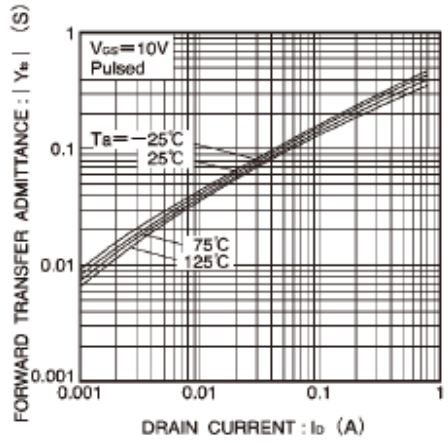



Fig.7 Forward transfer admittance vs. drain current

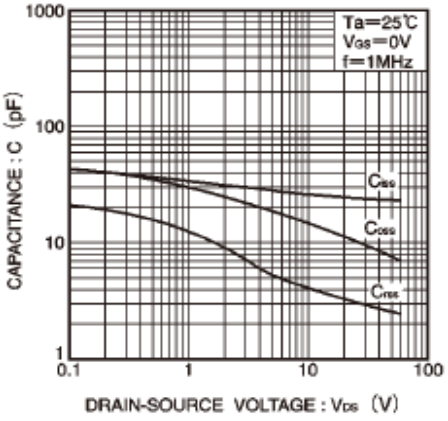



Fig.8 Typical capacitance vs. drain-source voltage

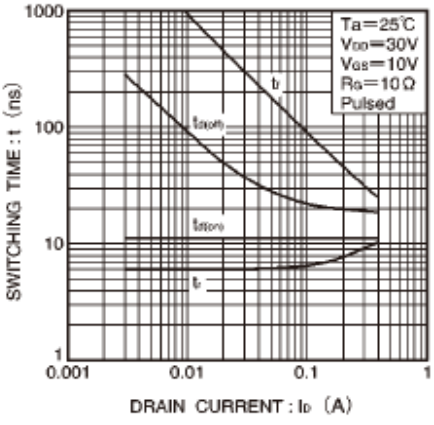
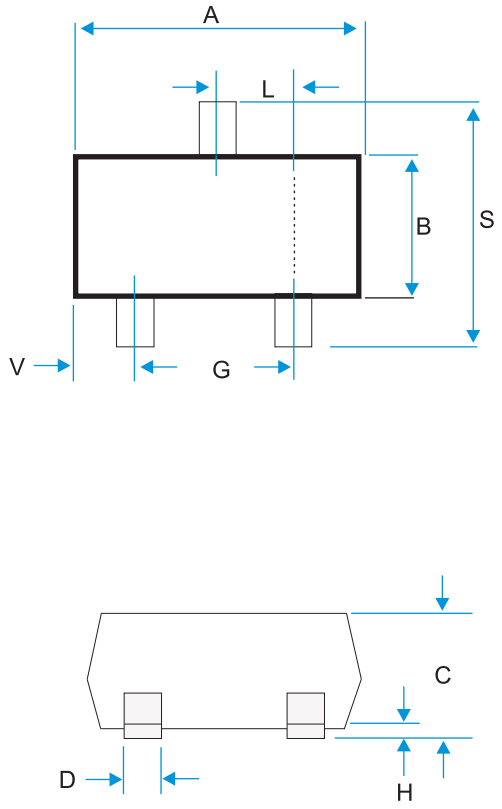



Fig.9 Switching characteristics
(See Figures 13 and 14 for the measurement circuit and resultant waveforms)

# SOT-323 Package Outline



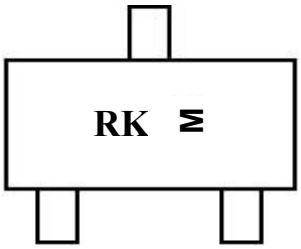

| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| A | 1.80 | 2.20 |
| B | 1.15 | 1.35 |
| C | 0.80 | 1.10 |
| D | 0.20 | 0.40 |
| G | 1.20 | 1.40 |
| H | 0.00 | 0.10 |
| J | 0.05 | 0.25 |
| K | 0.425 REF | |
| L | 0.650 BSC | |
| S | 2.00 | 2.45 |
| V | 0.30 | 0.40 |

**N-Channel MOSFET – ESD Protected**

**Device name:ME2N7002DW**

**Package:SOT-323**

**Marking Code:**




**RK: Device Marking Code**

**M: Date code**

MONTH CODE

ODD YEARS(2007,2009)

| | |
|---|---|
| **Jan** | 1 |
| **Feb** | 2 |
| **Mar** | 3 |
| **Apr** | 4 |
| **May** | 5 |
| **Jun** | 6 |
| **Jul** | 7 |
| **Aug** | 8 |
| **Sep** | 9 |
| **Oct** | T |
| **Nov** | V |
| **Dec** | C |

EVEN YEARS(2006,2008)

| | |
|---|---|
| **Jan** | E |
| **Feb** | F |
| **Mar** | H |
| **Apr** | J |
| **May** | K |
| **Jun** | L |
| **Jul** | N |
| **Aug** | P |
| **Sep** | U |
| **Oct** | X |
| **Nov** | Y |
| **Dec** | Z |