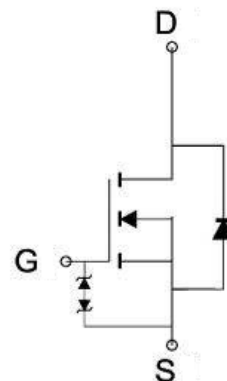
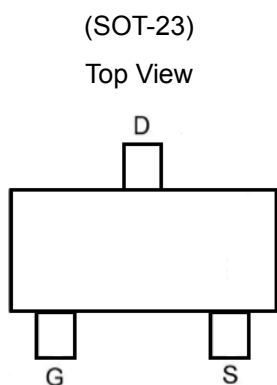


N-Channel 60V (D-S) MOSFET, ESD Protection
GENERAL DESCRIPTION

The ME2N7002F is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

PIN CONFIGURATION

N-Channel MOSFET
Ordering Information:ME2N7002F (Pb-free)

ME2N7002F-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	TA=25°C	0.17
		TA=70°C	0.13
Pulsed Drain Current	I _{DM}	0.7	A
Maximum Power Dissipation	P _D	TA=25°C	0.36
		TA=70°C	0.23
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	R _{θJA}	350	°C/W

 *The device mounted on 1in² FR4 board with 2 oz copper

FEATURES

- R_{DS(ON)} ≤ 8Ω@V_{GS}=4V
- R_{DS(ON)} ≤ 13Ω@V_{GS}=2.5V
- Super high density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



N-Channel 60V (D-S) MOSFET, ESD Protection
Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.8		1.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =4V, I _D =10mA		5	8	Ω
		V _{GS} =2.5V, I _D =1mA		7	13	
V _{SD}	Diode Forward Voltage	I _S =200mA, V _{GS} =0V			1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =25V, V _{GS} =10V, I _D =0.22A		4.9		nC
Q _{gs}	Gate-Source Charge			2.1		
Q _{gd}	Gate-Drain Charge			0.6		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHZ		21		pf
C _{oss}	Output Capacitance			10		
C _{rss}	Reverse Transfer Capacitance			2		
t _{d(on)}	Turn-On Delay Time	V _{DD} =5V, R _L =500Ω, V _{GEN} =5V, R _G =10Ω		10.1		ns
t _r	Turn-On Rise Time			7.3		
t _{d(off)}	Turn-Off Delay Time			31.3		
t _f	Turn-Off Fall Time			28.2		

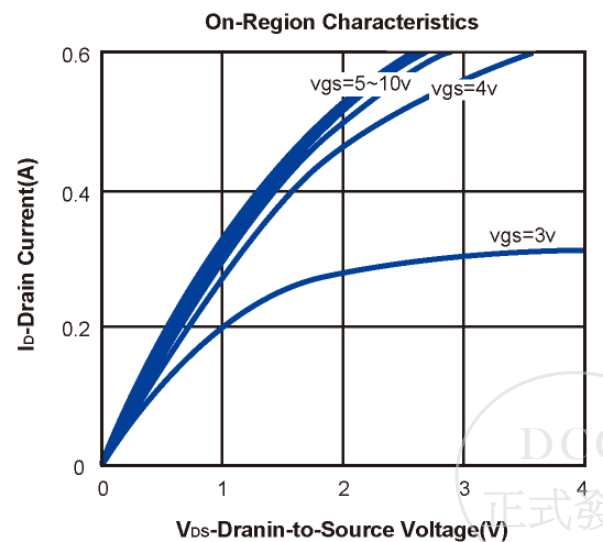
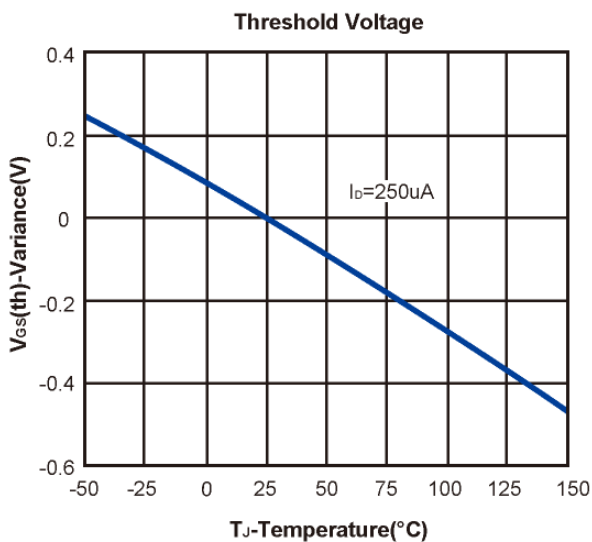
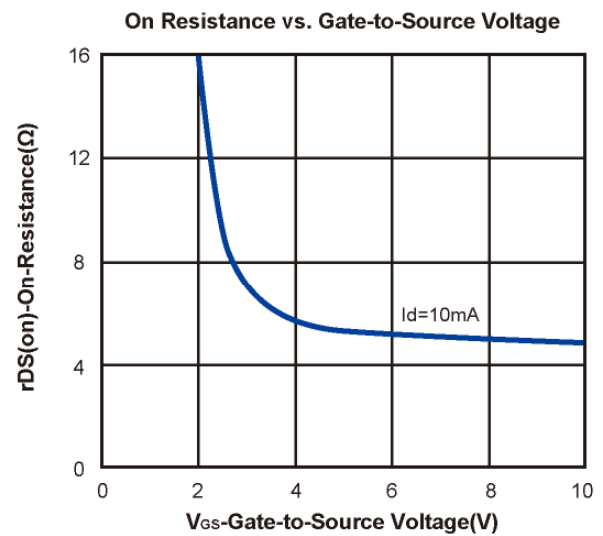
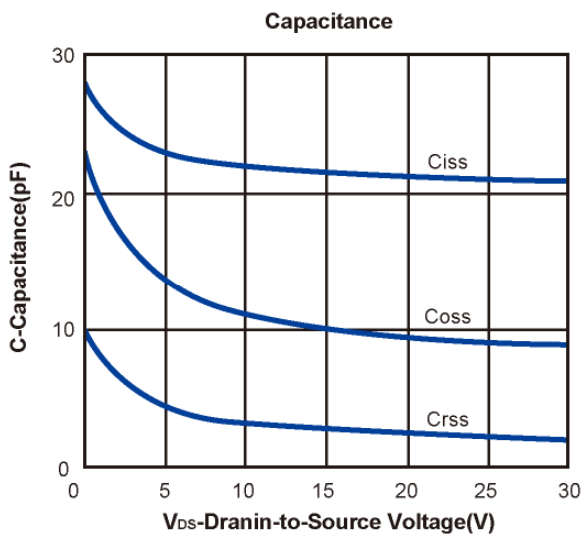
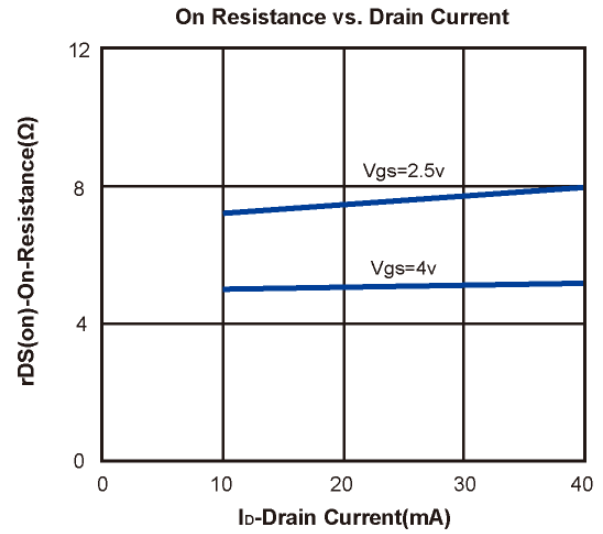
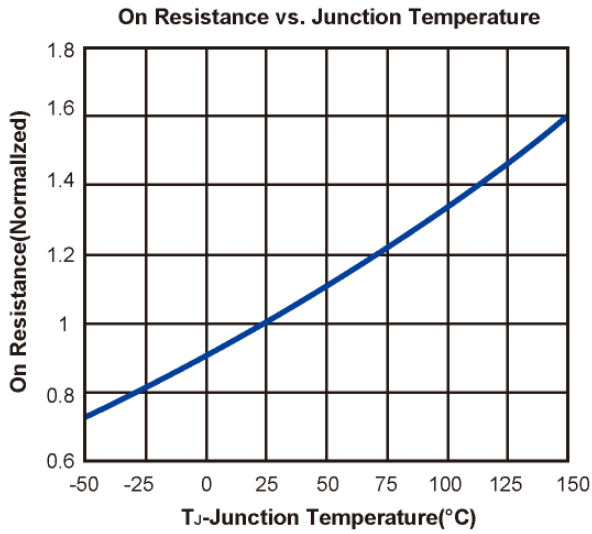
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



N-Channel 60V (D-S) MOSFET, ESD Protection

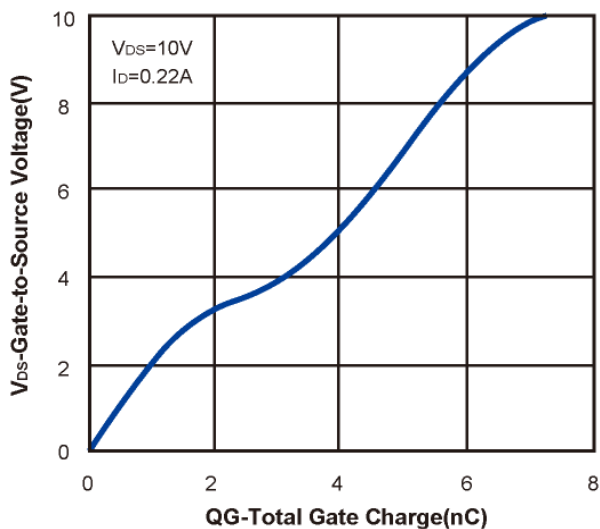
Typical Characteristics (T_J = 25°C Noted)



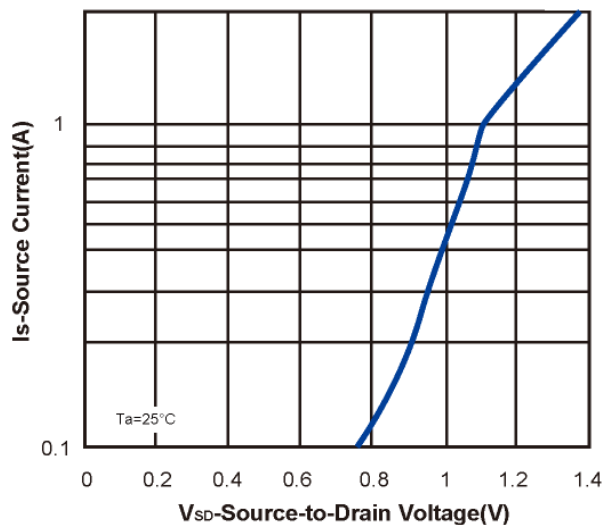
N-Channel 60V (D-S) MOSFET, ESD Protection

Typical Characteristics (T_J =25°C Noted)

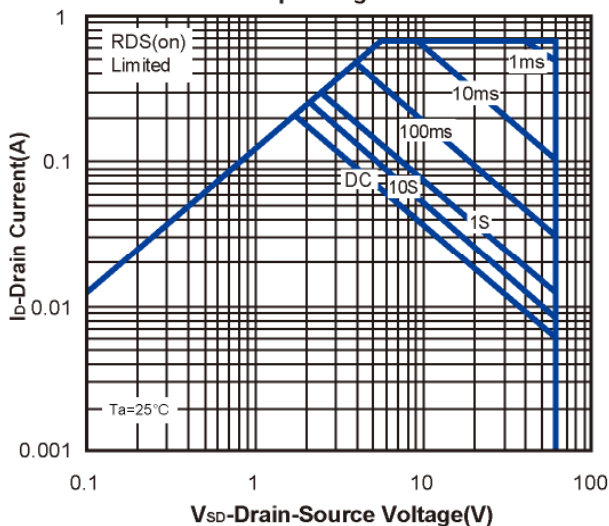
Gate Charge



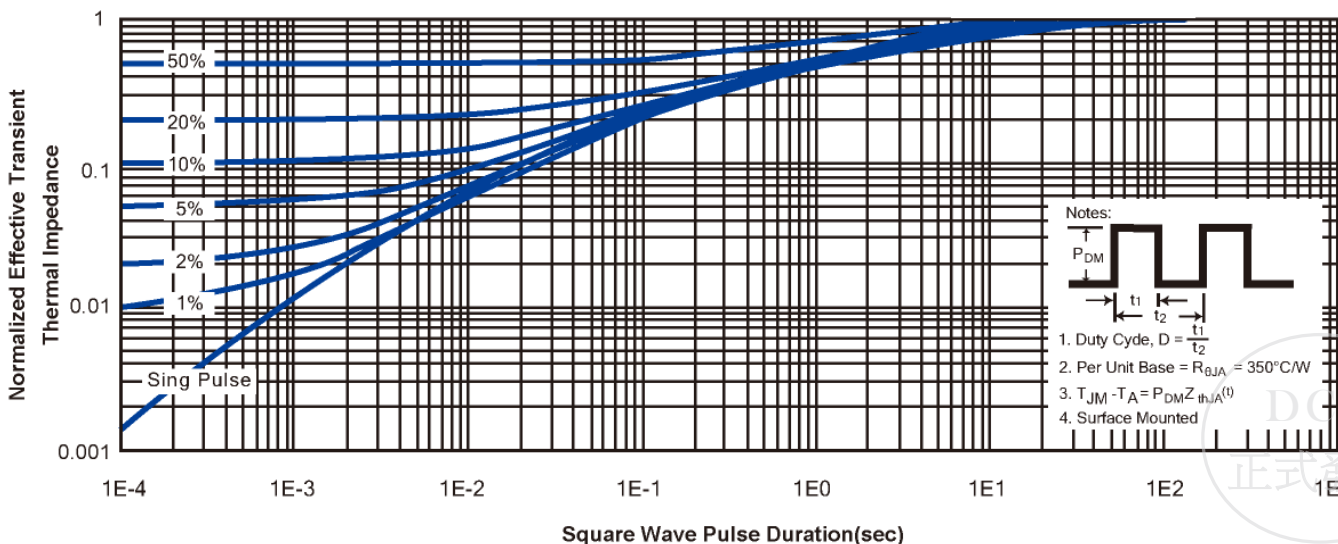
Body-diode characteristics



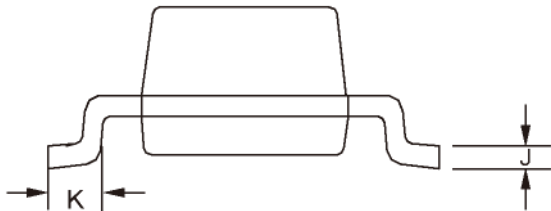
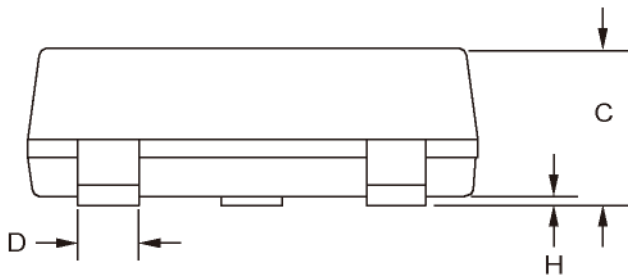
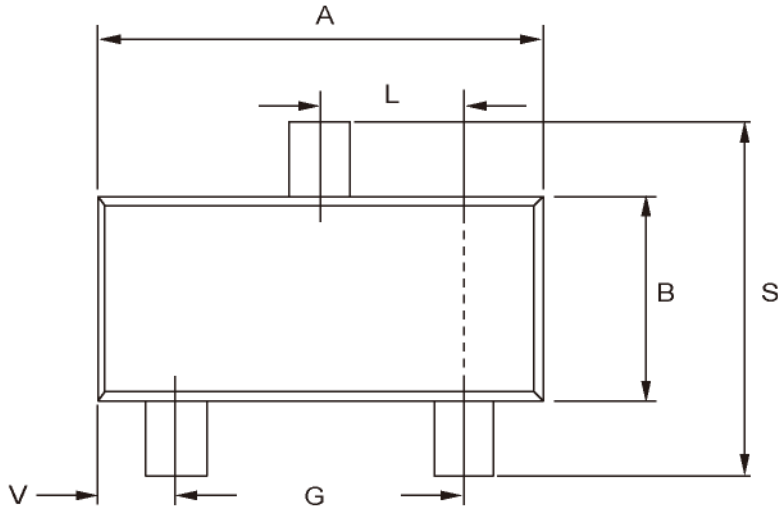
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

