Dual N - Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME2N7002KW is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 4\Omega @ V_{GS}=4.5V$
- ESD Protection HBM >1KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

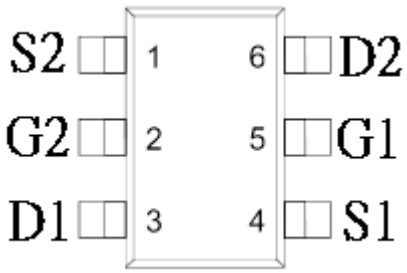
APPLICATIONS

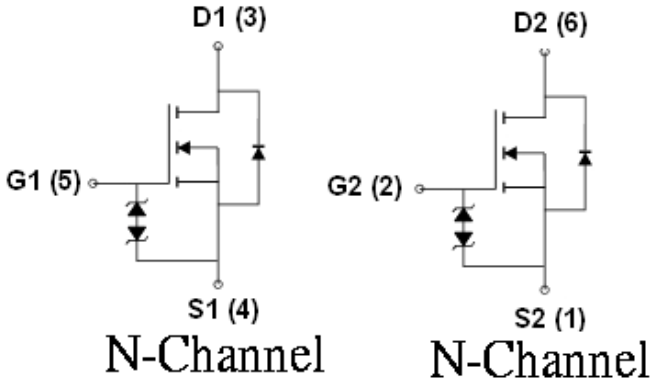
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-363)

Top View





Ordering Information: ME2N7002KW (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	0.3	A
	T_A=70℃	I_D	0.2	
Pulsed Drain Current		I_{DM}	1.1	A
Maximum Power Dissipation	T_A=25℃	P_D	0.3	W
	T_A=70℃	P_D	0.2	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	375	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		2.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±1	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=500mA		2.2	3	Ω
		V_{GS}=4.5V, I_D=200mA		2.4	4	
V_{SD}	Diode Forward Voltage *	I_S=200mA, V_{GS}=0V		0.82	1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V,V_{GS}=10V,I_D=200mA		3.7		nC
Qg	Total Gate Charge	V_{DS}=30V,V_{GS}=4.5V,I_D=200mA		1.4		
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			0.2		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		21		pF
Coss	Output Capacitance			3		
Crss	Reverse Transfer Capacitance			1		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, R_L =150Ω V_{GS}=10V,R_{GS}=10Ω I_D=200mA		3.5		ns
t_r	Turn-On Rise Time			20.3		
$t_{d(off)}$	Turn-Off Delay Time			4.4		
t_f	Turn-Off Fall Time			22.2		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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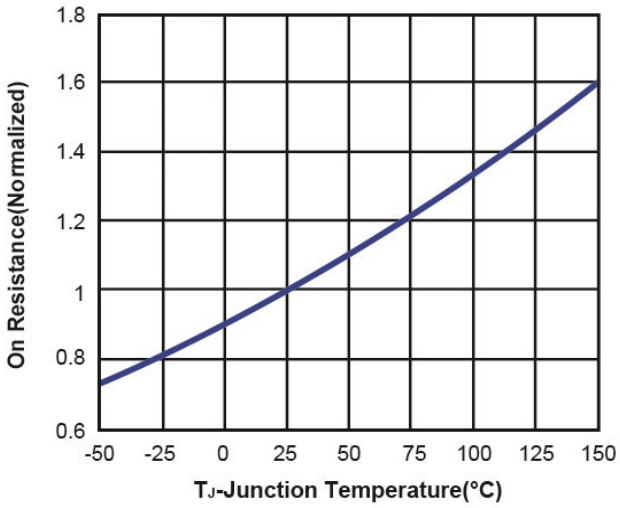
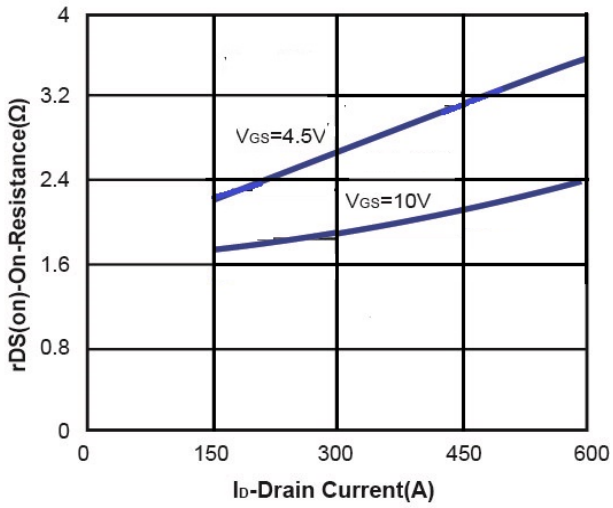
Typical Characteristics (T_J =25℃ Noted)

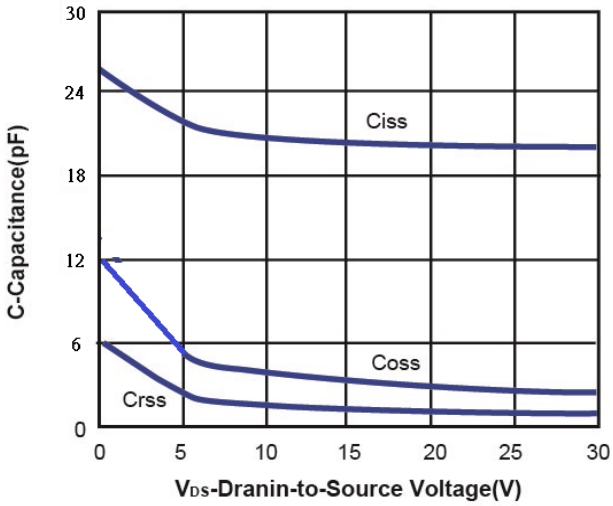
On Resistance vs. Junction Temperature



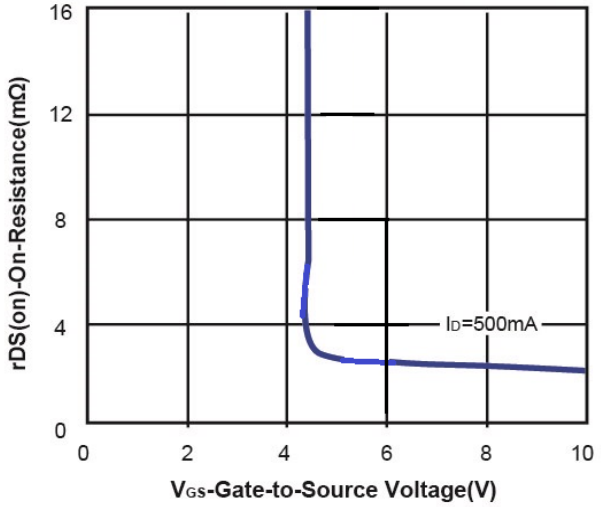
On Resistance vs. Drain Current



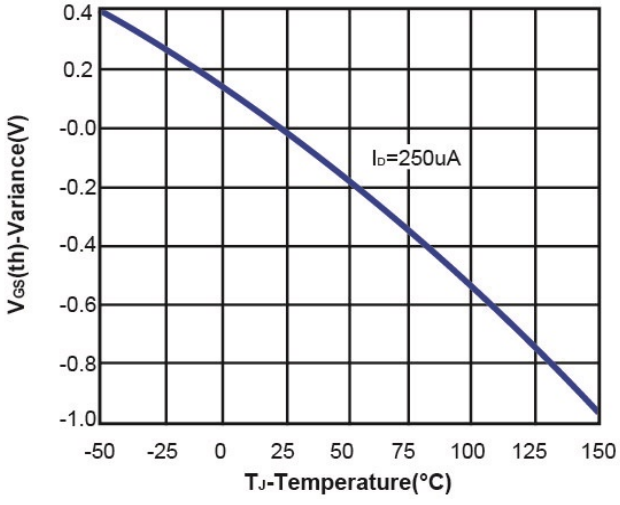
Capacitance



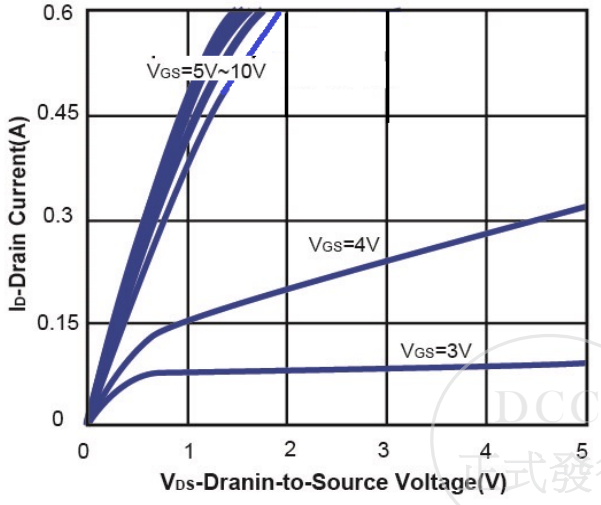
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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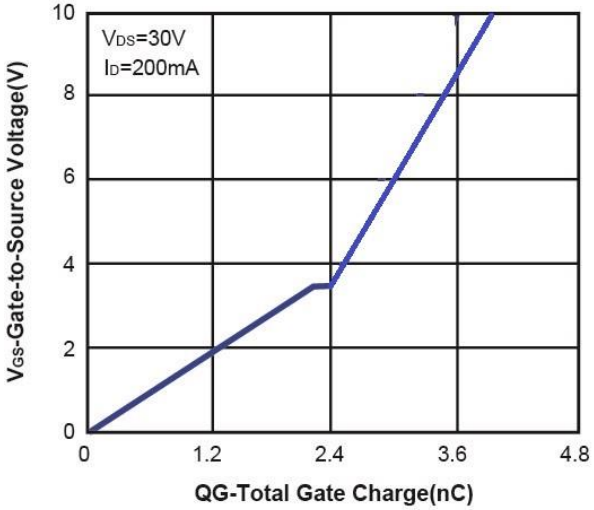
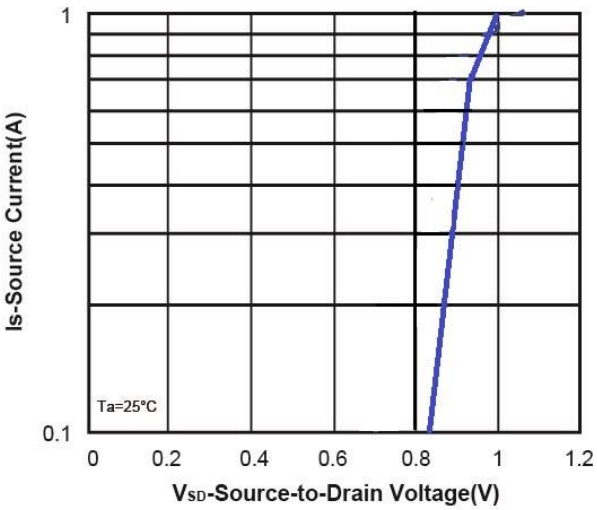
Typical Characteristics (T_J =25℃ Noted)

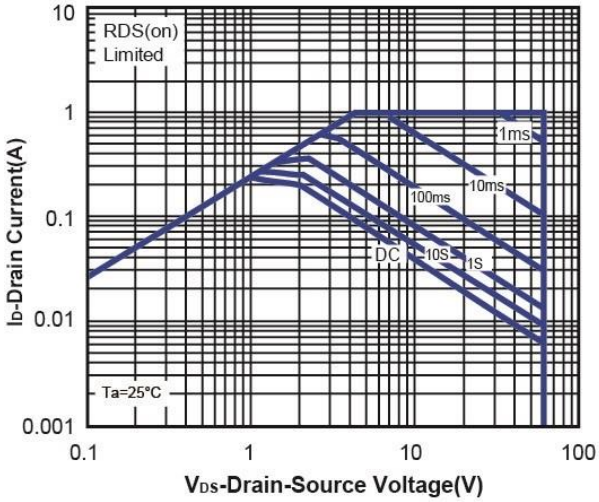
Gate Charge



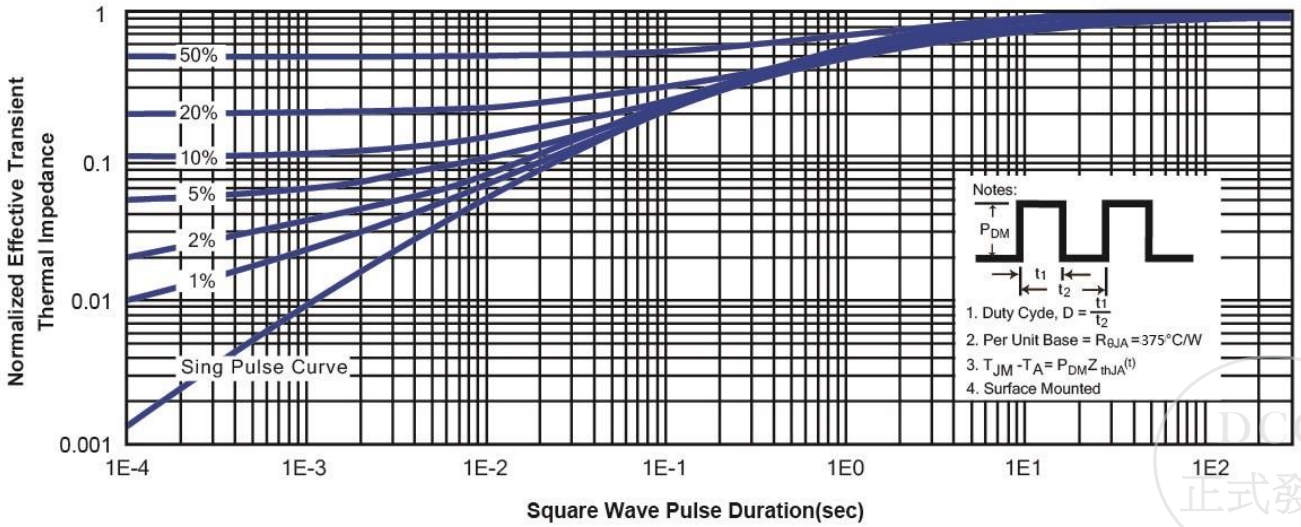
Body-diode characteristics



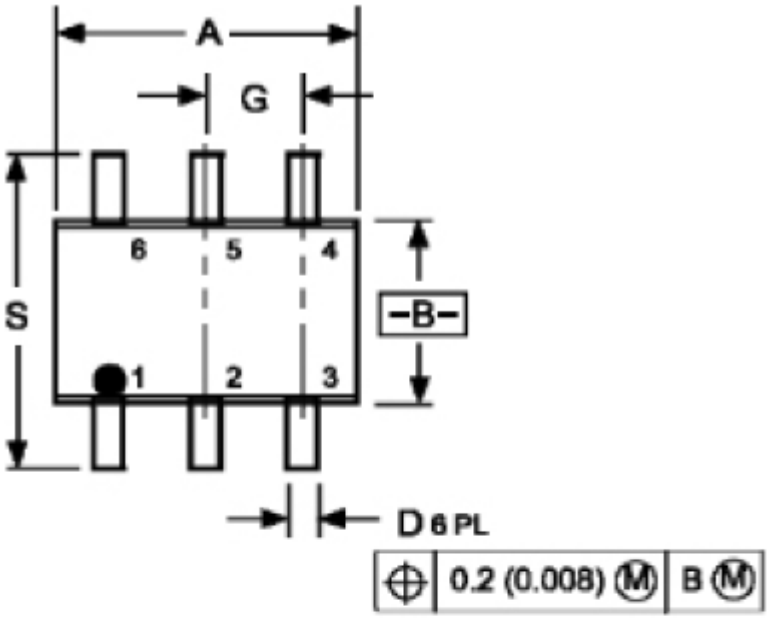
Maximum Forward Biased Safe Operating Area

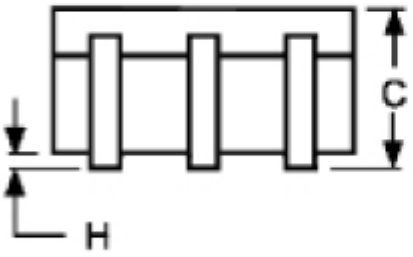


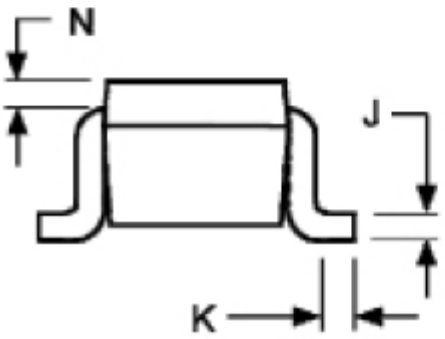
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-363 Package Outline







DIM	INCHES		MILLMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.012	0.018	0.30	0.45
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

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Device name: ME2N7002KW

Package: SOT-363

Marking Code:

E76: Device Marking Code
M: Date code

MONTH CODE

ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

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