N-Channel MOSFET

GENERAL DESCRIPTION

The ME2N7002W is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- Simple Drive Requirement
- Small Package Outline
- ROHS Compliant

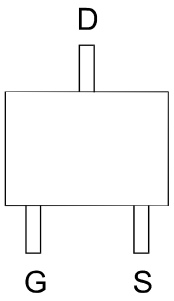
Mechanical data

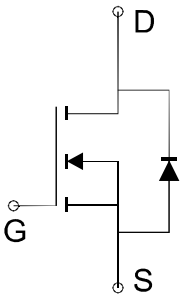
- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switching.
- Rugged and reliable.
- High saturation current capability.
- High-speed switching.
- Not thermal runaway.
- The soldering temperature and time shall not exceed 260℃ for more than 10 seconds.

PIN CONFIGURATION

(SOT-323)

Top View





PARAMETER	Symbol	Value		Units
Drain-Source Voltage	V_{DSS}	60		V
Drain-gate Voltage	V_{DRG}	60		V
Gate-Source Voltage	V_{GSS}	±20		V
Drain Current*	I_D	200		mA
Total Power Dissipation*	P_D	200		mW
Operating and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150		°C
Thermal Resistance, Junction-to-Ambient*	$R_{\theta JA}$	Typ	210	°C/W
		Max	350	

*The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, ID=10μA	60	-	-	V
$V_{th(GS)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	2.1	2.5	V
I_{GSS}	Gate-body Leakage	V_{DS}=0V, V_{GS}= ±20V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	-	-	1	uA
		V_{DS}=60V, V_{GS}=0V,T_j=125	-	-	500	
$I_{D(ON)}$	On-state Drain Current	V_{GS}=10V, V_{DS}≧2$V_{DS(ON)}$	500	-	-	mA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=500mA	-	2.5	4	Ω
		V_{GS}=4.5V, I_D=50mA	-	3	5	
g_{ts}	Forward Trans-conductance	V_{DS}≧2 $V_{DS(ON)}$, I_D=200mA	80	-	-	ms
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS}=10V, I_D=500mA	-	-	3.75	V
		V_{GS}=5V, I_D=50mA	-	-	1.5	V
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	25	50	pF
C_{OSS}	Output Capacitance		-	6	25	
C_{rss}	Reverse Transfer Capacitance		-	1.2	5	

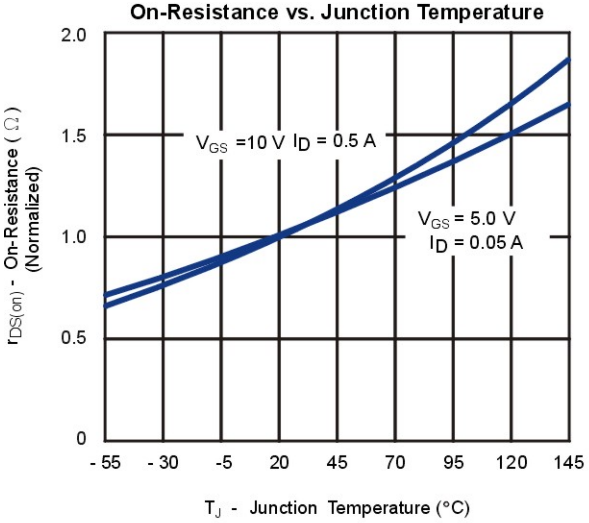
SWITCHING TIME

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	V_{DD}=30V, R_L=25Ω, I_{DD}=500mA V_{GS}=10V, R_{GEN}=25Ω	-	7.5	20	ns
$t_{d(off)}$	Turn-off Time		-	7.5	20	

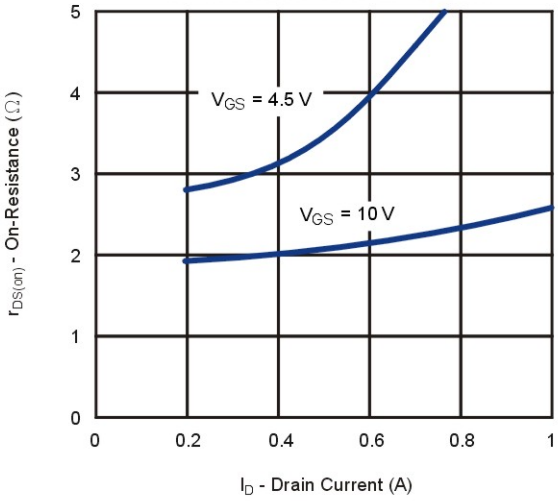
N-Channel MOSFET

Typical Characteristics (T_J =25℃ Noted)

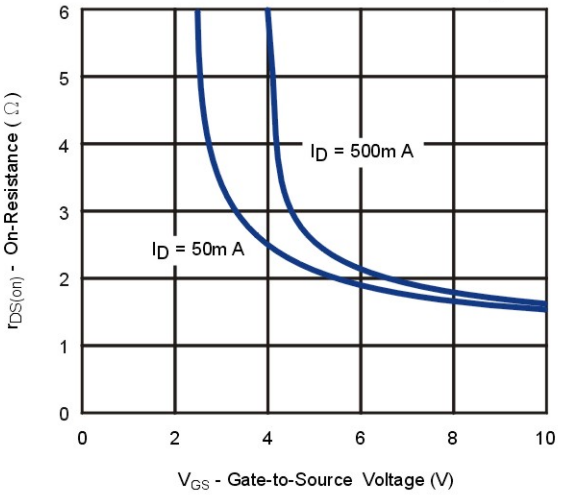
On-Resistance vs. Junction Temperature



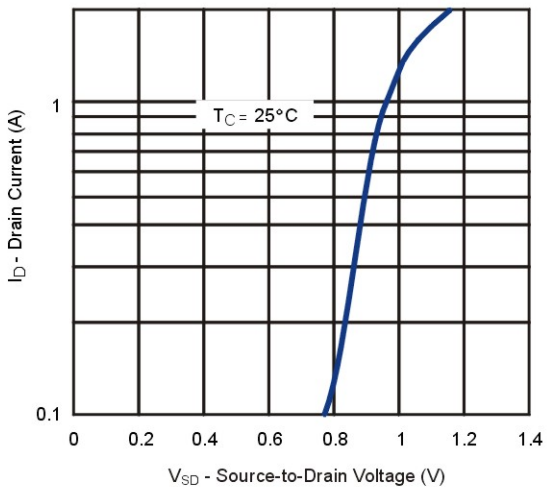
On-Resistance vs. Drain Current



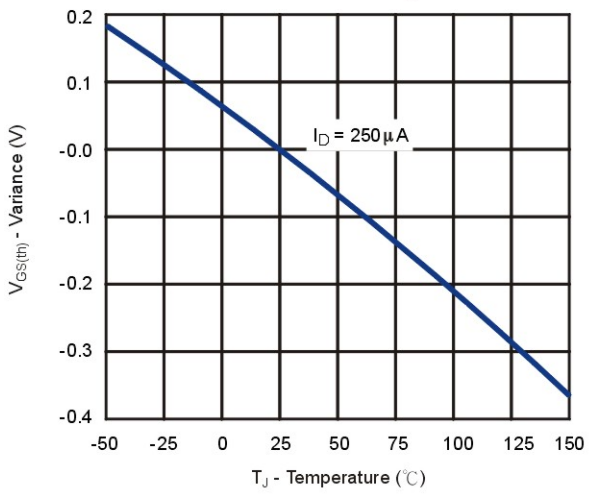
On-Resistance vs. Gate-Source Voltage



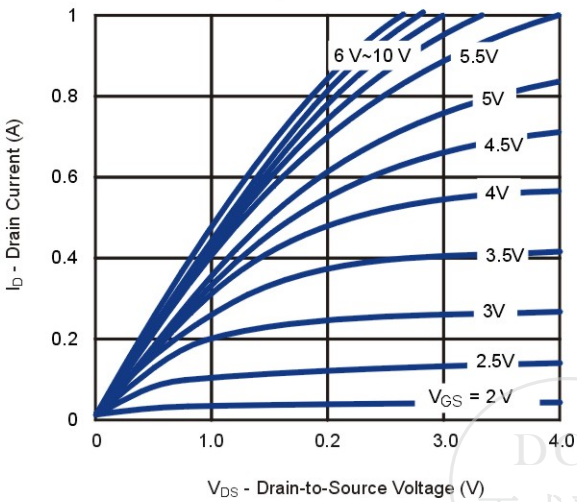
Body - Diode Characteristics



Threshold Voltage



On-Region Characteristics

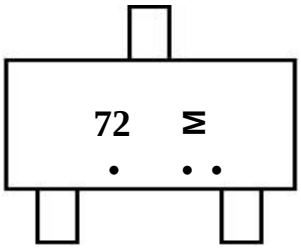


N-Channel MOSFET

Device name:ME2N7002W

Package:SOT-323

Marking Code:



72: Device Marking Code

M: Date Code

MONTH CODE

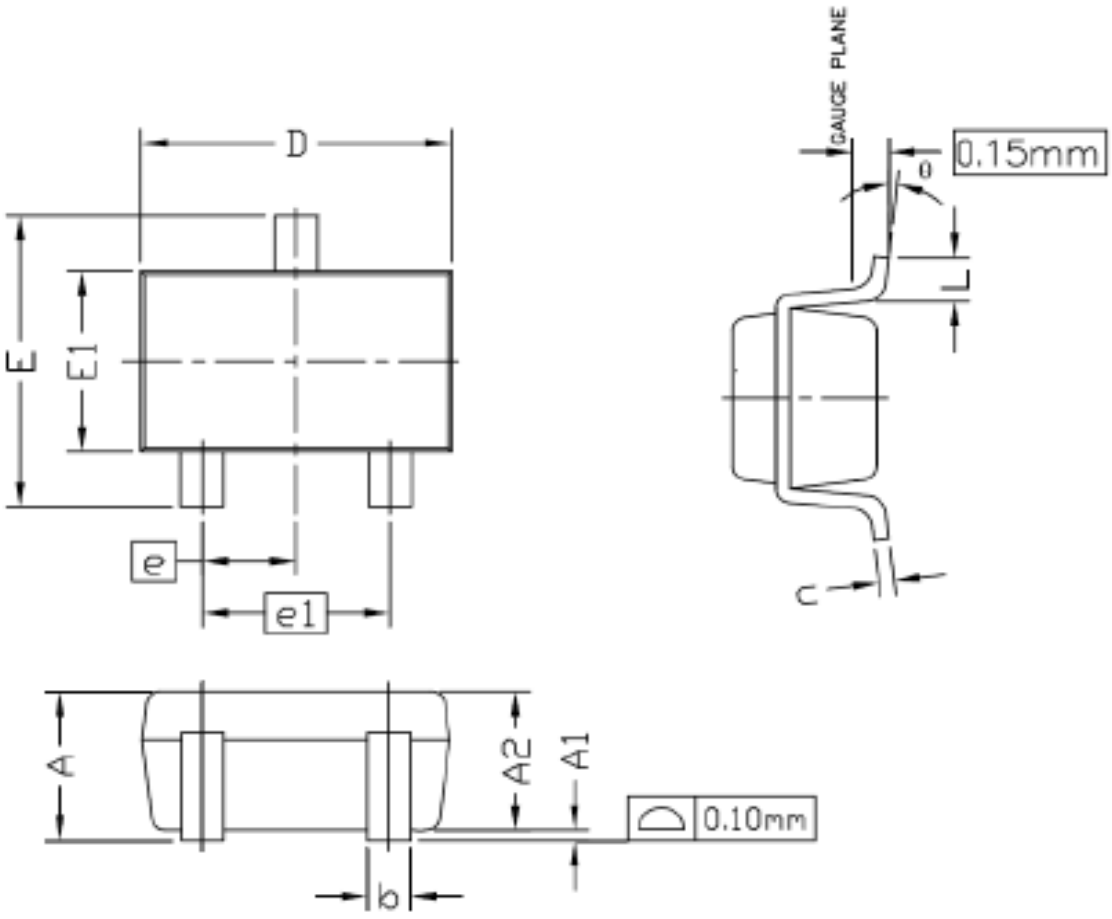
ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

SC-70-3L(SOT-323) Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.20	0.40
c	0.08	0.22
D	1.80	2.20
E	1.80	2.45
e	0.65 BSC	
e1	1.30 BSC	
E1	1.10	1.40
L	0.20	0.46
θ	0°	8°