

N-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4410 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

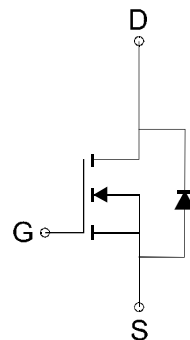
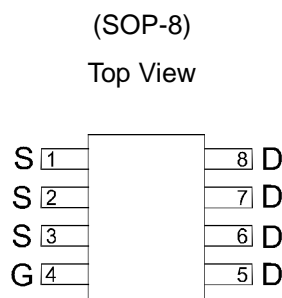
FEATURES

- $R_{DS(ON)} \leq 18m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 20m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

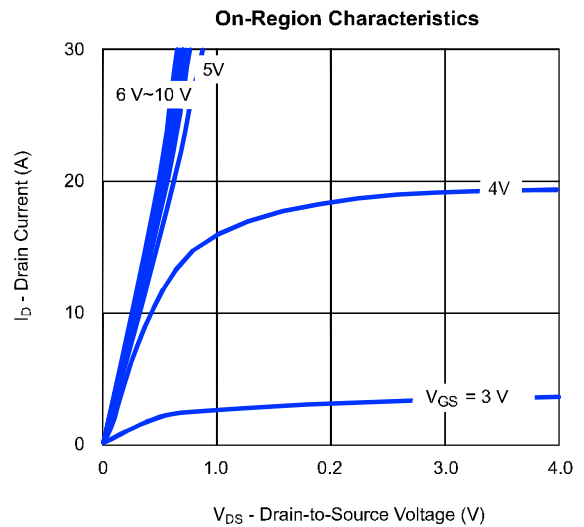
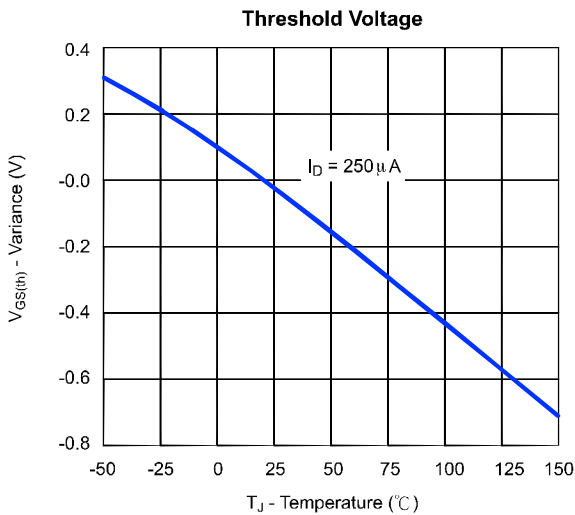
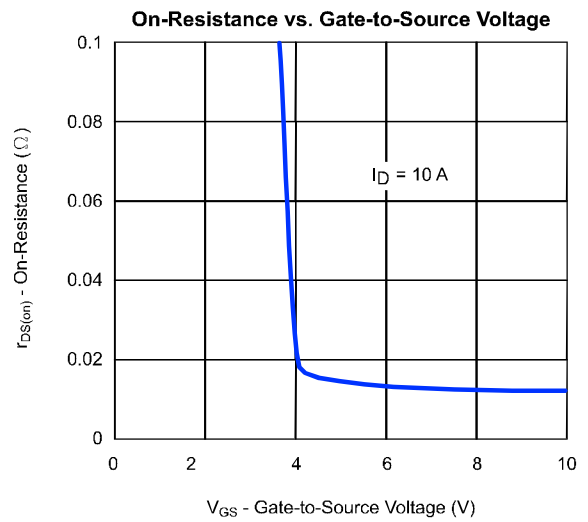
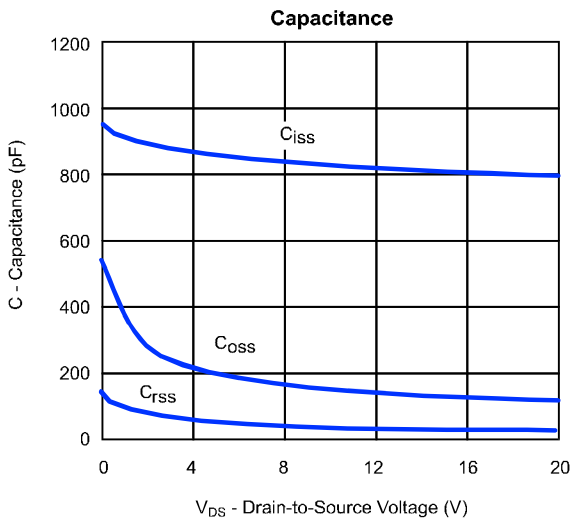
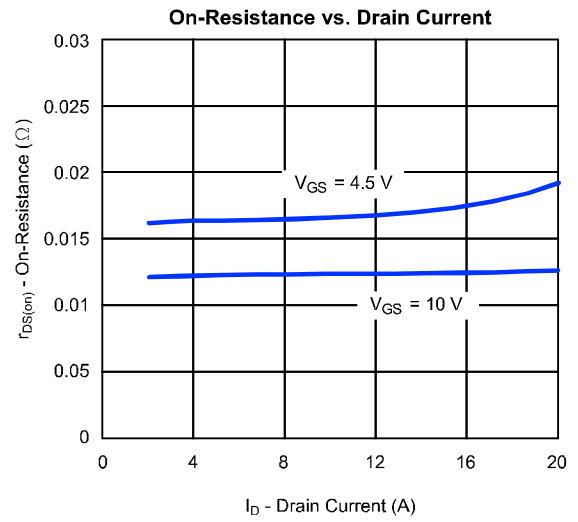
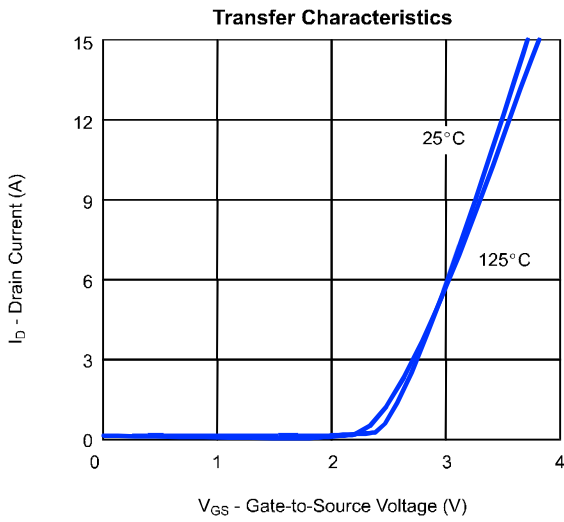
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	± 20		V
Continuous Drain Current ($T_j=150^\circ C$)	$T_A=25^\circ C$	I_D	10	7.5	A
	$T_A=70^\circ C$		8	6	
Pulsed Drain Current		I_{DM}	50		A
Continuous Source Current (Diode Conduction)		I_S	2.3	1.26	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	2.5	1.4	W
	$T_A=70^\circ C$		1.6	0.9	
Operating Junction Temperature		T_J	-55 to 150		$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	$T \leq 10 \text{ sec}$	35	$^\circ C/W$
			Steady State	60	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	32		$^\circ C/W$

*The device mounted on 1in² FR4 board with 2 oz copper

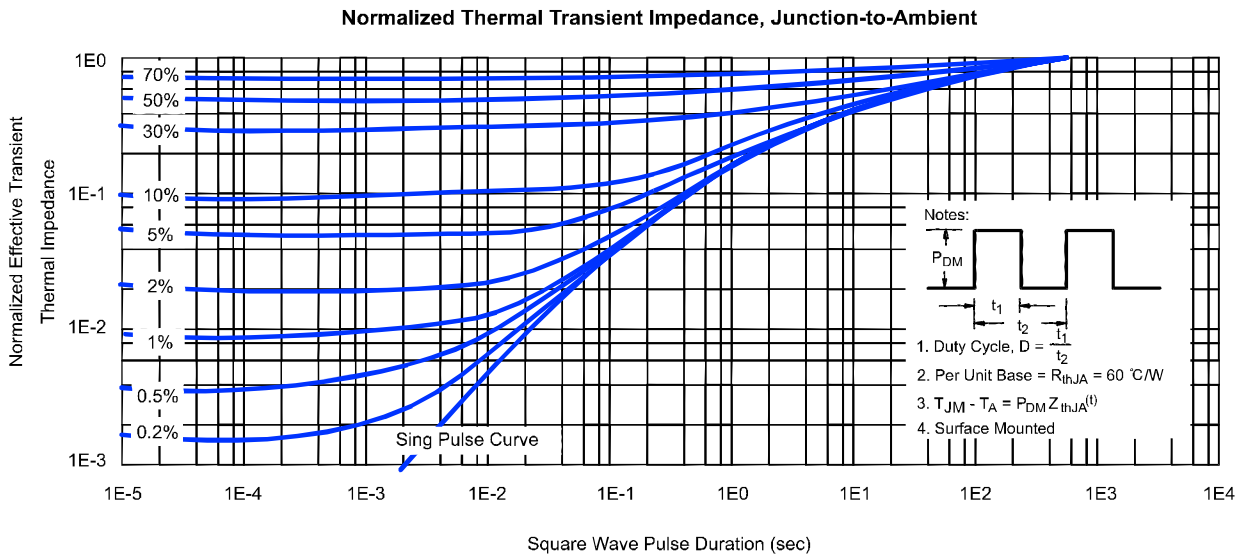
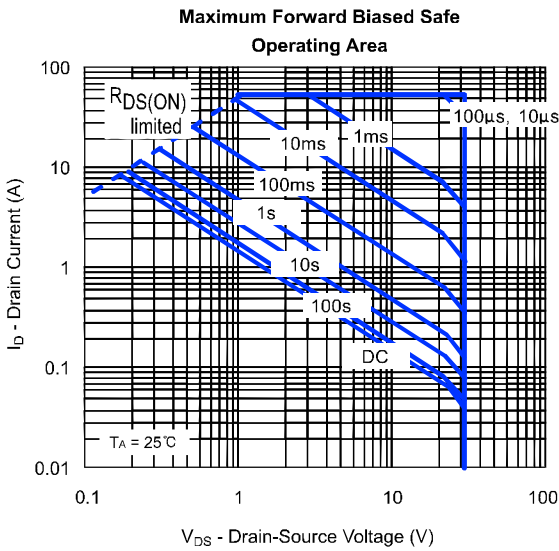
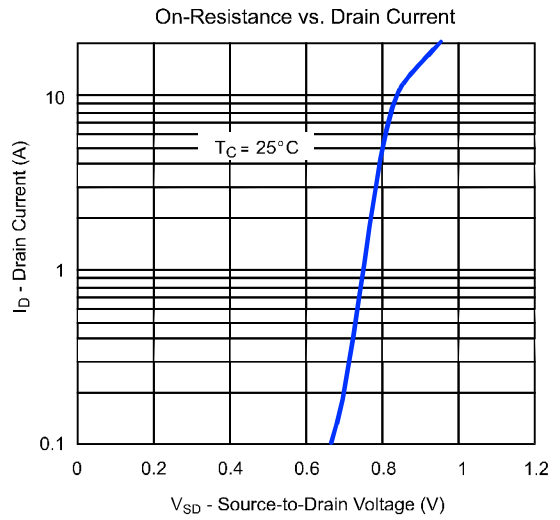
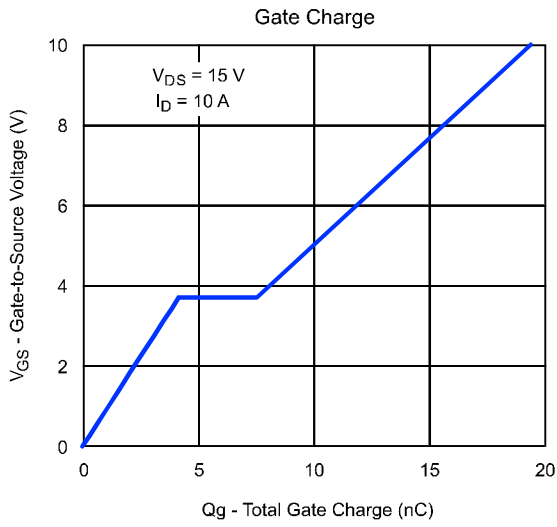
Electrical Characteristics (T_A = 25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.0	2.0	3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
		V _{DS} =30V, V _{GS} =0V T _J =55°C			5	
I _{D(ON)}	On-State Drain Current	V _{DS} ≥ 5V, V _{GS} = 10V	20			A
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D = 10A		12	18	mΩ
		V _{GS} =4.5V, I _D = 5A		16	20	
G _{FS}	Forward Transconductance	V _{DS} =15V, I _D =10A		17		S
V _{SD}	Diode Forward Voltage	I _S =2.3A, V _{GS} =0V		0.76	1.1	V
DYNAMIC						
Q _g	Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =10A		10	13	nC
Q _{gt}	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =10A		20	25	
Q _{gs}	Gate-Source Charge			4.2		
Q _{gd}	Gate-Drain Charge			4.7		
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		810	950	pF
C _{oss}	Output Capacitance			140		
C _{rss}	Reverse Transfer Capacitance			40		
R _g	Gate Resistance	f = 1MHz		1.7		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =25V, R _L =25Ω I _D =1A, V _{GEN} =10V R _G =6Ω		14	17	ns
t _r	Turn-On Rise Time			12	15	
t _{d(off)}	Turn-Off Delay Time			43	55	
t _f	Turn-On Fall Time			4	6	
t _{rr}	Source-Drain Reverse Recovery Time		I _F =2.3A, di/dt=100A/μs		35	

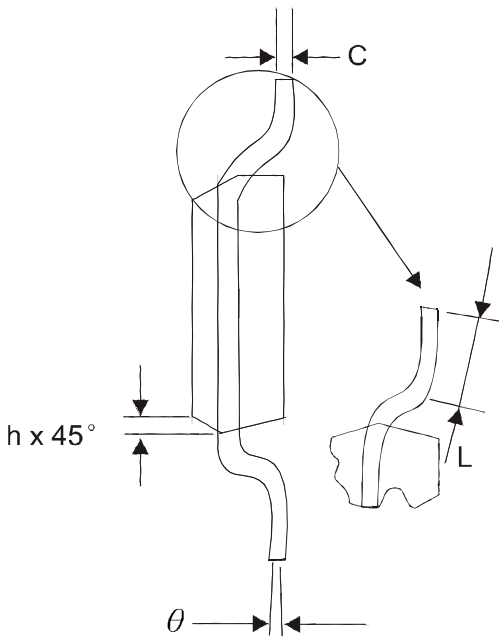
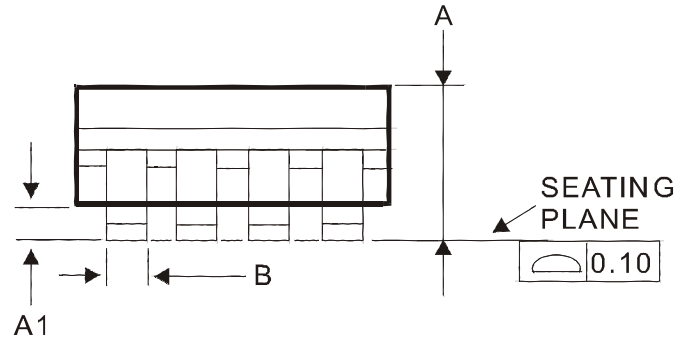
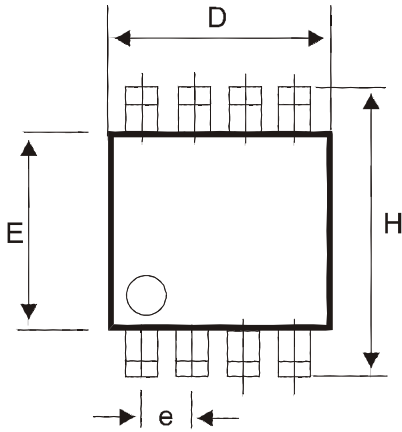
Typical Characteristics (T_J = 25°C Noted)



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SOP-8 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.