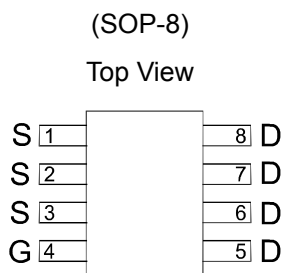


**P-Channel 30-V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME4425 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION**

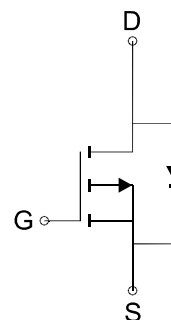


**FEATURES**

- $R_{DS(ON)} \leq 14m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 19m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P-Channel MOSFET

Ordering Information: ME4425 (Pb-free)

ME4425-G (Green product-Halogen free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	-10.6
		$T_A = 70^\circ C$	-8.5
Pulsed Drain Current	$I_{DM}$	-42	A
Avalanche Current	$I_{AR}$	-44	A
Avalanche Energy with Single Pulse(L=0.1mH)	$E_{AS}$	96.8	mJ
Maximum Power Dissipation	$P_D$	$T_A = 25^\circ C$	2.5
		$T_A = 70^\circ C$	1.6
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	50	$^\circ C/W$

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

## P-Channel 30-V (D-S) MOSFET

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA	-1		-3	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V			-1	μA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> = -9.1A		10	14	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> = -6.9A		15	19	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-2.1A, V <sub>GS</sub> =0V		-0.8	-1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-9.1A		67		nC
Q <sub>gs</sub>	Gate-Source Charge			11		
Q <sub>gd</sub>	Gate-Drain Charge			17		
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz		3100		pF
C <sub>oss</sub>	Output Capacitance			383		
C <sub>rss</sub>	Reverse Transfer Capacitance			312		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, R <sub>L</sub> =15Ω I <sub>D</sub> =-1A, V <sub>GEN</sub> =-10V R <sub>G</sub> =6Ω		43.9		ns
t <sub>r</sub>	Turn-On Rise Time			18.3		
t <sub>d(off)</sub>	Turn-Off Delay Time			209		
t <sub>f</sub>	Turn-On Fall Time			56		

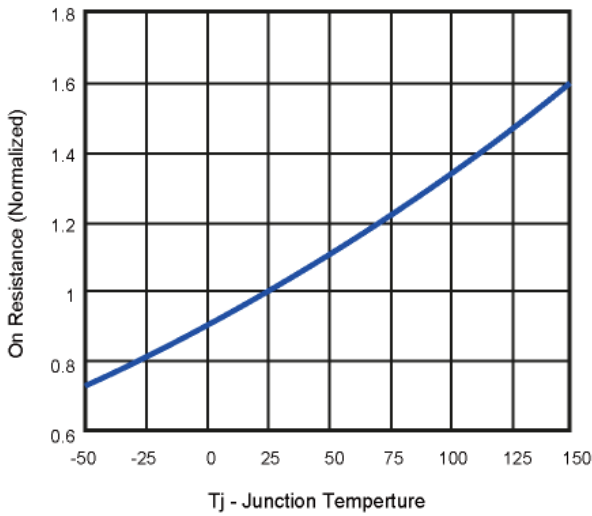
Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

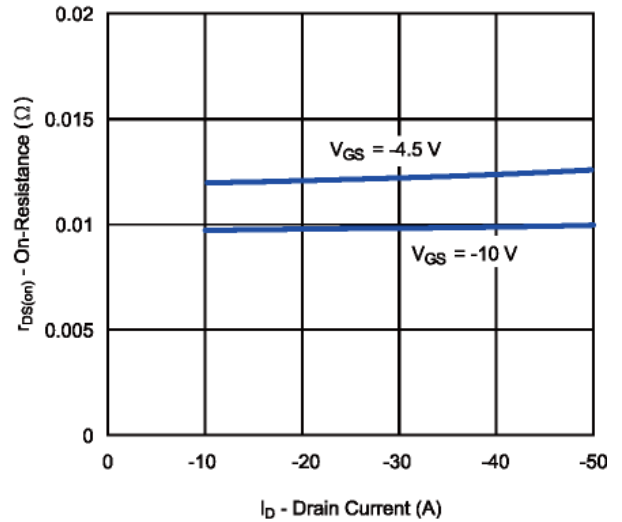
**P-Channel 30-V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

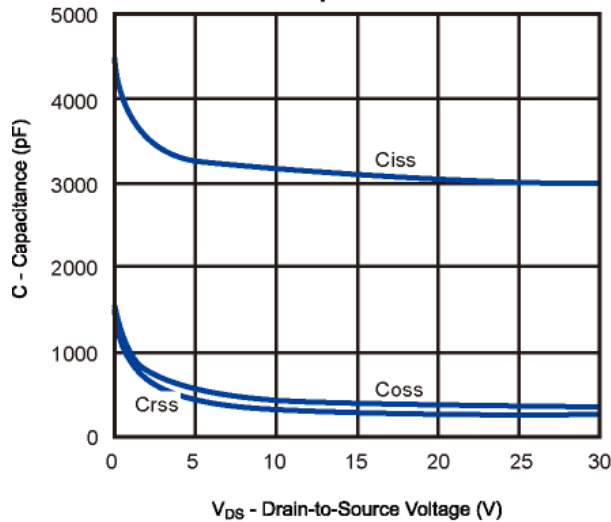
**On Resistance vs. Junction Temperature**



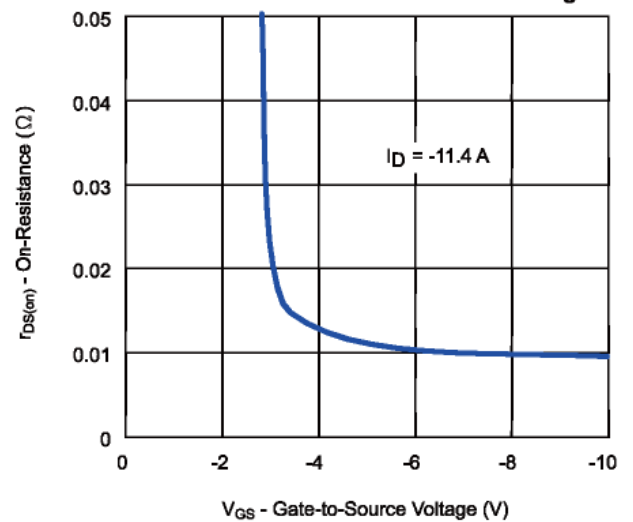
**On-Resistance vs. Drain Current**



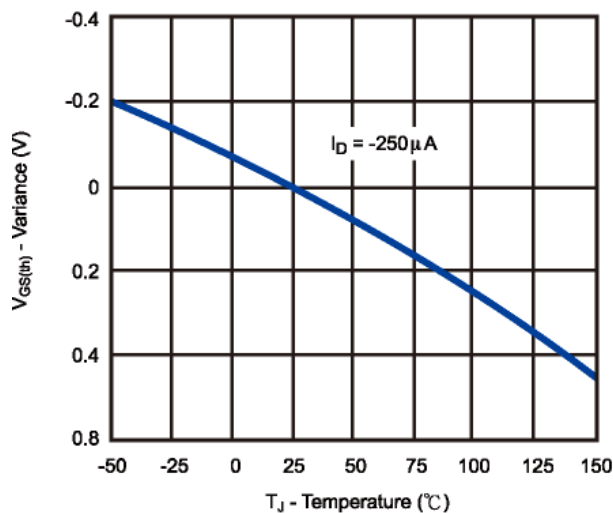
**Capacitance**



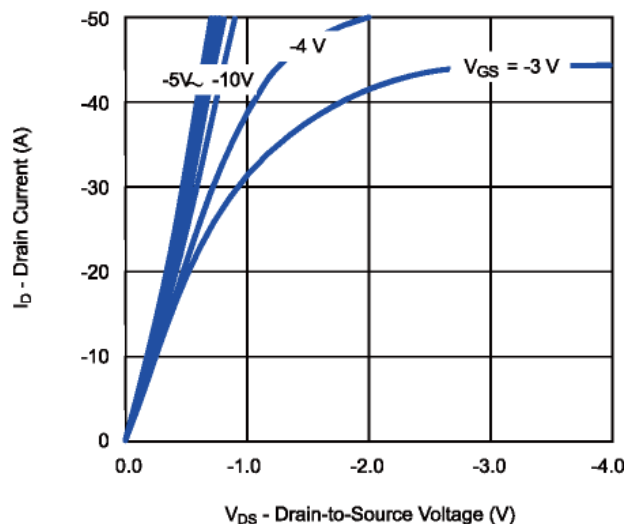
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**

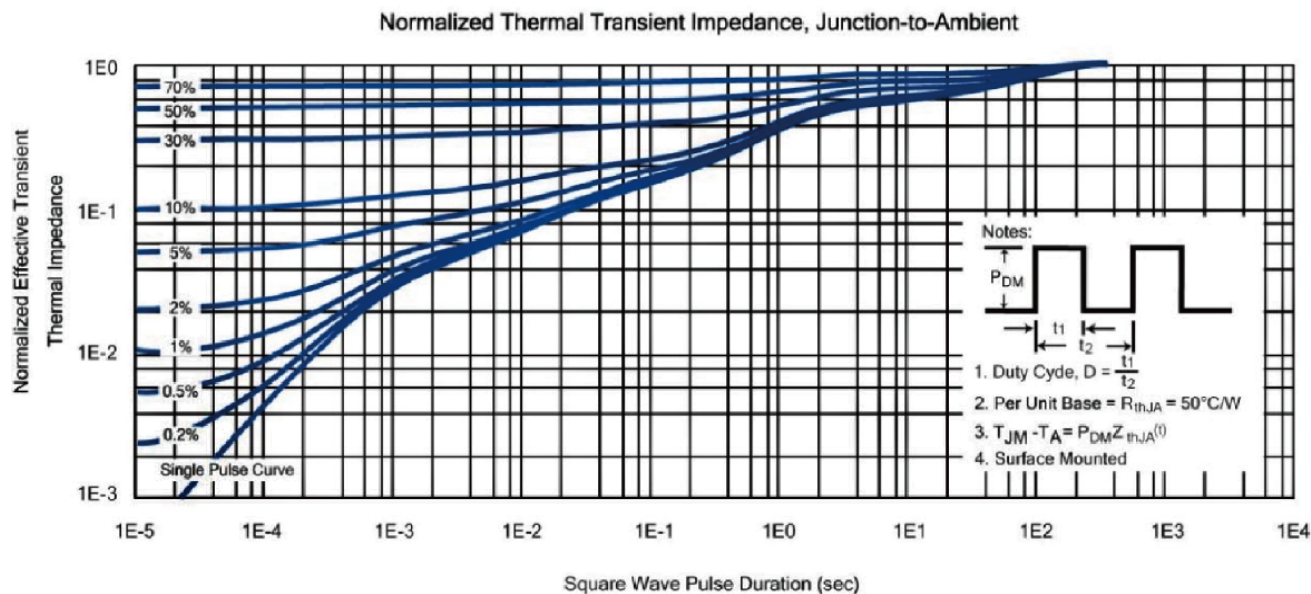
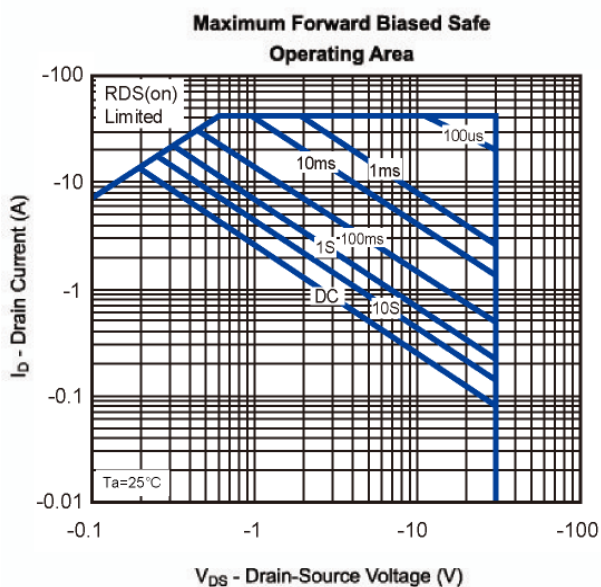
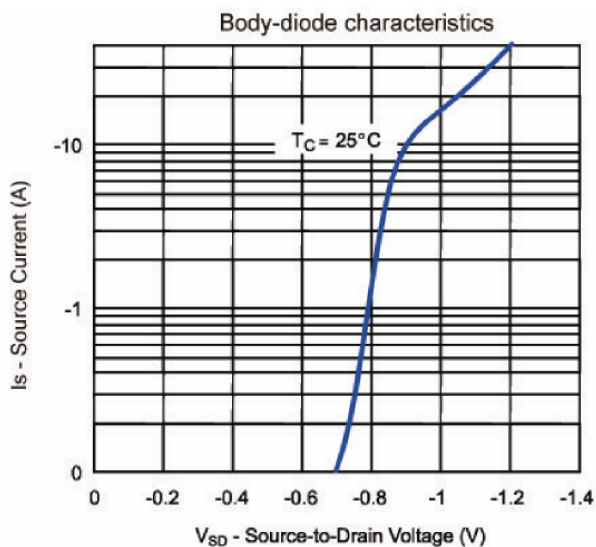
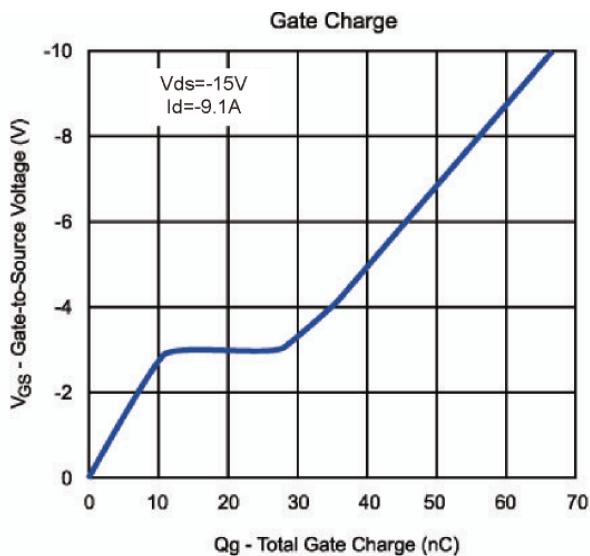


**On-Region Characteristics**

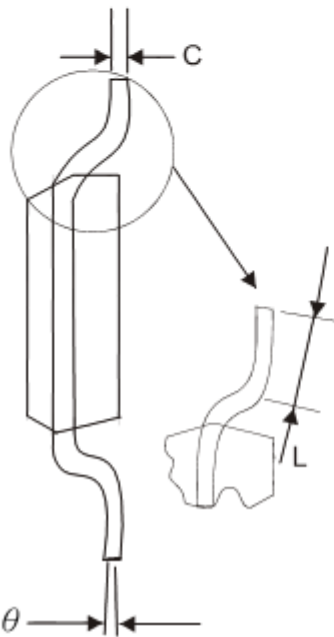
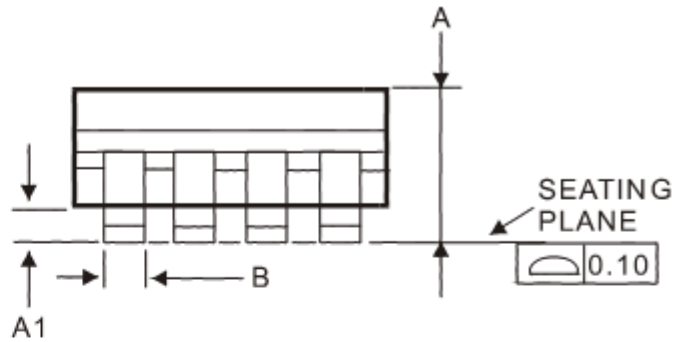
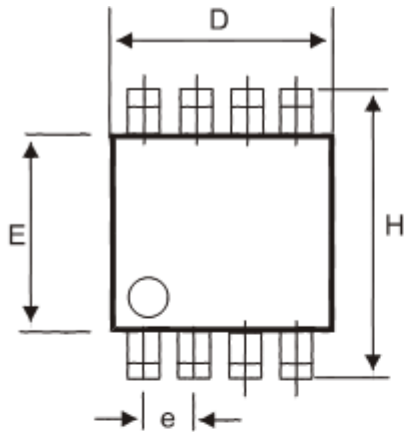


**P-Channel 30-V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**



**SOP-8 Package Outline**



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
$\theta$	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.