

P-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4435 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

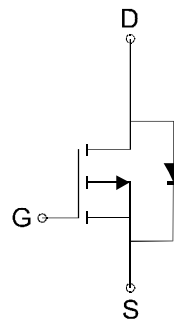
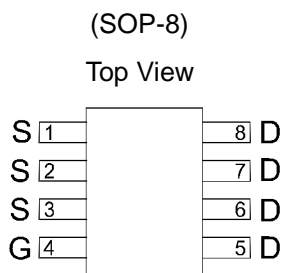
FEATURES

- -30V/-9.1A, $R_{DS(ON)}=20m\Omega @ V_{GS}=-10V$
- -30V/-6.9A, $R_{DS(ON)}=35m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION



P-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DSS}		-30	V	
Gate-Source Voltage	V_{GSS}		± 20	V	
Continuous Drain Current ($t_J=150^\circ\text{C}$)	I_D	$T_A=25^\circ\text{C}$	-9.1	-7	A
		$T_A=70^\circ\text{C}$	-7.3	-5.6	
Pulsed Drain Current	I_{DM}		-30	A	
Avalanche Energy with Single Pulse ($L=0.1\text{mH}$)	EAS		50	mJ	
Continuous Source Current (Diode Conduction)	I_S	-2.1	-1.25	A	
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.5	1.5	W
		$T_A=70^\circ\text{C}$	1.6	0.9	
Operating Junction Temperature	T_J	-55 to 150		$^\circ\text{C}$	
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	$T \leq 10 \text{ sec}$	30	$^\circ\text{C/W}$	
		Steady State	62		
Thermal Resistance-Junction to Case	$R_{\theta JC}$	38		$^\circ\text{C/W}$	

*The device mounted on 1in^2 FR4 board with 2 oz copper

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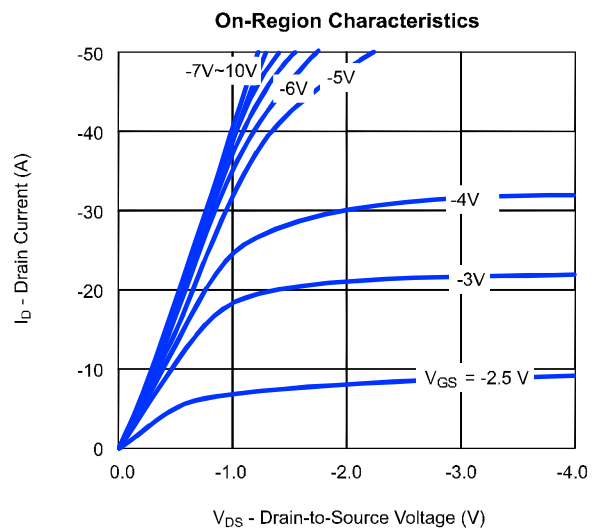
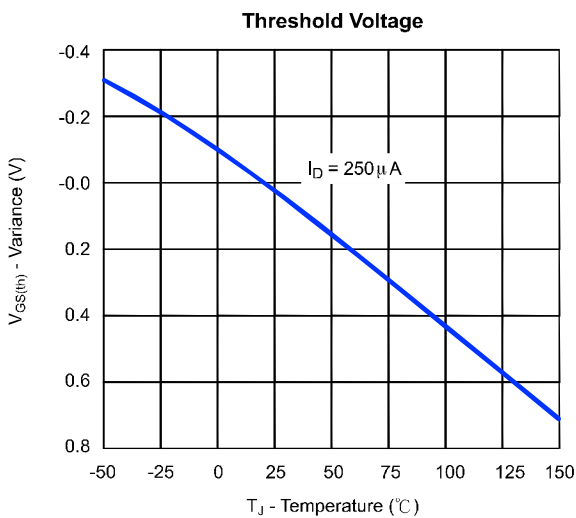
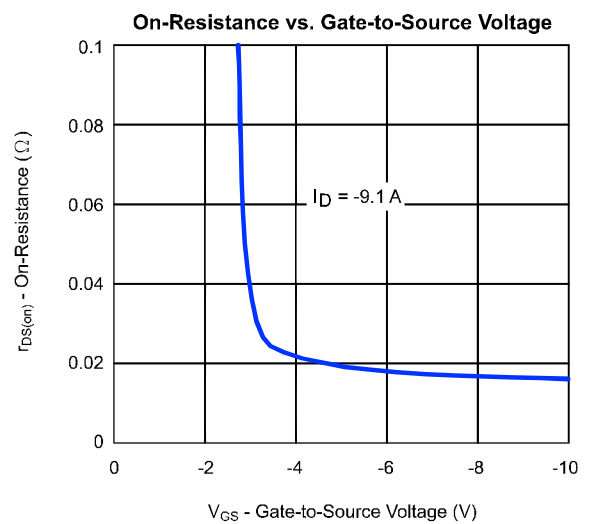
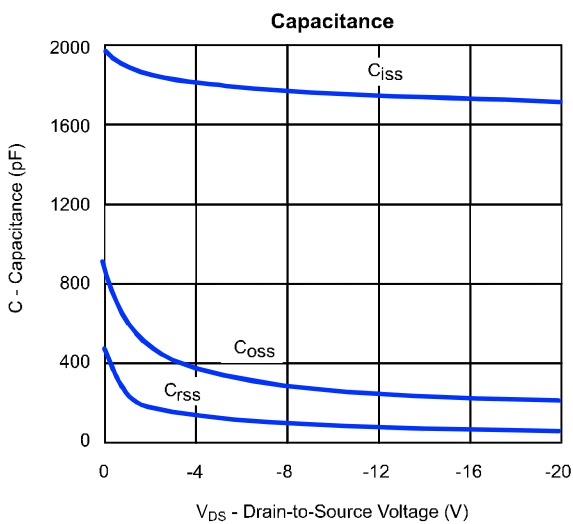
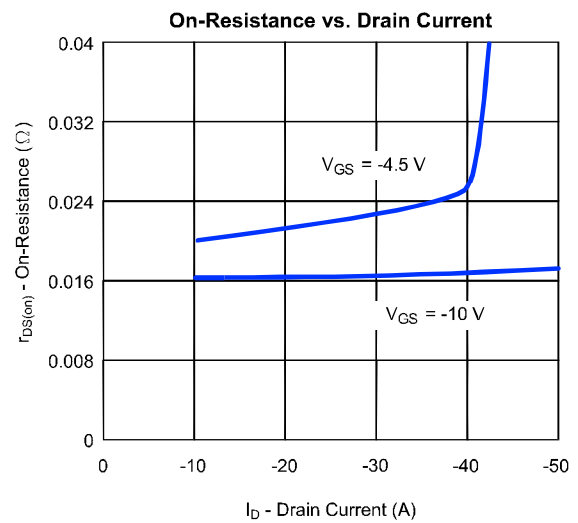
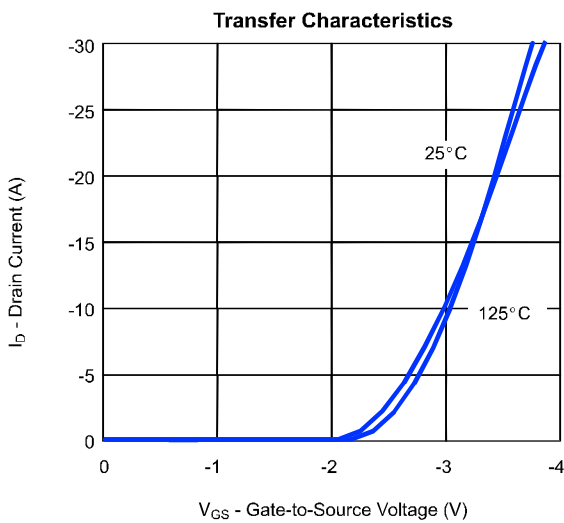
Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1	-1.4	-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
		V _{DS} =-30V, V _{GS} =0V			-25	
		T _J =55°C				
I _{D(ON)}	On-State Drain Current ^a	V _{DS} =-5V, V _{GS} =-10V	-30			A
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-9.1A		15	20	mΩ
		V _{GS} =-4.5V, I _D =-6.9A		25	35	
V _{SD}	Diode Forward Voltage	I _S =-2.1A, V _{GS} =0V		-0.8	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-9.1A		38	45	nC
Q _{gs}	Gate-Source Charge			7.7		
Q _{gd}	Gate-Drain Charge			9		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		5.5		Ω
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		1730	1900	pF
C _{oss}	Output Capacitance			240		
C _{rss}	Reverse Transfer Capacitance			70		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1A, V _{GEN} =-10V R _G =6Ω		41	50	ns
t _r	Turn-On Rise Time			19	23	
t _{d(off)}	Turn-Off Delay Time			105	120	
t _f	Turn-Off Fall Time			17	20	

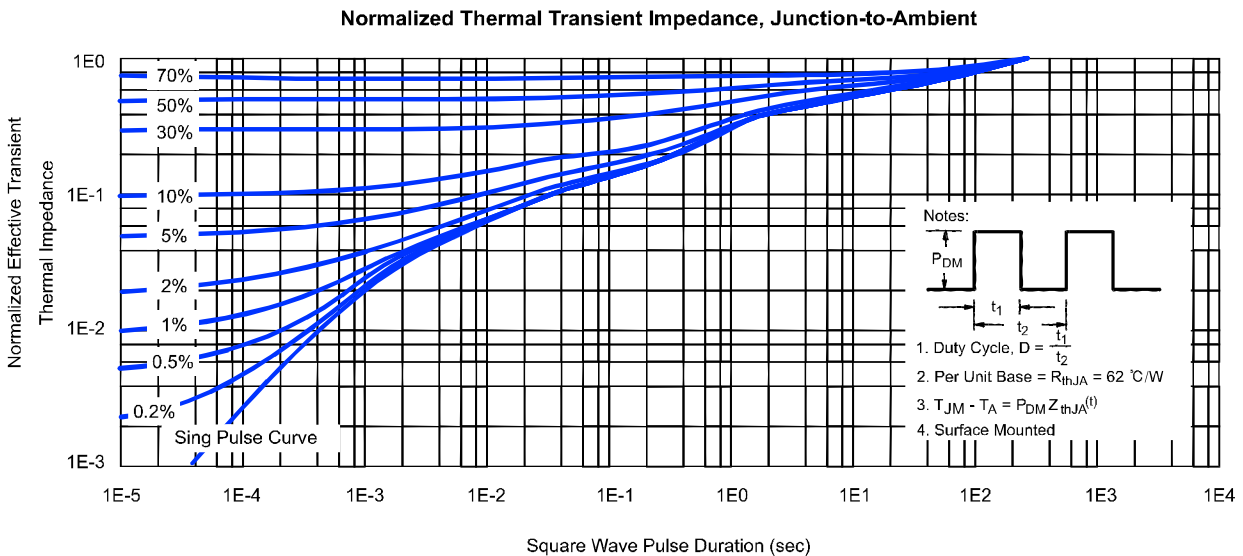
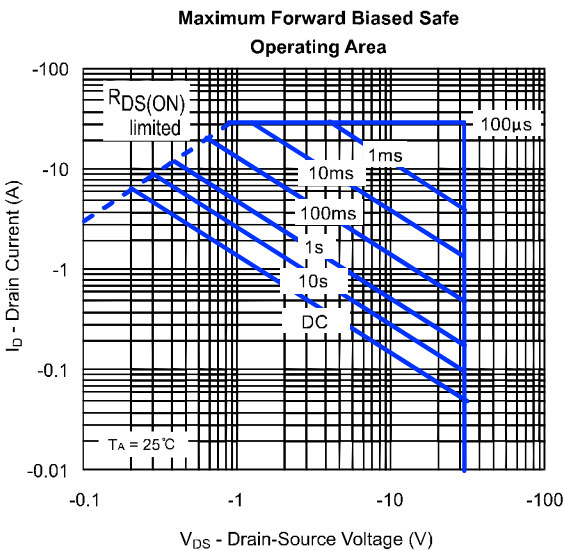
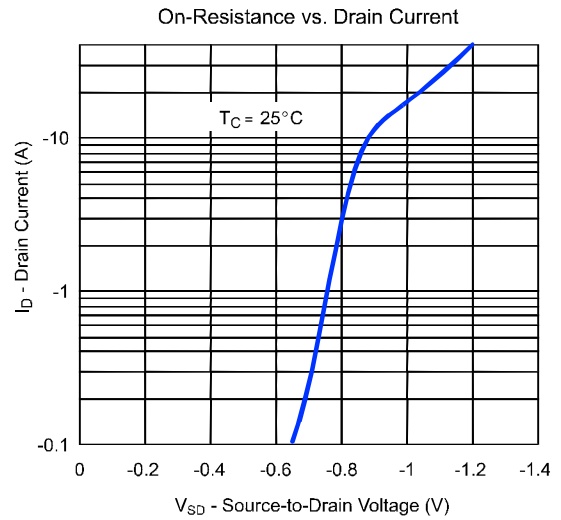
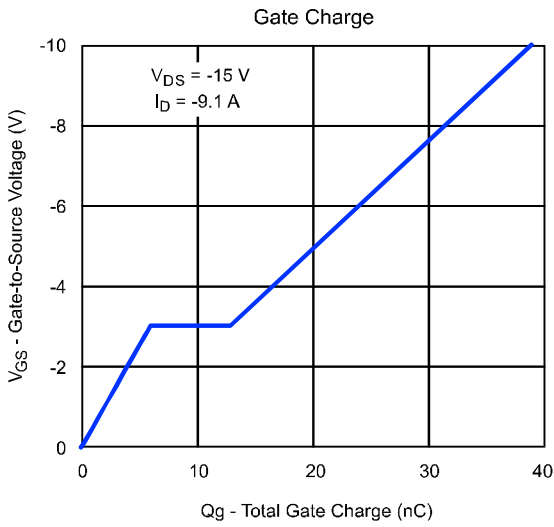
Notes:

a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

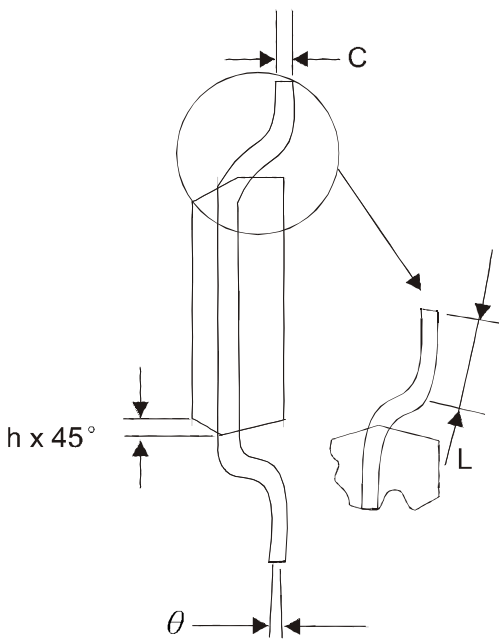
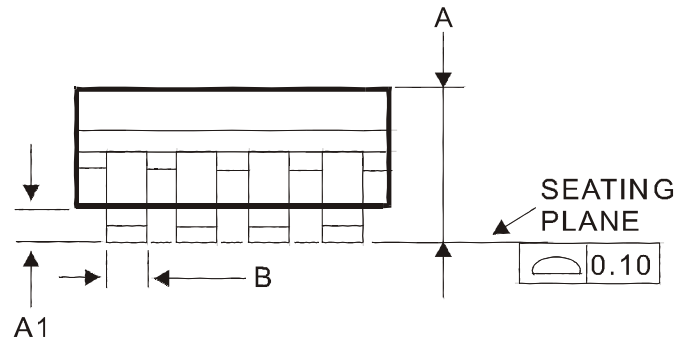
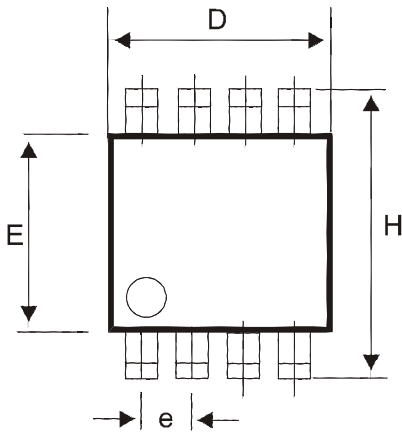
Typical Characteristics (T_J = 25°C Noted)



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SOP-8 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°