

**N-Channel 40-V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME4456 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

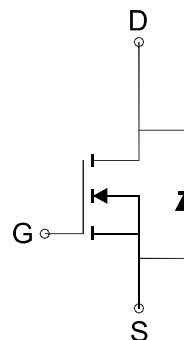
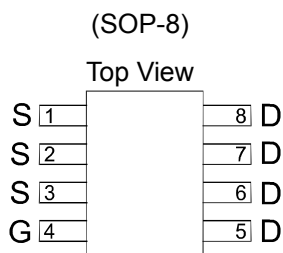
**FEATURES**

- $R_{DS(ON)} \leq 24m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 39m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- Battery Powered System
- DC/DC Converter
- Load Switch

**PIN CONFIGURATION**



N-Channel MOSFET

Ordering Information: ME4456 (Pb-free)

ME4456-G (Green product- Halogen free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DSS}$	40	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 150^\circ C$ )*	$I_D$	$T_A = 25^\circ C$	8
		$T_A = 70^\circ C$	6.5
Pulsed Drain Current	$I_{DM}$	32	A
Maximum Power Dissipation*	$P_D$	$T_A = 25^\circ C$	2.5
		$T_A = 70^\circ C$	1.6
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	50	$^\circ C/W$

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper



## N-Channel 40-V (D-S) MOSFET

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	40			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1		3	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(on)</sub>	Drain-Source On-State Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A		20	24	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		31	39	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =10A, V <sub>GS</sub> =0V		0.9	1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge(10V)	V <sub>DS</sub> =20V, V <sub>GS</sub> =10V, I <sub>D</sub> =6A		15		nC
Q <sub>g</sub>	Total Gate Charge(4.5V)	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		7.8		
Q <sub>gs</sub>	Gate-Source Charge			3.4		
Q <sub>gd</sub>	Gate-Drain Charge			3.8		
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1.0MHz		539		pF
C <sub>oss</sub>	Output Capacitance			76		
C <sub>rss</sub>	Reverse Transfer Capacitance			24		
R <sub>g</sub>	Gate-Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		0.9		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V, R <sub>L</sub> =15Ω V <sub>GEN</sub> =10V, R <sub>G</sub> =6Ω		13		ns
t <sub>r</sub>	Turn-On Rise Time			13		
t <sub>d(off)</sub>	Turn-Off Delay Time			37		
t <sub>f</sub>	Turn-Off Fall Time			4		

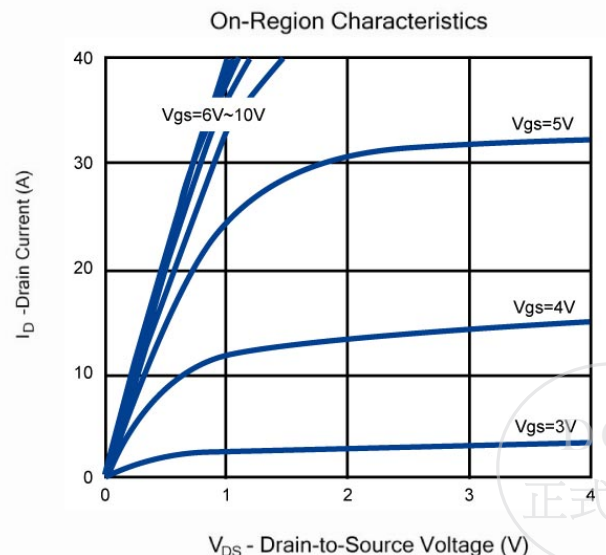
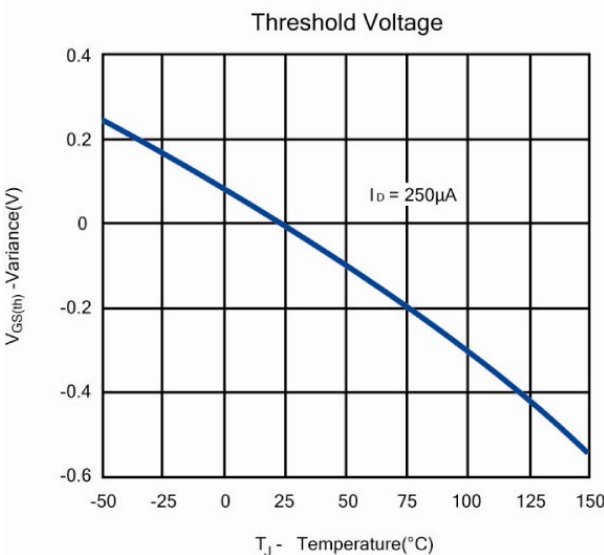
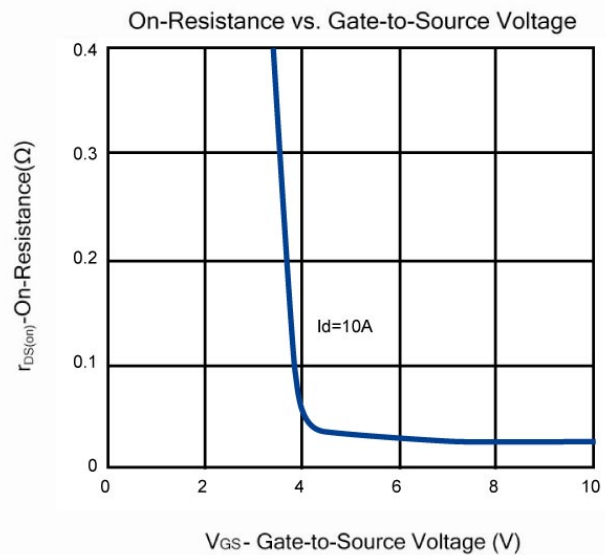
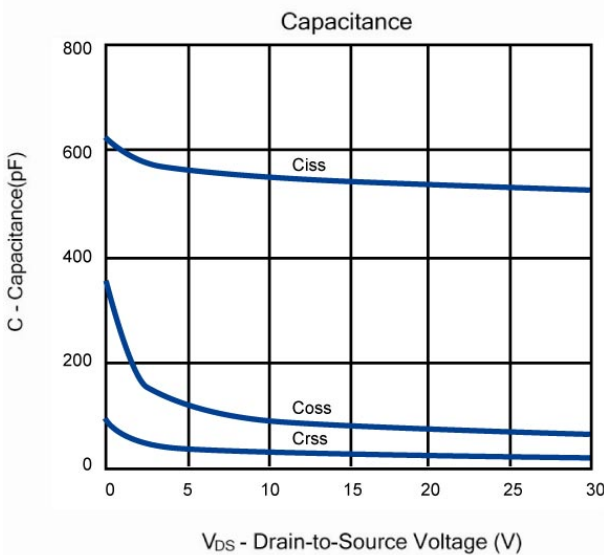
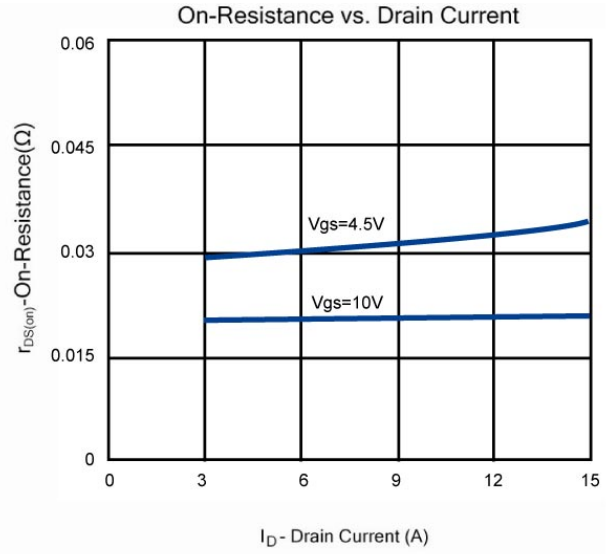
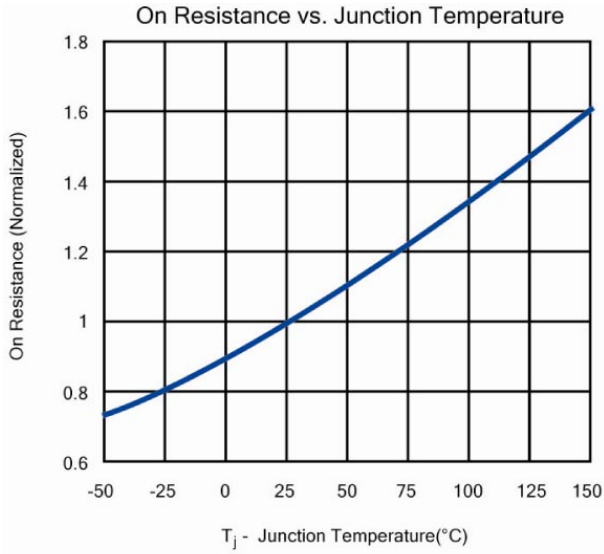
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.



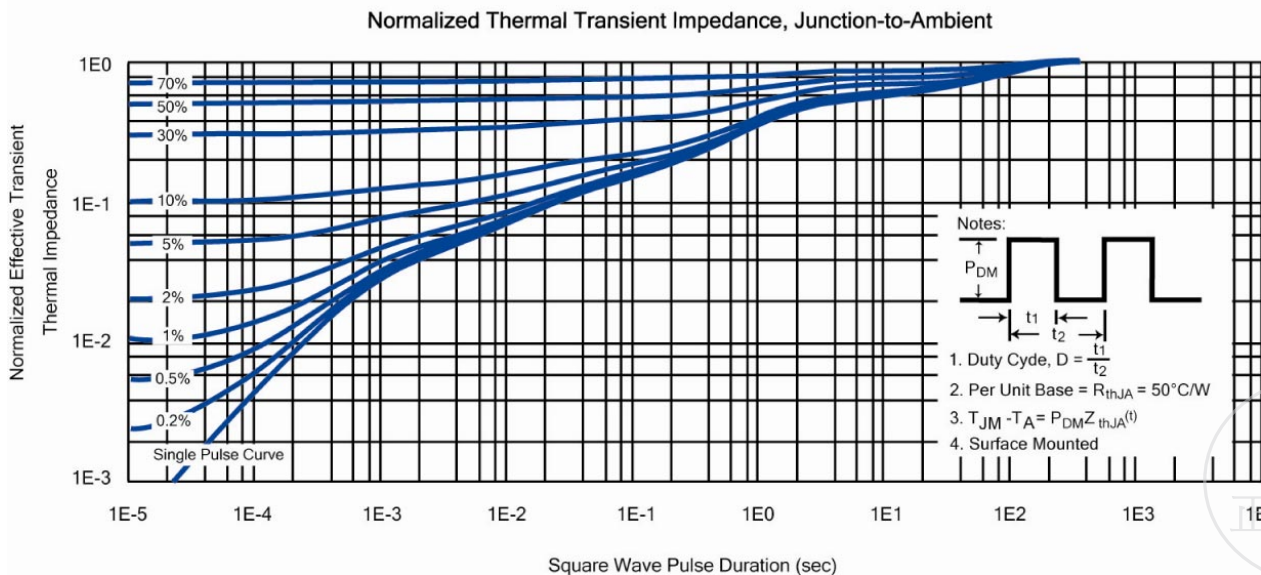
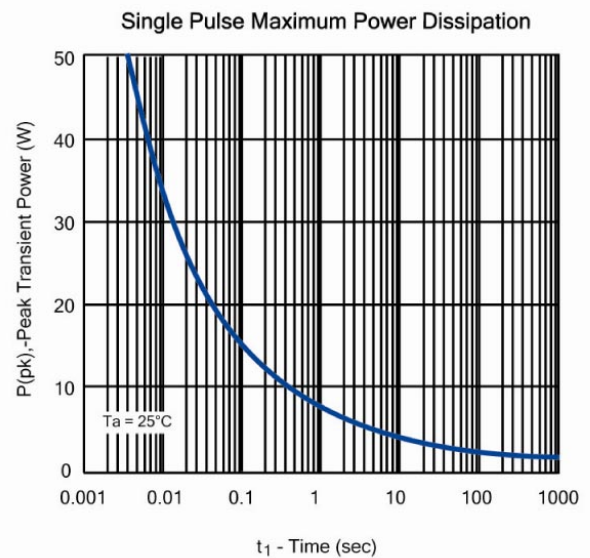
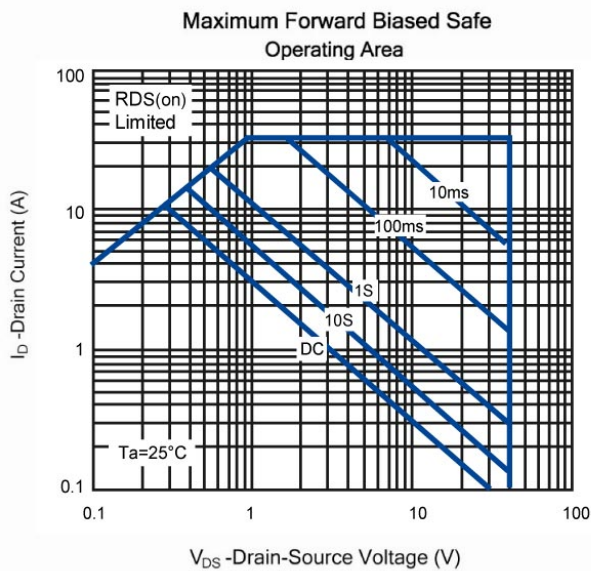
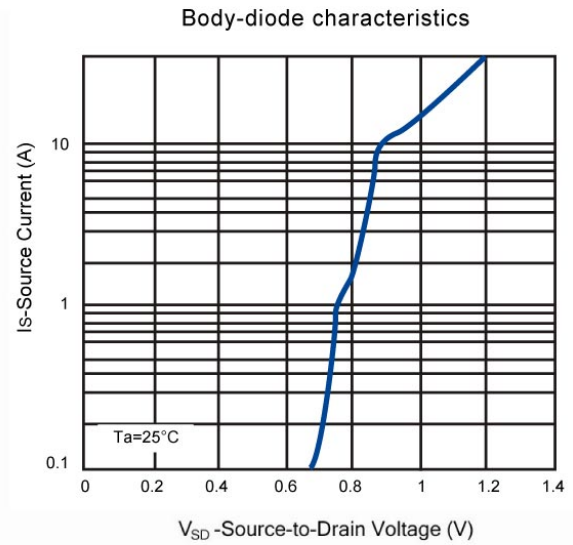
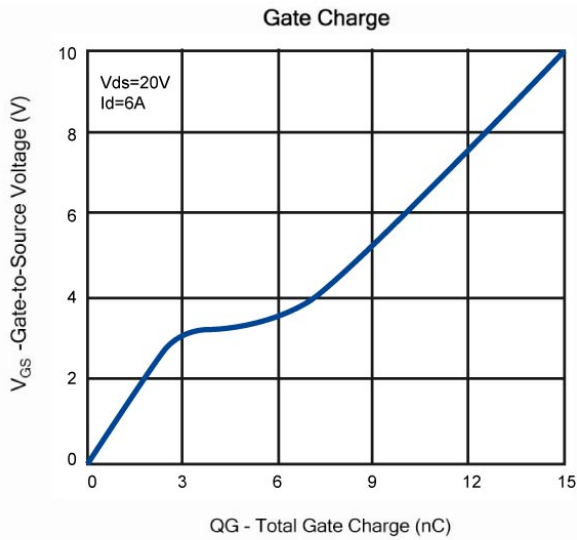
**N-Channel 40-V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

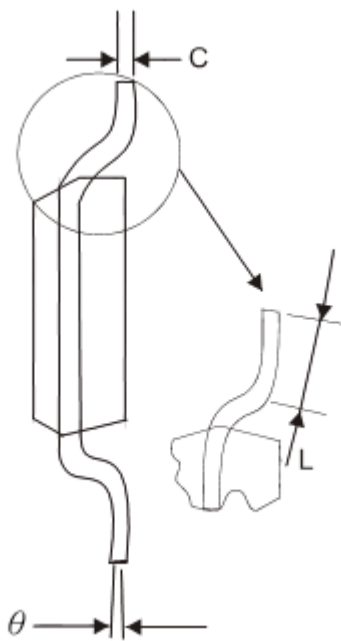
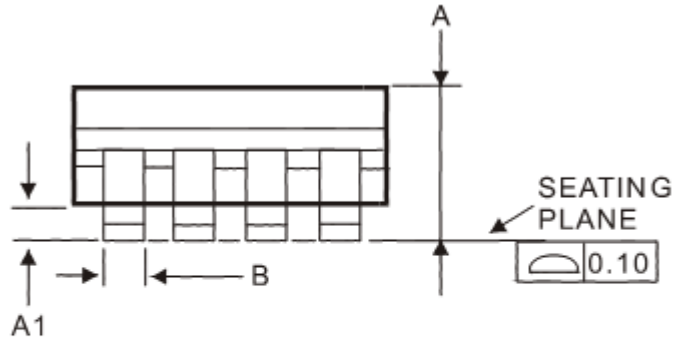
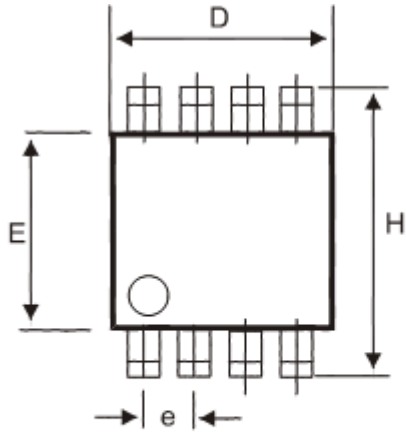


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**SOP-8 Package Outline**



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
$\theta$	0°	7°

